



3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/ CHECKERS AND BUS-HOLD

IDT74ALVCH16901

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(O)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{CC} = 3.3V \pm 0.3V$, Normal Range
- $V_{CC} = 2.7V$ to $3.6V$, Extended Range
- $V_{CC} = 2.5V \pm 0.2V$
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in TSSOP package

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

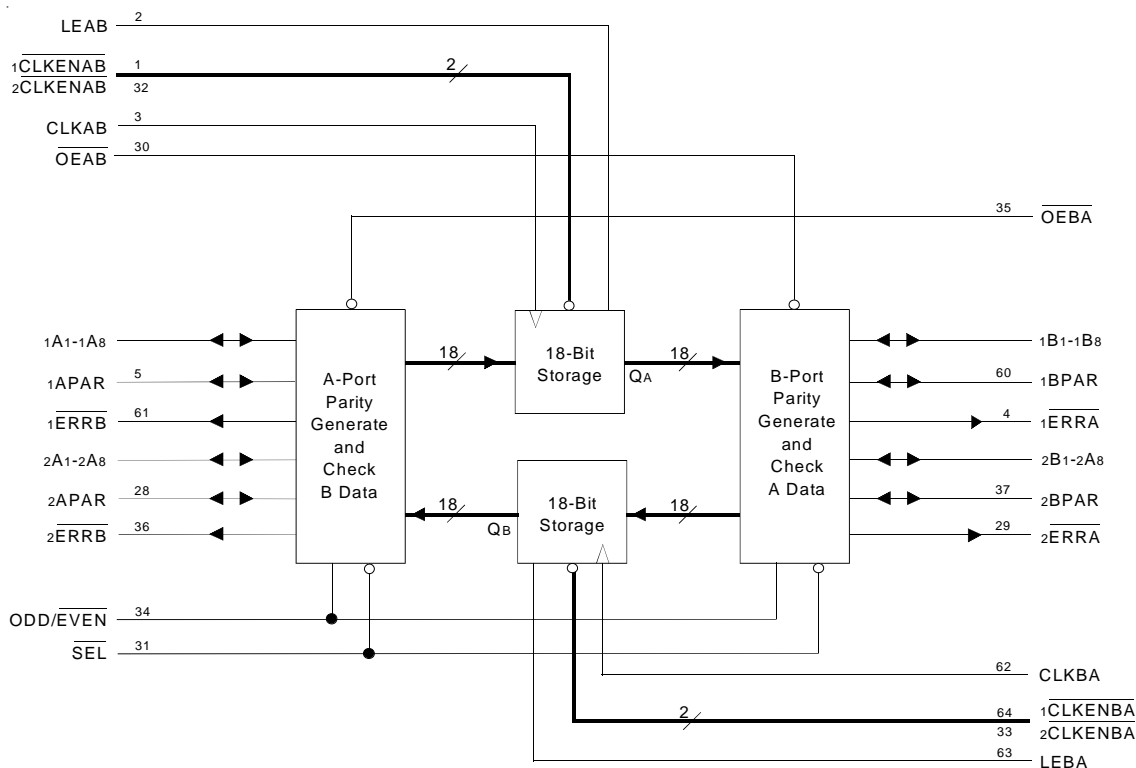
This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver or it can generate/check parity from the two 8-bit data buses in either direction.

The ALVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock enable ($\overline{CLKENAB}$ or $\overline{CLKENBA}$) inputs. It also provides parity-enable (\overline{SEL}) and parity-select (ODD/EVEN) inputs and separate error-signal (\overline{ERRA} and \overline{ERRB}) outputs for checking parity. The direction of data flow is controlled by \overline{OEAB} and \overline{OEBA} . When \overline{SEL} is low, the parity functions are enabled. When \overline{SEL} is high, the parity functions are disabled and the device acts as an 18-bit registered transceiver.

The ALVCH16901 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16901 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

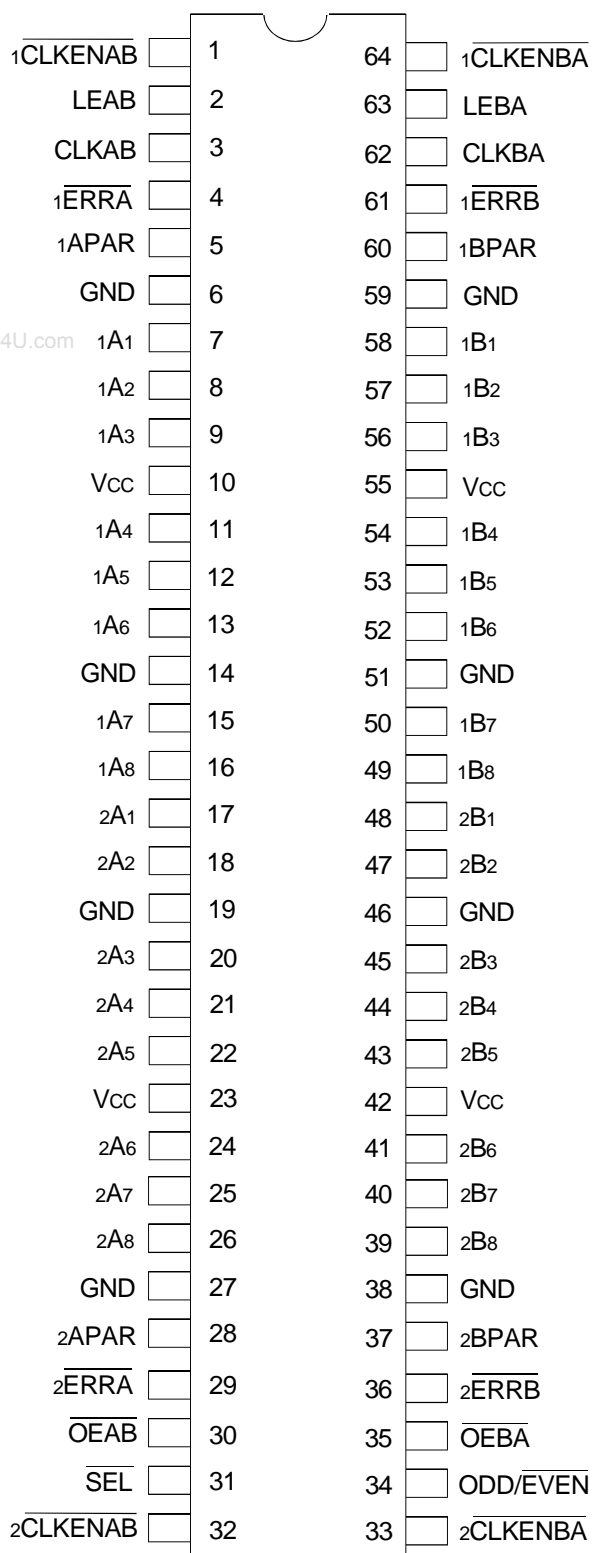
FUNCTIONAL BLOCK DIAGRAM



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INDUSTRIAL TEMPERATURE RANGE

PIN CONFIGURATION



TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, VI < 0 or VI > VCC	±50	mA
IOK	Continuous Clamp Current, VO < 0	-50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VCC terminals.
- All terminals except VCC.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COUT	Output Capacitance	VOUT = 0V	7	9	pF
COUT	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

- As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
\overline{OEAB}	A-to-B Output Enable Input (Active LOW)
\overline{OEBA}	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{xCLKENAB}$	A-to-B 9-bit Clock Enables
$\overline{xCLKENBA}$	B-to-A 9-bit Clock Enables
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
\overline{xERRA}	A Error-Signal Outputs
\overline{xERRB}	B Error-Signal Outputs
xAPAR	A Port Parities
xBPAPAR	B Port Parities
ODD/EVEN	Parity Select Input
\overline{SEL}	Parity Enables
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

- These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLE^(1,2)

Inputs					Outputs
CLKENAB	OEAB	LEAB	CLKAB	xAx	xBx
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ⁽³⁾
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ⁽³⁾
L	L	L	H	X	B ⁽⁴⁾

PARITY ENABLE

Inputs			Operation or Function	
SEL	OEBA	OEAB		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.	Qa data to B, Qb data to A
H	L	H		Qb data to A
H	H	L		Qa data to B
H	H	H		Isolation

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKENBA.
3. Output level before the indicated steady-state conditions were established.
4. Output level before the indicated steady-state conditions were established, provided that CLKAB was LOW before LEAB went LOW.

PARITY

Inputs							Outputs				
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1--A8 = H	Σ OF INPUTS B1--B8 = H	xAPAR	xBPAR	xAPAR	xERRA	xBPAR	xERRB
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	N/A	H	N/A	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	N/A	L	N/A	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	N/A	L	N/A	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	N/A	H	N/A	H
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	N/A	L	N/A	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	N/A	H	N/A	H
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	N/A	H	N/A	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	N/A	L	N/A	L
L	L	L	L	N/A	N/A	N/A	N/A	PE ⁽¹⁾	Z	PE ⁽¹⁾	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO ⁽²⁾	Z	PO ⁽²⁾	Z

NOTES:

1. Parity output is set to the level so that the specific bus side is set to even parity.
2. Parity output is set to the level so that the specific bus side is set to odd parity.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	±5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V		—	—	±10	μA
		V _O = GND		—	—	±10	
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC1} I _{CC2} I _{CC3}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3V		—	—	—	μA
		V _I = 0.8V		75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V		—	—	—	μA
		V _I = 0.7V		45	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V		V _I = 0 to 3.6V		±500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = - 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V		I _{OH} = - 24mA	2	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to + 85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz	22	27	pF
CPD	Power Dissipation Capacitance Outputs disabled		5	8	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		125	—	125	—	125	—	MHz
t _{PLH} t _{PHL}	Propagation Delay xAx to xBx or xBx to xAx	1	5.2	—	4.8	1	4.4	ns
t _{PLH} t _{PHL}	Propagation Delay xAx to xBPAR or xBx to xAPAR	2	8.9	—	7.6	2	6.7	ns
t _{PLH} t _{PHL}	Propagation Delay xAPAR to xBPAR or xBPAR to xAPAR	1	5.7	—	5.2	1	4.7	ns
t _{PLH} t _{PHL}	Propagation Delay xAPAR to xERRA or xBPAR to xERRB	2	9.7	—	8.7	2	7.5	ns
t _{PLH} t _{PHL}	Propagation Delay ODD/EVEN to xERRB or xERRA	1.5	8.7	—	7.9	1.5	6.8	ns
t _{PLH} t _{PHL}	Propagation Delay ODD/EVEN to xAPAR or xBPAR	1.5	8.3	—	7.6	1.5	6.5	ns
t _{PLH} t _{PHL}	Propagation Delay SEL to xAPAR or xBPAR	1	6.1	—	5.9	1	5.1	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xAx or LEAB to xBx	1	6	—	5.5	1	4.8	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xAPAR or LEAB to xBPAR (parity feed through)	1.5	6.7	—	6	1.5	5.3	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xAPAR or LEAB to xBPAR (parity generated)	2.5	9.8	—	8.3	2	7.4	ns
t _{PLH} t _{PHL}	Propagation Delay LEBA to xERRB or LEAB to xERRA	2.5	9.9	—	8.5	2	7.5	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xAx or CLKAB to xBx	1	6.4	—	5.8	1	5.1	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xAPAR or CLKAB to xBPAR (parity feed through)	1.5	7.1	—	6.3	1.5	5.6	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xAPAR or CLKAB to xBPAR (parity generated)	2.5	10.2	—	8.7	2	7.7	ns
t _{PLH} t _{PHL}	Propagation Delay CLKBA to xERRB or CLKAB to xERRA	2.5	10.5	—	8.9	2	7.9	ns

SWITCHING CHARACTERISTICS (CONTINUED)⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{PZH} t _{PZL}	Output Enable Time \overline{OEAB} or \overline{OEBA} to xBx, xBPAR or xAx, xAPAR	1.4	6.3	—	6.1	1	5.3	ns
t _{PZH} t _{PZL}	Output Enable Time \overline{OEAB} or \overline{OEBA} to \overline{xERRA} or \overline{xERRB}	1.4	6.2	—	5.5	1	4.9	ns
t _{PZH} t _{PZL}	Output Enable Time \overline{SEL} to \overline{xERRA} or \overline{xERRB}	1.4	6.7	—	6.5	1	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OEAB} or \overline{OEBA} to xBx, xBPAR or xAx, xAPAR	1.3	6.1	—	5.2	1.5	4.9	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{OEAB} or \overline{OEBA} to \overline{xERRA} or \overline{xERRB}	1.3	7.3	—	6.5	1	5.7	ns
t _{PHZ} t _{PLZ}	Output Disable Time \overline{SEL} to \overline{xERRA} or \overline{xERRB}	1.3	6.4	—	5.4	1.5	4.9	ns
tsu	Set-up Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR before CLK↑	1.9	—	2	—	1.7	—	ns
tsu	Set-up Time, HIGH or LOW, $\overline{xCLKENAB}$ or $\overline{xCLKENBA}$ before CLK↑	2.1	—	2.1	—	1.7	—	ns
tsu	Set-up Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR before LE↓	1.4	—	1.3	—	1.2	—	ns
t _H	Hold Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR after CLK↑	0.4	—	0.4	—	0.5	—	ns
t _H	Hold Time, HIGH or LOW, $\overline{xCLKENAB}$ or $\overline{xCLKENBA}$ after CLK↑	0.5	—	0.5	—	0.7	—	ns
t _H	Hold Time, HIGH or LOW, xAx, xAPAR or xBx, xBPAR after LE↓	0.9	—	1.1	—	0.9	—	ns
t _w	Pulse Width LEAB or LEBA HIGH	3	—	3	—	3	—	ns
t _w	Pulse Width CLKAB or CLKBA HIGH or LOW	3	—	3	—	3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

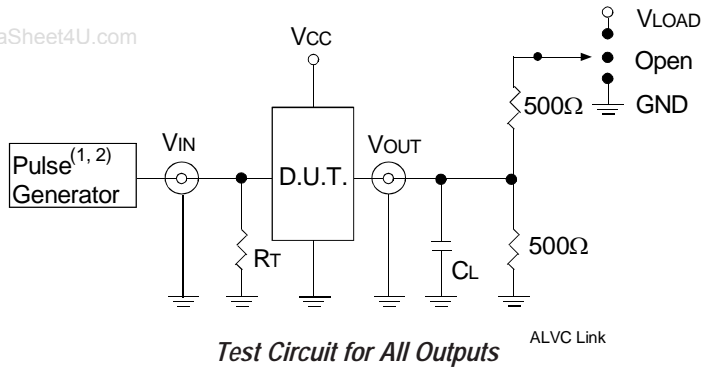
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T_A = - 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs ALVC Link

DEFINITIONS:

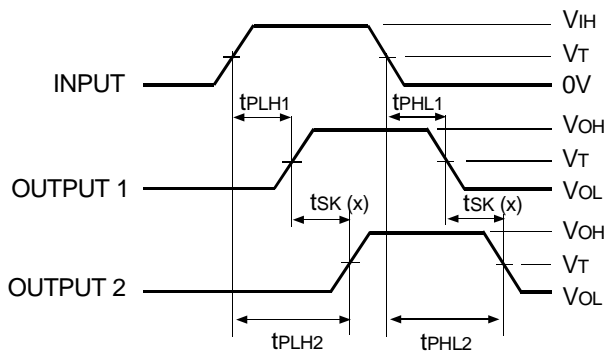
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

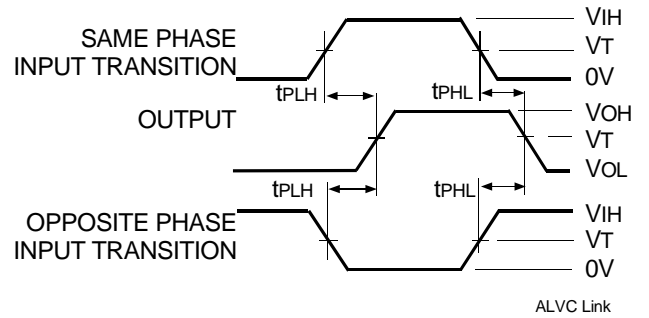


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

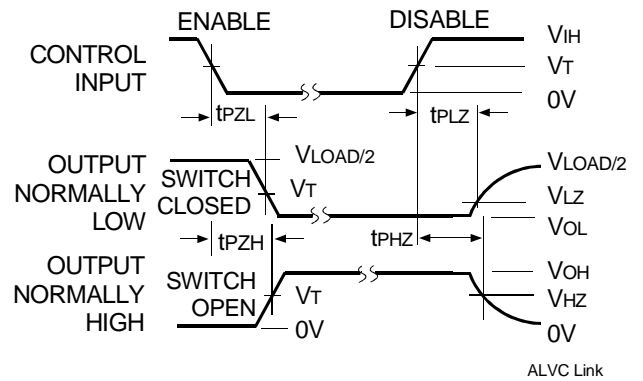
Output Skew - t_{SK}(x) ALVC Link

NOTES:

1. For t_{SK}(a) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



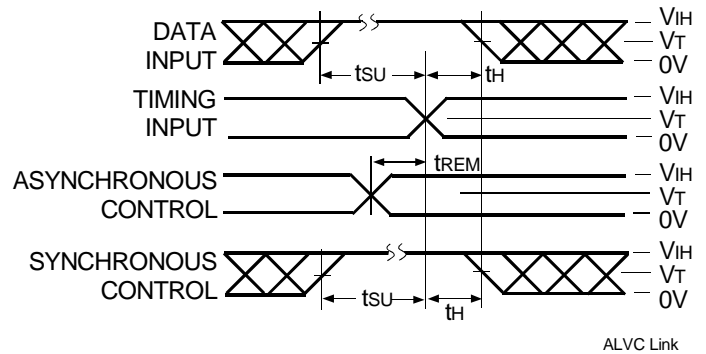
Propagation Delay ALVC Link



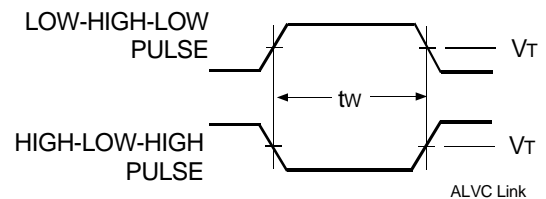
Enable and Disable Times ALVC Link

NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

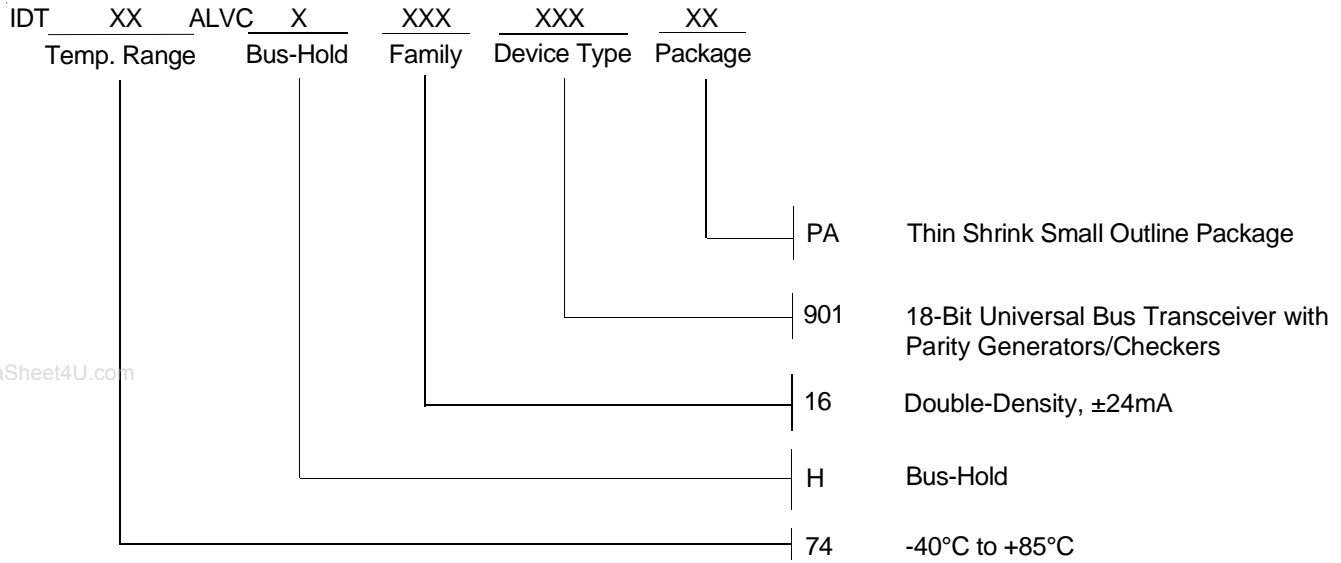


Set-up, Hold, and Release Times ALVC Link



Pulse Width ALVC Link

ORDERING INFORMATION



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