



Integrated Device Technology, Inc.

# FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161/A/C  
IDT54/74FCT163/A/C

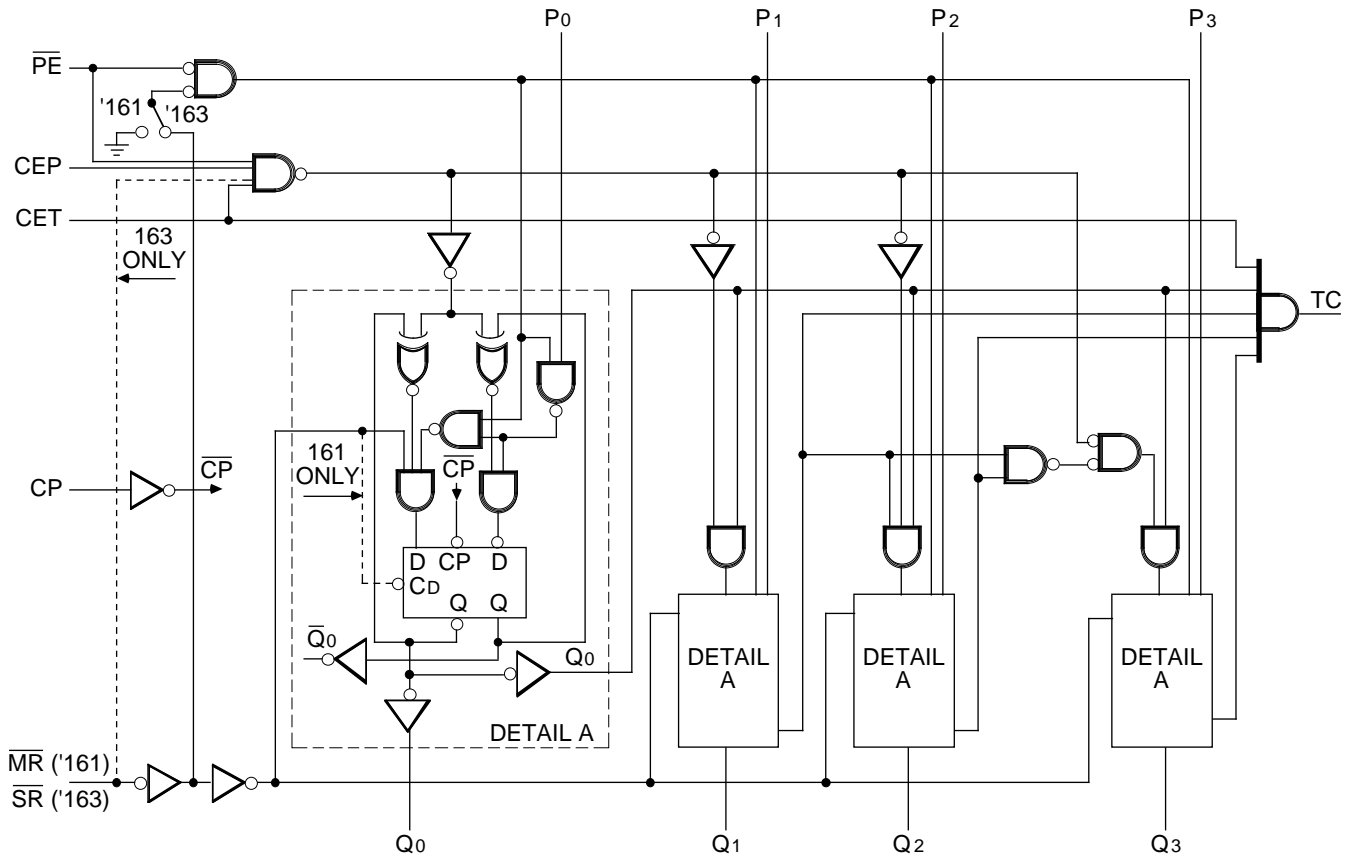
## FEATURES:

- IDT54/74FCT161/163 equivalent to FAST™ speed
- IDT54/74FCT161A/163A 35% faster than FAST
- IDT54/74FCT161A/163C 45% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT54/74FCT161/163, IDT54/74FCT161A/163A and IDT54/74FCT161C/163C are high-speed synchronous modulo-16 binary counters built using an advanced dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multistage counters. The IDT54/74FCT161/A/C have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163/A/C have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

## FUNCTIONAL BLOCK DIAGRAMS



2612 drw 01

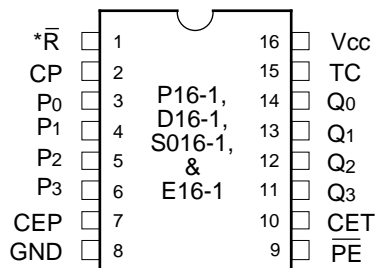
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MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

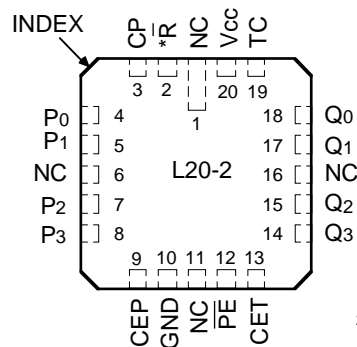
## PIN CONFIGURATIONS

### IDT54/74FCT861 10-BIT TRANSCEIVERS



DIP/SOIC/CERPACK  
 TOP VIEW

\*SR for '163  
 \*MR for '161



LCC  
 TOP VIEW  
 \*SR FOR '163

2612 drw 02

## PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
MR ('161)	Asynchronous Master Reset Input (Active LOW)
SR ('163)	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

2612 tbl 05

## FUNCTION TABLE<sup>(2)</sup>

SR <sup>(1)</sup>	PE	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (P <sub>n</sub> →Q <sub>n</sub> )
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

### NOTES:

- For FCT163/163A/163C only.
- H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

2612 tbl 06

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub>	-0.5 to V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

NOTES: 2612 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals only.
- Outputs and I/O terminals only.

### CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

NOTE: 2612 tbl 02  
1. This parameter is measured at characterization but not tested.

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Commercial: T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5.0V ± 5%; Military; T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit		
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L <sup>(5)</sup>	2.0V	—	—	V	
			MIL	3.0V	—	—	V	
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V		
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max.	V <sub>I</sub> = V <sub>CC</sub>	—	—	5	μA	
I <sub>IL</sub>	Input LOW Current		V <sub>I</sub> = 2.7V	—	—	5 <sup>(4)</sup>		
			V <sub>I</sub> = 0.5V	—	—	-5 <sup>(4)</sup>		
			V <sub>I</sub> = GND	—	—	-5		
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>N</sub> = -18mA	—	-0.7	-1.2	V		
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>O</sub> = GND	-60	-120	—	mA		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32μA	V <sub>HC</sub>	V <sub>CC</sub>	—	V		
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -300μA	V <sub>HC</sub>	V <sub>CC</sub>		—	
			I <sub>OH</sub> = -12mA MIL.	2.4	4.3		—	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub>	V		
			V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 300μA	—		GND	V <sub>LC</sub> <sup>(4)</sup>
				I <sub>OL</sub> = 32mA MIL.	—		0.3	0.5
				I <sub>OL</sub> = 48mA COM'L.	—		0.3	0.5

NOTES: 2612 tbl 03

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.
- Clock pin requires a minimum V<sub>IH</sub> of 2.7V.

**POWER SUPPLY CHARACTERISTICS**  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}$ ; $V_{IN} \leq V_{LC}$	—	0.2	1.5	mA	
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4V^{(3)}$	—	0.5	2.0	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Load Mode CEP = CET = $\overline{PE} = \text{GND}$ $\overline{MR}$ or $\overline{SR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle CEP = CET = $\overline{PE} = \text{GND}$ $\overline{MR}$ or $\overline{SR} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2.2	6.0		
		$V_{CC} = \text{Max.}$ , Outputs Open Load Mode $f_{CP} = 10\text{MHz}$ 50% Duty Cycle CEP = CET = $\overline{PE} = \text{GND}$ $\overline{MR}$ or $\overline{SR} = V_{CC}$ Four Bits Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8 <sup>(5)</sup>	
		$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.2	12.8 <sup>(5)</sup>		

**NOTES:**

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CCDHNT} + I_{CCD}(f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $DH = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } DH$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

2612 tbl 04

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT161/163				IDT54/74FCT161A/163A				IDT54/74FCT161C/163C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CP to Q <sub>n</sub> ( $\overline{PE}$ Input HIGH)	CL = 50pF RL = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to Q <sub>n</sub> ( $\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	2.0	7.4	2.0	8.3	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
tPHL	Propagation Delay MR to Q <sub>n</sub> ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	2.0	6.0	2.0	6.6	ns
tPHL	Propagation Delay MR to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	2.0	7.0	2.0	7.7	ns
tsu	Set-up Time, HIGH or LOW P <sub>n</sub> to CP		5.0	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
th	Hold Time, HIGH or LOW P <sub>n</sub> to CP		1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
tsu	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
th	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tsu	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	9.5	—	11.0	—	ns
th	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
tw	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	ns
tw	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns
tw	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	4.0 <sup>(3)</sup>	—	ns
tREM	Recovery Time MR to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

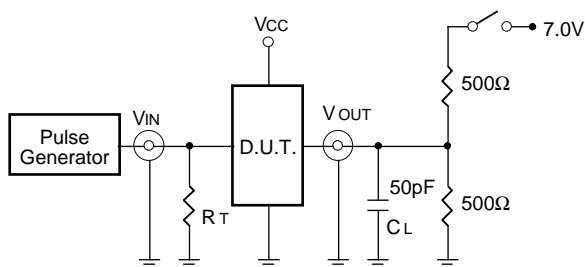
**NOTES:**

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2612 tbl 07

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

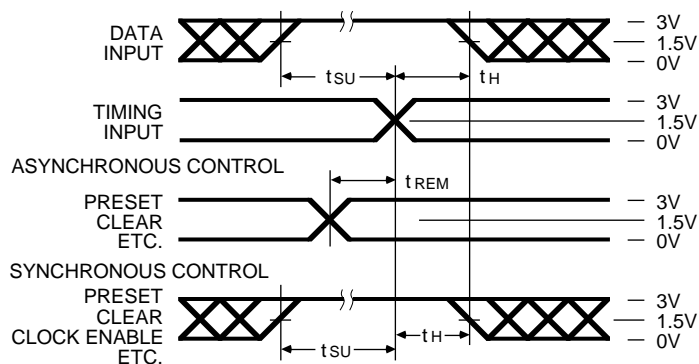
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

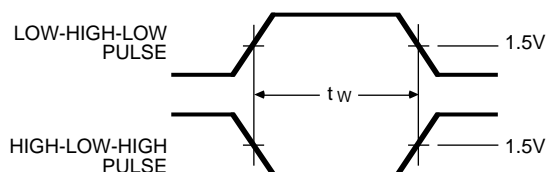
CL = Load capacitance: includes jig and probe capacitance.  
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2612 tbl 08

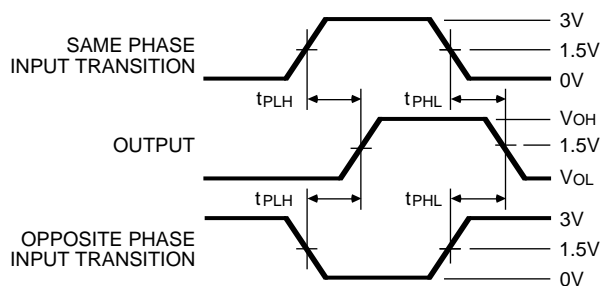
### SET-UP, HOLD AND RELEASE TIMES



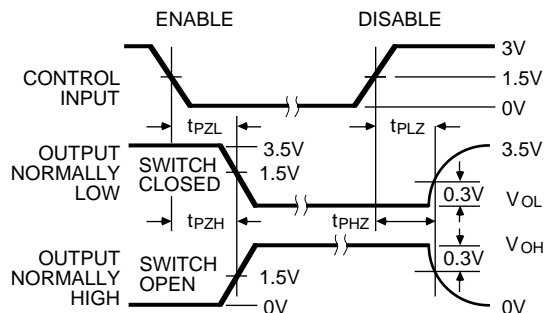
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

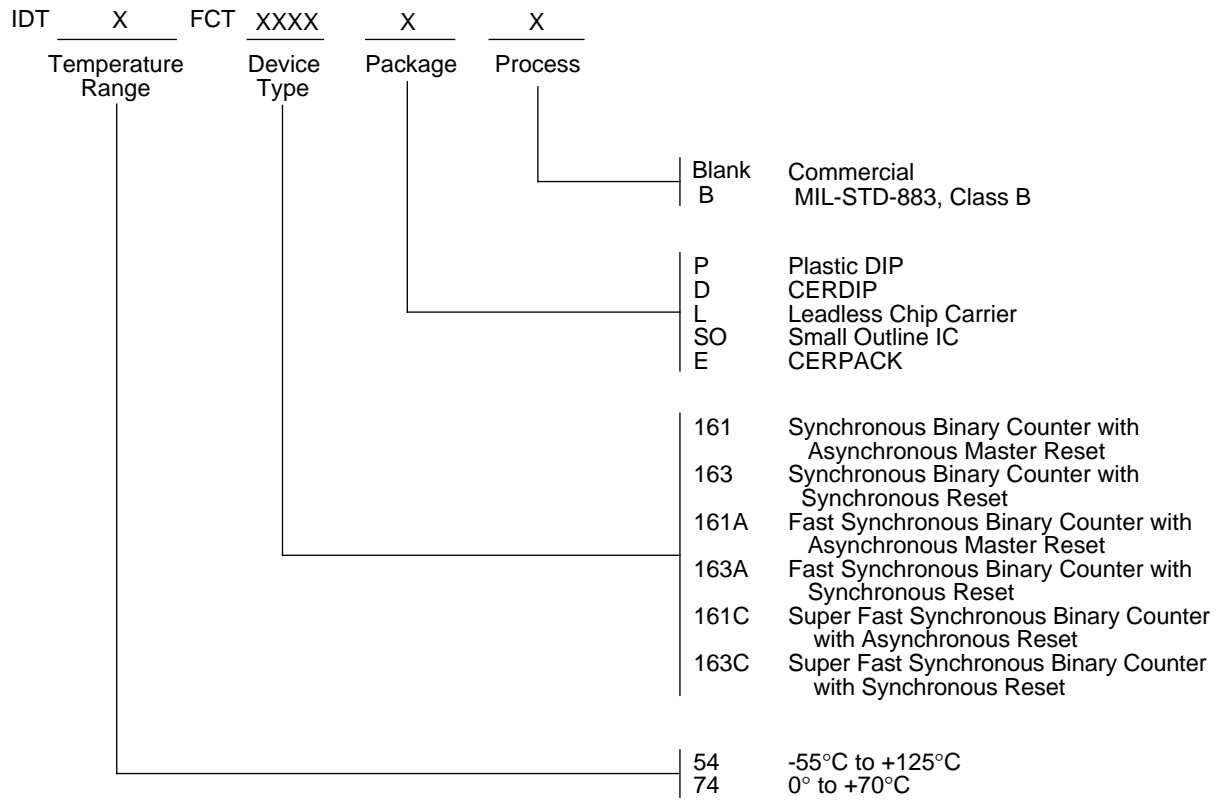


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_o \leq 50\Omega$ ;  $t_f \leq 2.5$ ns;  $t_r \leq 2.5$ ns.

2612 drw 04

**ORDERING INFORMATION**



2612 drw 03