FAST CMOS 20-BIT BUFFERS

IDT54/74FCT16827AT/BT/CT/ET
IDT54/74FCT162827AT/BT/CT/ET

Integrated Device Technology, Inc.

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical tsκ(o) (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - Packages include 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch Cerpack
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16827AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162827AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial),
                              ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
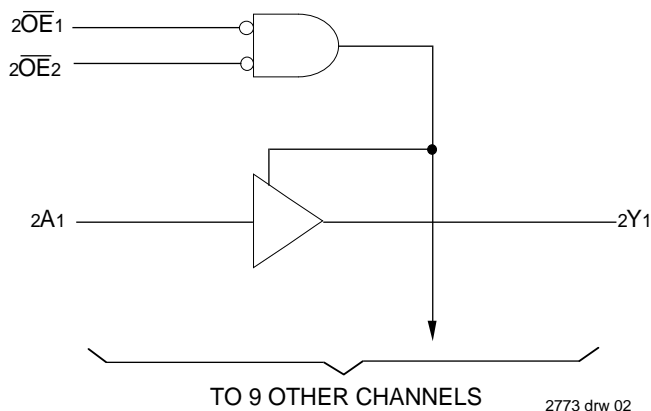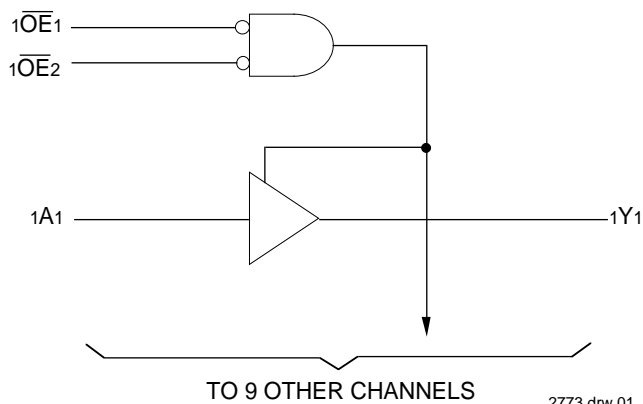
DESCRIPTION:

The FCT16827AT/BT/CT/ET and FCT162827AT/BT/CT/ET 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pair of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16827AT/BT/CT/ET are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162827AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162827AT/BT/CT/ET are plug-in replacements for the FCT16827AT/BT/CT/ET and ABT16827 for on-board interface applications.
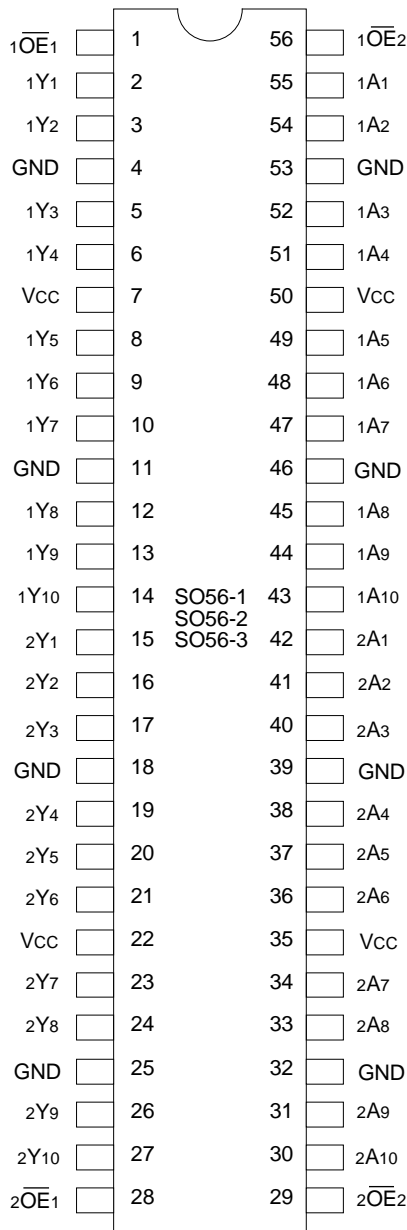
FUNCTIONAL BLOCK DIAGRAM

TO 9 OTHER CHANNELS   2773 drw 01

TO 9 OTHER CHANNELS   2773 drw 02

MILITARY AND COMMERCIAL TEMPERATURE RANGES   **AUGUST 1996**

PIN CONFIGURATIONS

	SSOP/TSSOP/TVSOP TOP VIEW	
1$\overline{OE}$1	1	56	1$\overline{OE}$2
1Y1	2	55	1A1
1Y2	3	54	1A2
GND	4	53	GND
1Y3	5	52	1A3
1Y4	6	51	1A4
Vcc	7	50	Vcc
1Y5	8	49	1A5
1Y6	9	48	1A6
1Y7	10	47	1A7
GND	11	46	GND
1Y8	12	45	1A8
1Y9	13	44	1A9
1Y10	14	43	1A10
2Y1	15	42	2A1
2Y2	16	41	2A2
2Y3	17	40	2A3
GND	18	39	GND
2Y4	19	38	2A4
2Y5	20	37	2A5
2Y6	21	36	2A6
Vcc	22	35	Vcc
2Y7	23	34	2A7
2Y8	24	33	2A8
GND	25	32	GND
2Y9	26	31	2A9
2Y10	27	30	2A10
2$\overline{OE}$1	28	29	2$\overline{OE}$2

SO56-1
SO56-2
SO56-3

**SSOP/
TSSOP/TVSOP
TOP VIEW**

2773 drw 03

E56-1

**CERPACK
TOP VIEW**

2773 drw 04

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$x	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2773 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max.	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
V$_{TERM}$[3]	Terminal Voltage with Respect to GND	−0.5 to V$_{CC}$ +0.5	V
T$_{STG}$	Storage Temperature	−65 to +150	°C
I$_{OUT}$	DC Output Current	−60 to +120	mA

2773 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE[1]

Inputs			Outputs
x$\overline{OE}$1	x$\overline{OE}$2	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

2773 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

CAPACITANCE (T$_A$ = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 0V	3.5	6.0	pF
C$_{OUT}$	Output Capacitance	V$_{OUT}$ = 0V	3.5	8.0	pF

2773 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2773 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2773 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2773 lnk 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1 = x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	—	60	100	μA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle $x\overline{OE}_1 = x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	—	3.0	5.5[5]	
		50% Duty Cycle $x\overline{OE}_1 = x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2773 tbl 08

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

N_{CP} = Number of Clock Inputs at f_{CP}

f_i = Input Frequency

N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16827AT/162827AT				FCT16827BT/162827BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
t_{PZH} t_{PZL}	Output Enable Time xOEx to xYx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time xOEx to xYx	C_L = 5pF[4] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2773 tbl 09

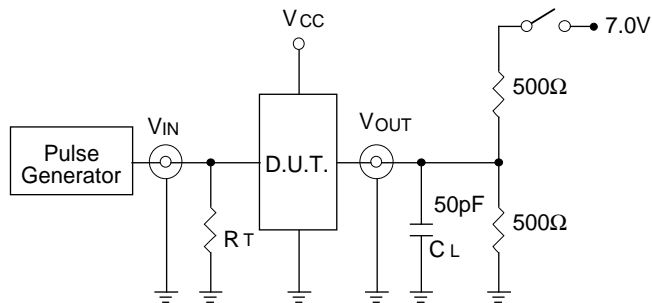| Symbol	Parameter	Condition[1]	FCT16827CT/162827CT				FCT16827ET/162827ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	4.4	1.5	5.0	1.5	3.2	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	10.0	1.5	11.0	1.5	7.0	—	—	
t_{PZH} t_{PZL}	Output Enable Time xOEx to xYx	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time xOEx to xYx	C_L = 5pF[4] R_L = 500Ω	1.5	5.7	1.5	6.7	1.5	4.0	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	4.0	—	—	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2773 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

VCC

7.0V

500Ω

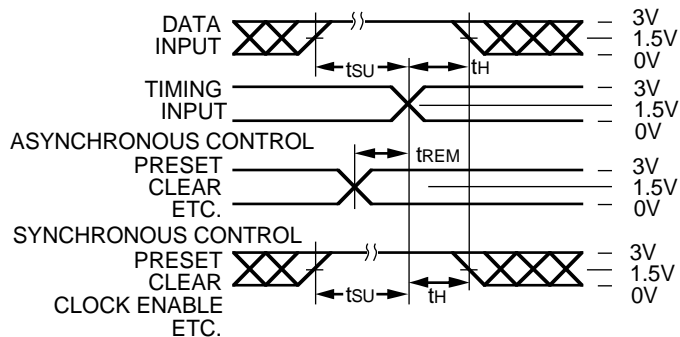Pulse Generator

V_{IN}

D.U.T.

V_{OUT}

R_T

50pF

C_L

500Ω

2773 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2773 lnk 11

DEFINITIONS:
C_L= Load capacitance: includes jig and probe capacitance.
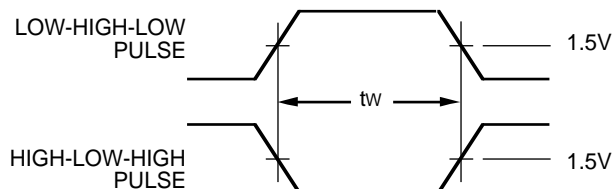R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.
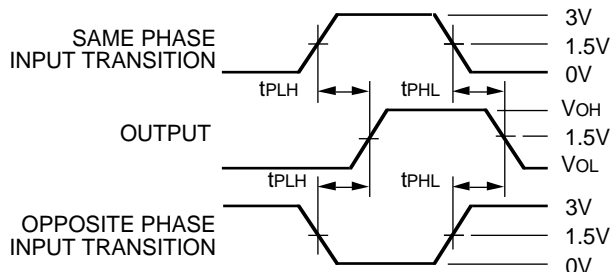
SET-UP, HOLD AND RELEASE TIMES

DATA INPUT — 3V / 1.5V / 0V

t_{SU} t_H

TIMING INPUT — 3V / 1.5V / 0V

ASYNCHRONOUS CONTROL PRESET CLEAR ETC. — t_{REM} — 3V / 1.5V / 0V

SYNCHRONOUS CONTROL PRESET CLEAR CLOCK ENABLE ETC. — t_{SU} t_H — 3V / 1.5V / 0V

2773 drw 06

PULSE WIDTH

LOW-HIGH-LOW PULSE — 1.5V

t_W

HIGH-LOW-HIGH PULSE — 1.5V

2773 drw 07

PROPAGATION DELAY

SAME PHASE INPUT TRANSITION — 3V / 1.5V / 0V

t_{PLH} t_{PHL}

OUTPUT — V_{OH} / 1.5V / V_{OL}

t_{PLH} t_{PHL}

OPPOSITE PHASE INPUT TRANSITION — 3V / 1.5V / 0V

2773 drw 08

ENABLE AND DISABLE TIMES

ENABLE   DISABLE

CONTROL INPUT — 3V / 1.5V / 0V

t_{PZL} t_{PLZ}

OUTPUT NORMALLY LOW — SWITCH CLOSED — 3.5V / 1.5V

OUTPUT NORMALLY HIGH — SWITCH OPEN — 1.5V / 0V

t_{PZH} t_{PHZ}

0.3V — V_{OL}

0.3V — V_{OH}

2773 drw 09

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION

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IDT     XX     FCT    XXXX        X         X
      Temp. Range    Device Type  Package   Process
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Blank	Commercial
B	MIL-STD-883, Class B
PV	Shrink Small Outline Package (SO56-1)
PA	Thin Shrink Small Outline Package (SO56-2)
PF	Thin Very Small Outline Package (SO56-3)
E	CERPACK (E56-1)
16827AT	Non-Inverting 20-Bit Buffers
16827BT	
16827CT	
16827ET	
162827AT	
162827BT	
162827CT	
162827ET	
54	−55°C to +125°C
74	−40°C to +85°C

2773 drw 10

5.17   **8**