



Integrated Device Technology, Inc.

# FAST CMOS UP/DOWN BINARY COUNTERS

IDT54/74FCT193  
IDT54/74FCT193A

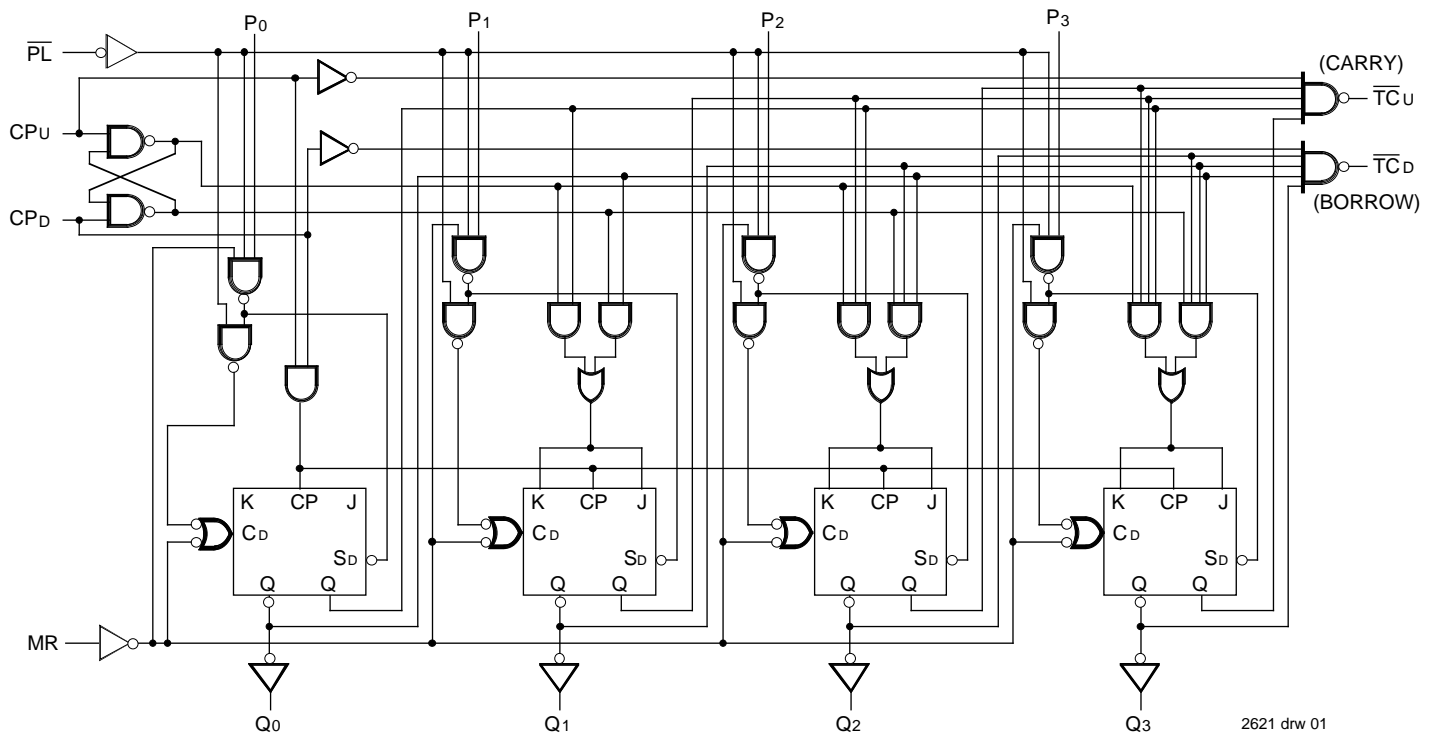
## FEATURES:

- IDT54/74FCT193 equivalent to FAST™ speed
- **IDT54/74FCT193A 35% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Substantially lower input current levels than FAST (5µA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT54/74FCT193 and IDT54/74FCT193A are up/down modulo-16 binary counters built using an advanced dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multiusage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ( $\overline{PL}$ ) and the Master Reset (MR) inputs asynchronously override the clocks.

## FUNCTIONAL BLOCK DIAGRAM

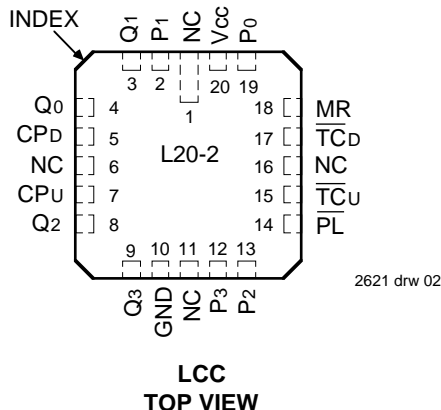
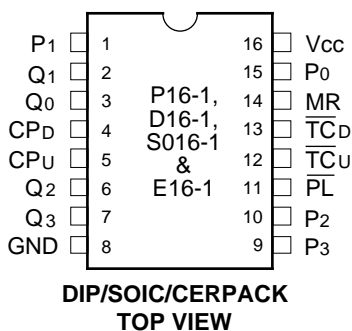


The IDT logo is a registered trademark of Integrated Device Technology, Inc.  
FAST is a trademark of National Semiconductor Co.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

## PIN CONFIGURATIONS



## PIN DESCRIPTION

Pin Names	Description
CPU	Count Up Clock Input (Active Rising Edge)
CPD	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P <sub>n</sub>	Parallel Data Inputs
Q <sub>n</sub>	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

2621 tbl 05

## FUNCTION TABLE<sup>(1)</sup>

MR	$\overline{PL}$	CPU	CPD	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

**NOTE:**

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
↑ = LOW-to-HIGH Clock Transition.

2621 tbl 06

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>cc</sub>	-0.5 to V <sub>cc</sub>	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

**NOTES:**

2621 tbl 01

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>cc</sub> by +0.5V unless otherwise noted.
- Input and V<sub>cc</sub> terminals.
- Output and I/O terminals.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

- This parameter is guaranteed by characterization data and not tested.

2621 tbl 02

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Commercial:  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$ ; Military:  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		COM'L <sup>(5)</sup>	2.0V	—	—	V
				MIL	3.0V	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	—	5	$\mu A$	
			$V_I = 2.7V$	—	—	5 <sup>(4)</sup>		
$I_{IL}$	Input LOW Current		$V_I = 0.5V$	—	—	-5 <sup>(4)</sup>		
			$V_I = GND$	—	—	-5		
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$		—	-0.7	-1.2	V	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = GND$		-60	-120	—	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$		$V_{HC}$	$V_{CC}$	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	$V_{HC}$	$V_{CC}$	—		
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3	—		
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3	—		
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$		—	GND	$V_{LC}$	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND	$V_{LC}^{(4)}$		
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3	0.5		
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3	0.5		

### NOTES:

2621 tbl 03

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.
- Clock pin requires a minimum  $V_{IH}$  of 2.7V.

## POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.2	1.5	mA	
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max., V <sub>IN</sub> = 3.4V <sup>(3)</sup>	—	0.5	2.0	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open Preset Mode $\overline{P_L} = \overline{M_R} = C_{P_U} = C_{P_D} = GND$ One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open Preset Mode $\overline{P_L} = \overline{M_R} = C_{P_U} = C_{P_D} = GND$ One Bit Toggling at f <sub>i</sub> = 10MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.0	5.0	
		V <sub>CC</sub> = Max. Outputs Open Preset Mode $\overline{P_L} = \overline{M_R} = C_{P_U} = C_{P_D} = GND$ Four Bits Toggling at f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	3.2	6.5 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	4.2	10.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

2621 tbl 04

### SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT193				IDT54/74FCT193A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CPU or CPD to $\overline{TCU}$ or $\overline{TCd}$	CL = 50pF RL = 500Ω	2.0	10.0	2.0	10.5	2.0	6.5	2.0	6.9	ns
tPLH tPHL	Propagation Delay CPU or CPD to Qn		2.0	13.5	2.0	14.0	2.0	8.8	2.0	9.1	ns
tPLH tPHL	Propagation Delay Pn to Qn		2.0	15.5	2.0	16.5	2.0	10.1	2.0	10.8	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to Qn		2.0	14.0	2.0	13.5	2.0	8.8	2.0	9.1	ns
tPHL	Propagation Delay MR to Qn		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
tPLH	Propagation Delay MR to $\overline{TCU}$		3.0	14.5	3.0	15.0	3.0	9.4	3.0	9.8	ns
tPHL	Propagation Delay MR to $\overline{TCd}$		3.0	15.5	3.0	16.0	3.0	10.1	3.0	10.4	ns
tPLH tPHL	Propagation Delay $\overline{PL}$ to $\overline{TCU}$ or $\overline{TCd}$		3.0	16.5	3.0	18.5	3.0	10.8	3.0	12.0	ns
tPLH tPHL	Propagation Delay Pn to $\overline{TCU}$ or $\overline{TCd}$		3.0	15.5	3.0	16.5	3.0	10.1	3.0	10.8	ns
tsu	Set-up Time, HIGH or LOW Pn to $\overline{PL}$		5.0	—	6.0	—	4.0	—	5.0	—	ns
th	Hold Time, HIGH or LOW Pn to $\overline{PL}$		2.0	—	2.0	—	1.5	—	1.5	—	ns
tw	$\overline{PL}$ Pulse Width, LOW		6.0	—	7.5	—	5.0	—	6.5	—	ns
tw	CPU or CPD Pulse Width HIGH or LOW		5.0	—	7.0	—	4.0 <sup>(3)</sup>	—	6.0	—	ns
tw	CPU or CPD Pulse Width LOW (Change of Direction)		10.0	—	12.0	—	8.0	—	10.0	—	ns
tw	MR Pulse Width HIGH		6.0	—	6.0	—	5.0	—	5.0	—	ns
tREM	Recovery Time $\overline{PL}$ to CPU or CPD		6.0	—	8.0	—	5.0	—	7.0	—	ns
tREM	Recovery Time MR to CPU or CPD	4.0	—	4.5	—	3.0	—	3.5	—	ns	

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

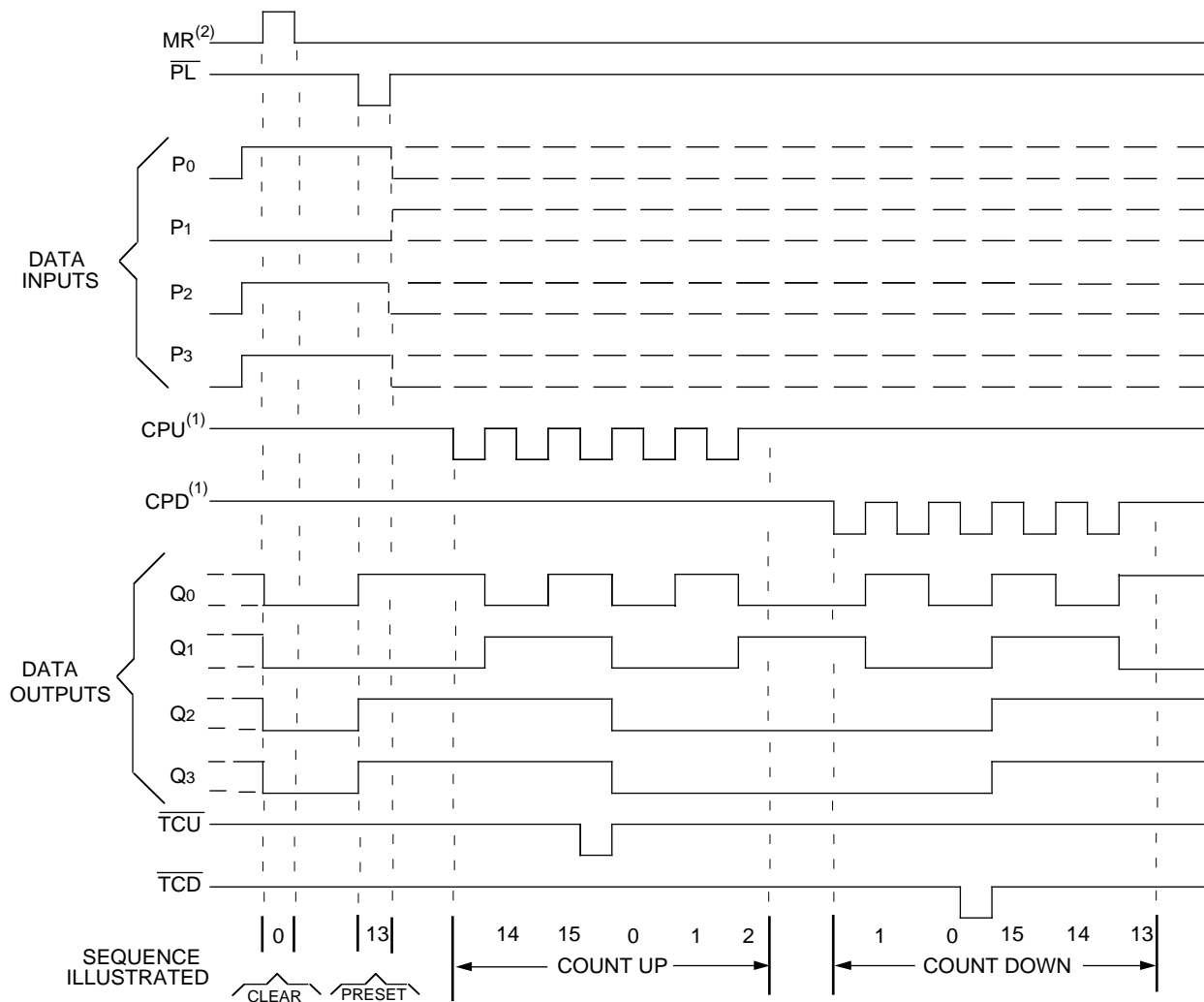
2621 tbl 07

## TIMING WAVEFORMS

### Typical clear, load, and count sequences

Illustrated below is the following sequence:

- Clear outputs to zero
- Load (preset) to binary thirteen
- Count up to fourteen, fifteen, carry zero, one and two
- Count down to one, zero, borrow, fifteen, fourteen and thirteen



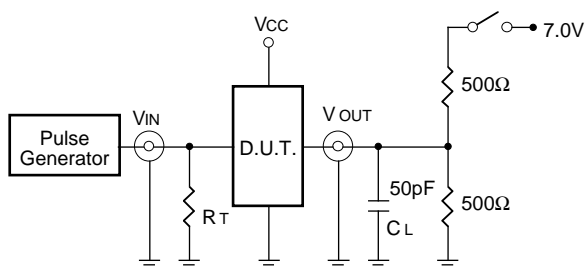
2621 drw 03

#### NOTES:

1. MR overrides load, data, and count inputs
2. When counting up, CPD input must be HIGH; when counting down, CPU input must be HIGH.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

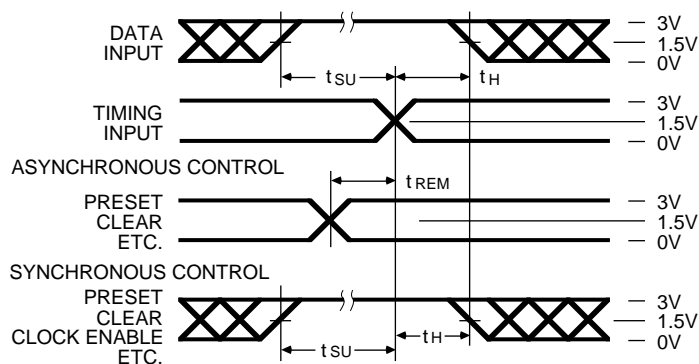
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

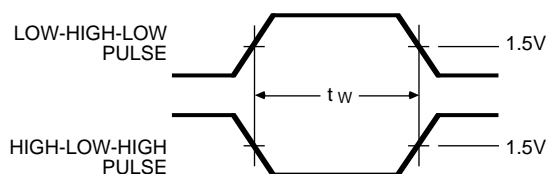
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

2621 tbl 09

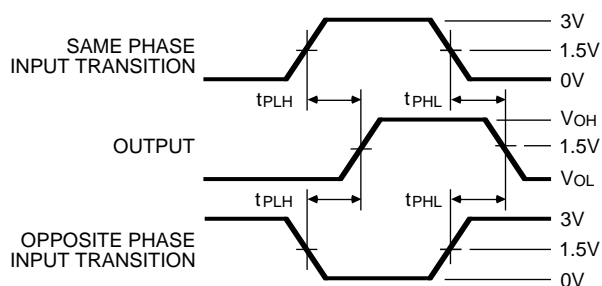
### SET-UP, HOLD AND RELEASE TIMES



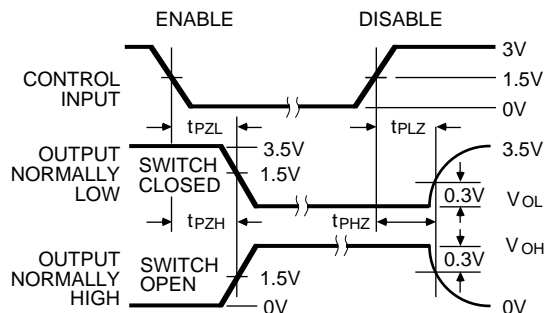
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

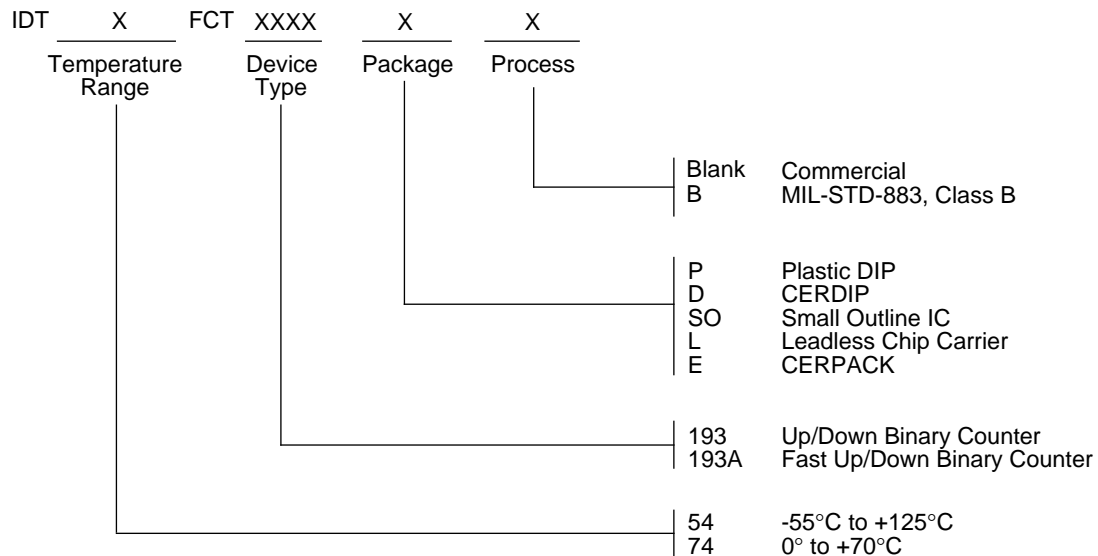


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_o \leq 50\Omega$ ;  $t_f \leq 2.5$  ns;  $t_r \leq 2.5$  ns.

2621 drw 04

**ORDERING INFORMATION**



2621 drw 03