

Integrated Device Technology, Inc.

# FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

**IDT54/74FCT377**  
**IDT54/74FCT377A**  
**IDT54/74FCT377C**

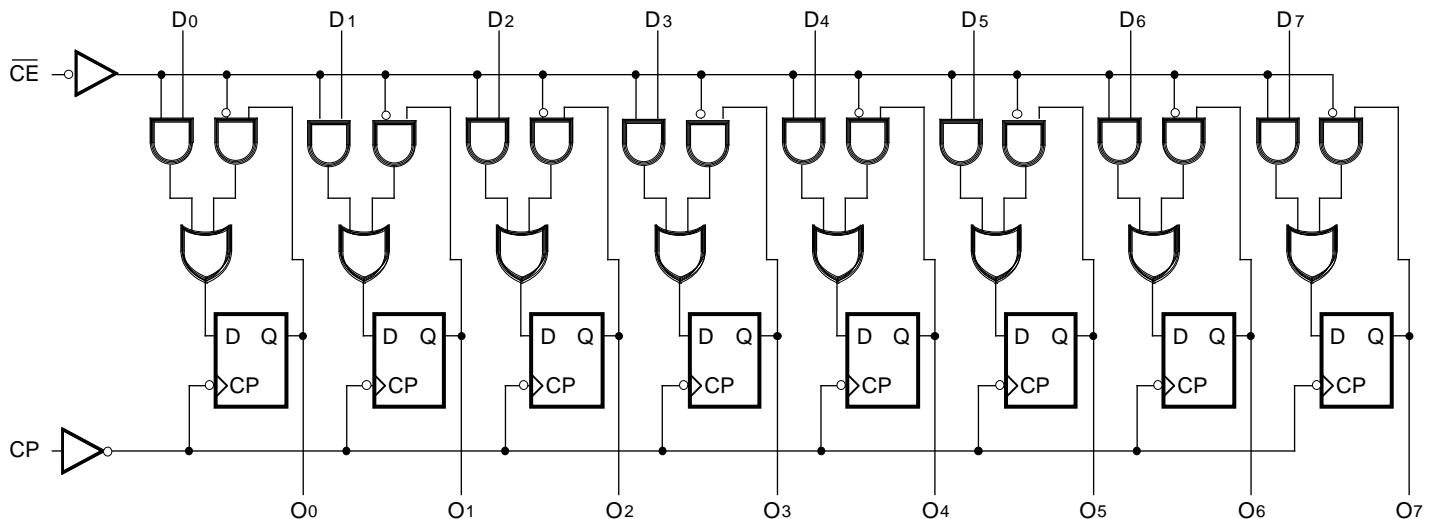
## FEATURES:

- IDT54/74FCT377 equivalent to FAST™ speed
- IDT54/74FCT377A 25% faster than FAST
- IDT54/74FCT377C 40% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial) and 32mA (military)
- IiH and IiL only 5µA max.
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Meets or exceeds JEDEC Standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

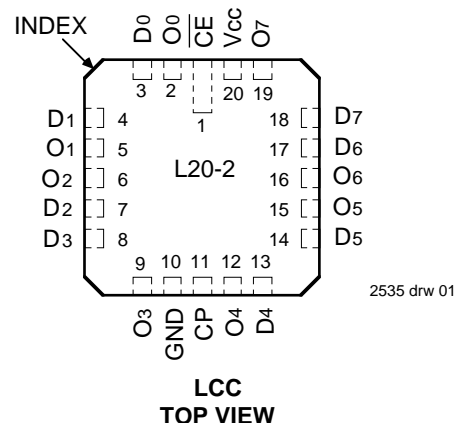
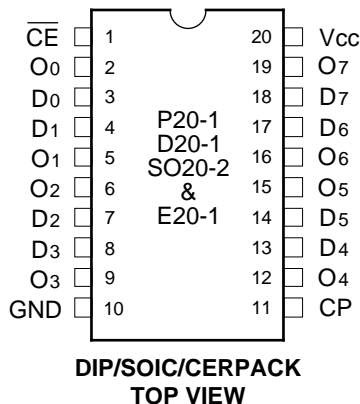
The IDT54/74FCT377/A/C is an octal D flip-flop built using an advanced dual metal CMOS technology. The IDT54/74FCT377/A/C have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ( $\overline{CE}$ ) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The  $\overline{CE}$  input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATIONS

2535 drw 02



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FAST is a trademark of National Semiconductor Co.

## MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1992

## PIN DESCRIPTION

Pin Names	Description
D0–D7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
O0–O7	Data Outputs
CP	Clock Pulse Input

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## FUNCTION TABLE<sup>(1)</sup>

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load “1”	↑	l	h	H
Load “0”	↑	l	l	L
Hold (Do Nothing)	↑ H	h H	X X	No Change No Change

**NOTE:**

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- H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock Transition  
L = LOW voltage level  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition  
X = Immaterial  
↑ = LOW-to-HIGH clock transition

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Commercial	Military	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	–0.5 to Vcc	–0.5 to Vcc	V
T <sub>A</sub>	Operating Temperature	0 to +70	–55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	–55 to +125	–65 to +135	°C
T <sub>STG</sub>	Storage Temperature	–55 to +125	–65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

**NOTES:**

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
- Input and Vcc terminals only.
- Outputs and I/O terminals only.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

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- This parameter is guaranteed but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Commercial:  $T_A = 0^\circ C$  to  $+70^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$ ; Military:  $T_A = -55^\circ C$  to  $+125^\circ C$ ,  $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$ $V_i = V_{CC}$ $V_i = 2.7V$ $V_i = 0.5V$ $V_i = \text{GND}$	—	—	5	$\mu A$	
$I_{IL}$	Input LOW Current		—	—	$5^{(4)}$		
			—	—	$-5^{(4)}$		
			—	—	-5		
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_N = -18mA$	—	-0.7	-1.2	V	
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}^{(3)}, V_O = \text{GND}$	-60	-120	—	mA	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OH} = -32\mu A$	$V_{HC}$	$V_{CC}$	—	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -300\mu A$	$V_{HC}$	$V_{CC}$		—
			$I_{OH} = -12mA \text{ MIL.}$	2.4	4.3		—
			$I_{OH} = -15mA \text{ COM'L.}$	2.4	4.3		—
$V_{OL}$	Output LOW Voltage	$V_{CC} = 3V, V_{IN} = V_{LC} \text{ or } V_{HC}, I_{OL} = 300\mu A$	—	GND	$V_{LC}$	V	
		$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 300\mu A$	—	GND		$V_{LC}^{(4)}$
			$I_{OL} = 32mA \text{ MIL.}$	—	0.3		0.5
			$I_{OL} = 48mA \text{ COM'L.}$	—	0.3		0.5

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

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## POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>HC</sub> ; V <sub>IN</sub> ≤ V <sub>LC</sub>		—	0.2	1.5	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max. V <sub>IN</sub> = 3.4V <sup>(3)</sup>		—	0.5	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup>	V <sub>CC</sub> = Max. Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub>	—	0.15	0.25	mA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{CE}$ = GND One Bit Toggling at f <sub>i</sub> = 5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	1.7	4.0	mA
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	2.2	6.0	
		V <sub>CC</sub> = Max. Outputs Open f <sub>CP</sub> = 10MHz 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f <sub>i</sub> = 2.5MHz 50% Duty Cycle	V <sub>IN</sub> ≥ V <sub>HC</sub> V <sub>IN</sub> ≤ V <sub>LC</sub> (FCT)	—	4.0	7.8 <sup>(5)</sup>	
			V <sub>IN</sub> = 3.4V V <sub>IN</sub> = GND	—	6.2	16.8 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

2535 tbl 06

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Condition <sup>(1)</sup>	IDT54/74FCT377				IDT54/74FCT377A				IDT54/74FCT377C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH tPHL	Propagation Delay CP to On	CL = 50pF RL = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.2	2.0	5.5	ns
tsu	Set-up Time HIGH or LOW Dn to CP		2.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW Dn to CP		2.0	—	2.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tsu	Set-up Time HIGH or LOW CE to CP		4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns
th	Hold Time HIGH or LOW CE to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tw	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns

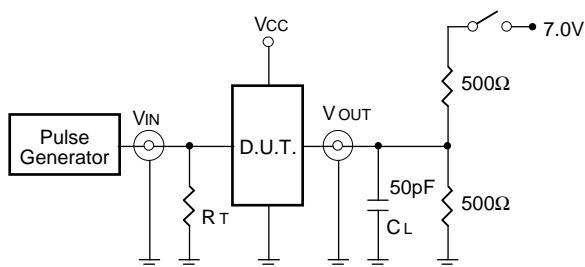
**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

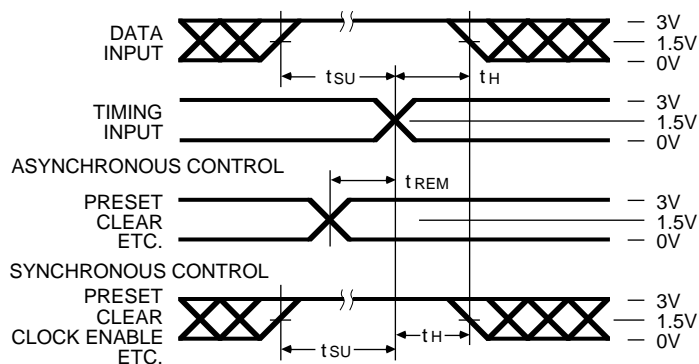
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

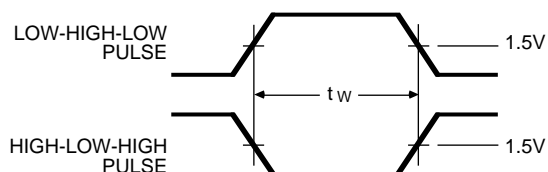
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

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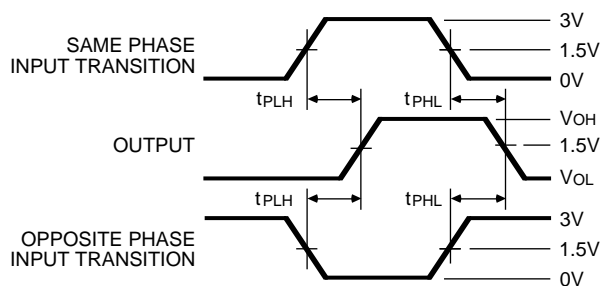
### SET-UP, HOLD AND RELEASE TIMES



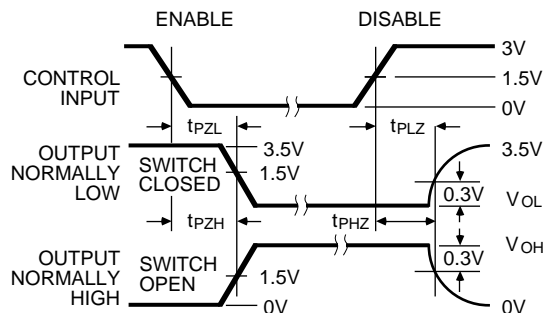
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

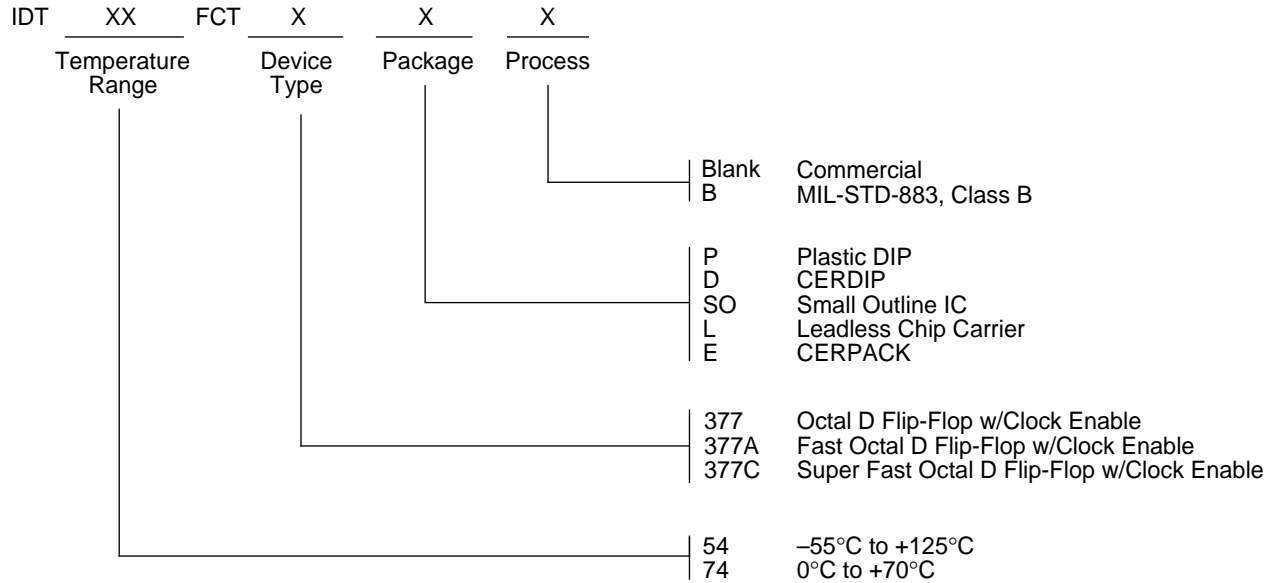


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_o \leq 50\Omega$ ;  $t_f \leq 2.5$  ns;  $t_r \leq 2.5$  ns.

2535 drw 04

**ORDERING INFORMATION**



2535 drw 03