FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543/A/C

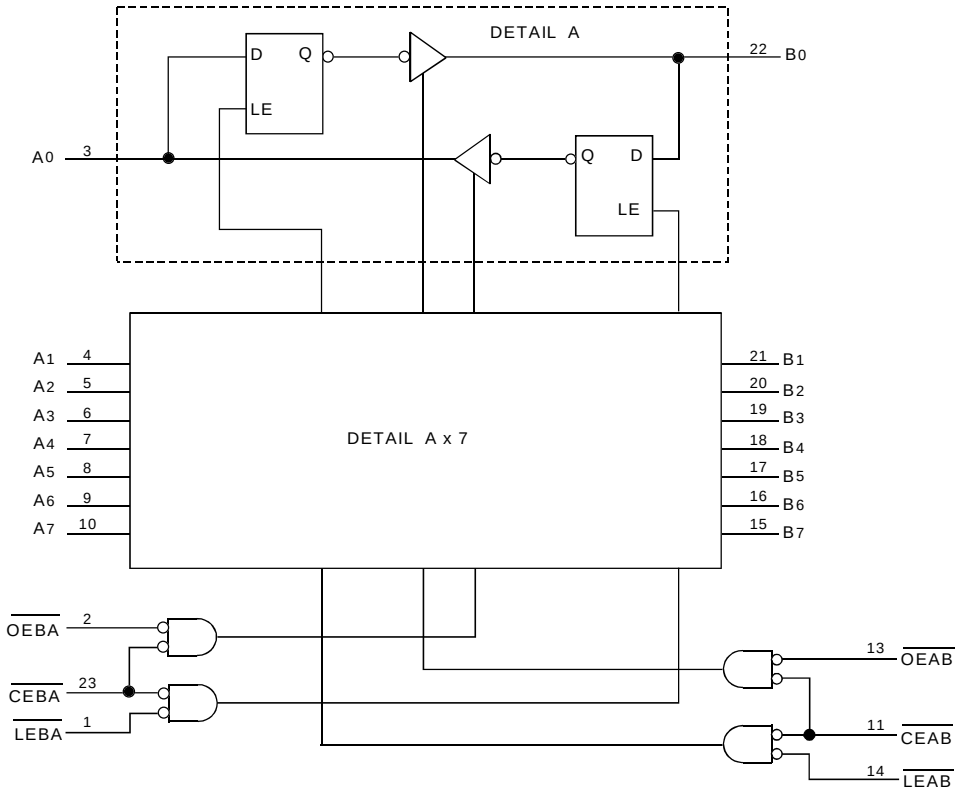
FEATURES:

- IDT54/74FCT543 equivalent to FAST™ speed
- IDT54/74FCT543A 25% faster than FAST
- IDT54/74FCT543C 40% faster than FAST
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- I_{OL} = 64mA (commercial), 48mA (military)
- Separate controls for data flow in each direction
- Back-to-back latches for storage
- CMOS power levels (1mW typ. static)
- Substantially lower input current levels than FAST (5µA max.)
- TTL input and output level compatible
- CMOS output level compatible
- Military product compliant to MIL-STD-883, Class B
- Available in the following packages:
  - Commercial: SOIC
  - Military: CERDIP, LCC, CERPACK

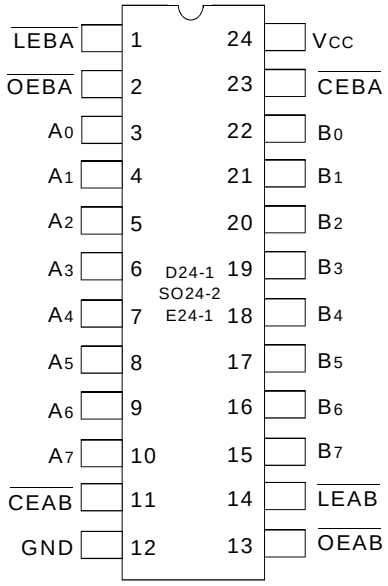
DESCRIPTION:

The FCT543 is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. These devices contain two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ low, a low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

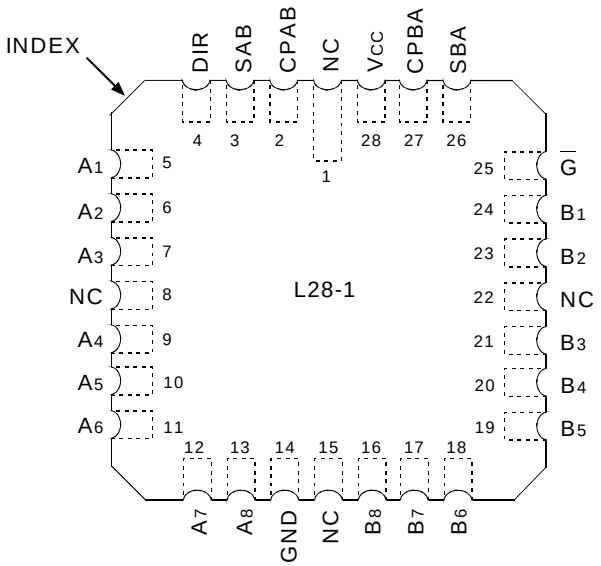
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC/ CERPACK
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

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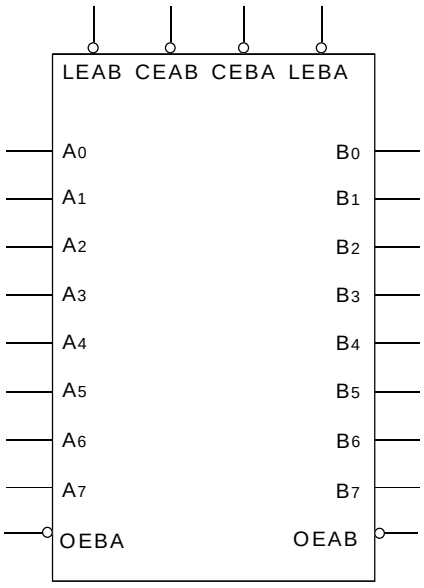
NOTE:
1. This parameter is measured at characterization but not tested.

LOGIC SYMBOL



PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE (1,2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0–B_7
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
			V_I = 2.7V	—	—	5[4]	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	—	—	–5[4]	µA
			V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current (I/O pins Only)	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
			V_I = 2.7V	—	—	15[4]	
I_{IL}	Input LOW Current (I/O pins Only)		V_I = 0.5V	—	—	–15[4]	µA
			V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA	V_{HC}[4]	V_{CC}	—	
			I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	—	GND	V_{LC}[4]	
			I_{OL} = 48mA MIL.[5]	—	0.3	0.55	
			I_{OL} = 64mA COM'L.[5]	—	0.3	0.55	

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	7	12.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	9.2	21.8[5]	

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

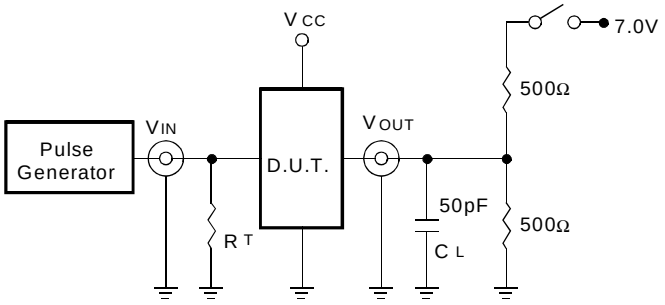
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT543				IDT54/74FCT543A				IDT54/74FCT543C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	C_L = 50pF R_L = 500Ω	2.5	8.5	2.5	10	2.5	6.5	2.5	7.5	2.5	5.3	2.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n, $\overline{LEAB}$ to B_n		2.5	12.5	2.5	14	2.5	8	2.5	9	2.5	7	2.5	8	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		2	12	2	14	2	9	2	10	2	8	2	9	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		2	9	2	13	2	7.5	2	8.5	2	6.5	2	7.5	ns
t_{SU}	Set-up Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		3	—	3	—	2	—	2	—	2	—	2	—	ns
t_H	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		2	—	2	—	2	—	2	—	2	—	2	—	ns
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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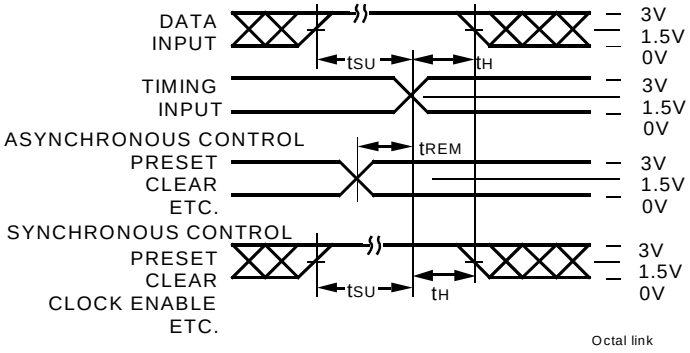
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD, AND RELEASE TIMES



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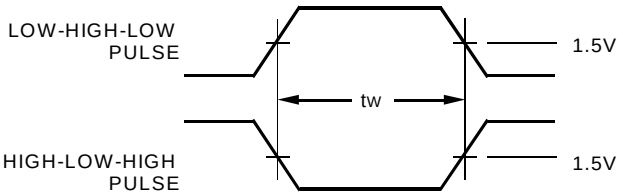
PULSE WIDTH



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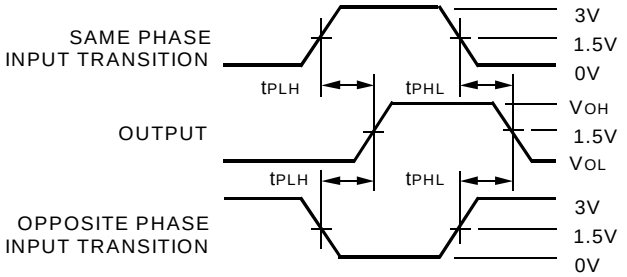
PROPAGATION DELAY



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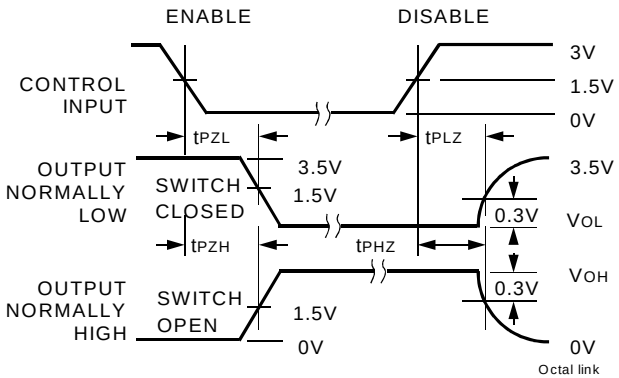
ENABLE AND DISABLE TIMES



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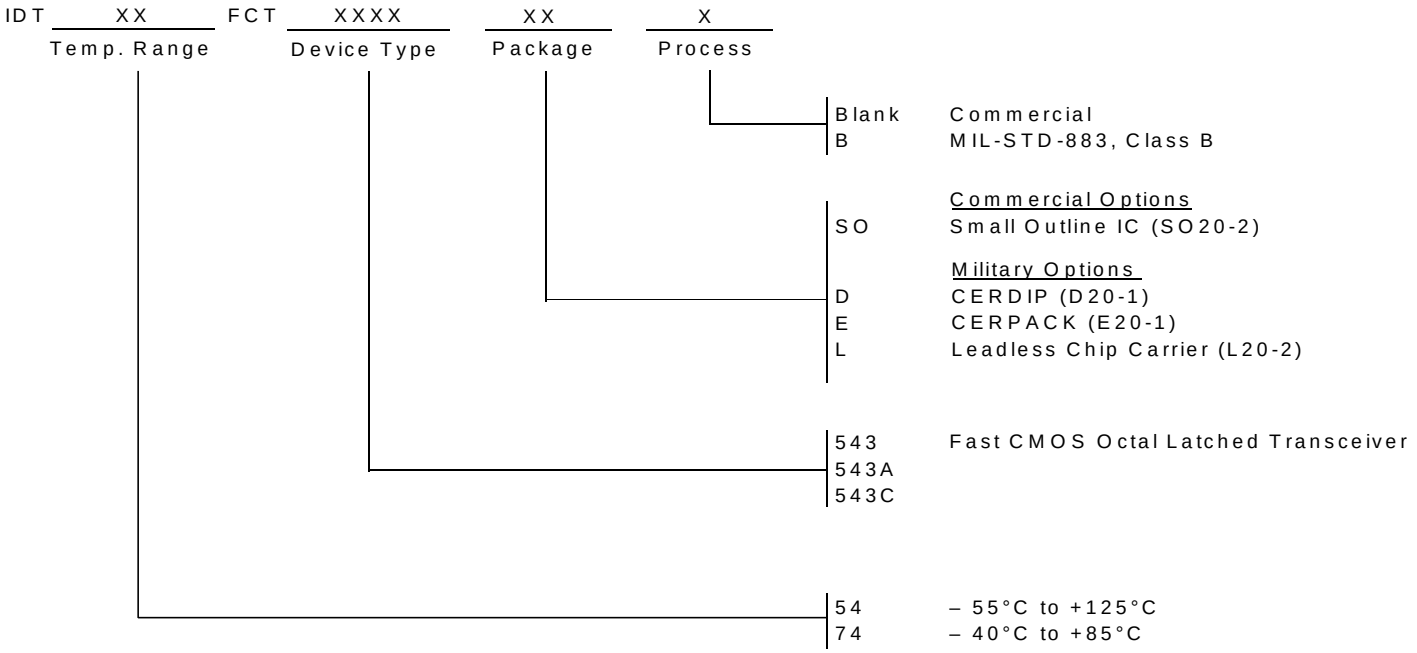
NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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