DATASHEET

28-BIT 1:2 REGISTERED BUFFER WITH PARITY

IDT74SSTUBF32865A

Description

This 28-bit 1:2 registered buffer with parity is designed for 1.7V to 1.9V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load. The IDT74SSTUBF32865A operates from a differential clock (CLK and $\overline{\text{CLK}}$). Data are registered at the crossing of CLK going high, and $\overline{\text{CLK}}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{\text{RESET}}$) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs except $\overline{\text{PTYERR}}$ are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CLK and $\overline{\text{CLK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the IDT74SSTUBF32865A must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs and will gate the Qn outputs from changing states when both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ are high. If either $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. The $\overline{\text{RESET}}$ input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and will force the Qn outputs low and the $\overline{\text{PTYERR}}$ output high. If the DCS-control functionality is not desired, then the CSGateEnable input can be hardwired to ground, in which case, the setup-time requirement for DCS would be the same as for the other D data inputs.

The IDT74SSTUBF32865A includes a parity checking function. The IDT74SSTUBF32865A accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{\text{PTYERR}}$ pin (active LOW).

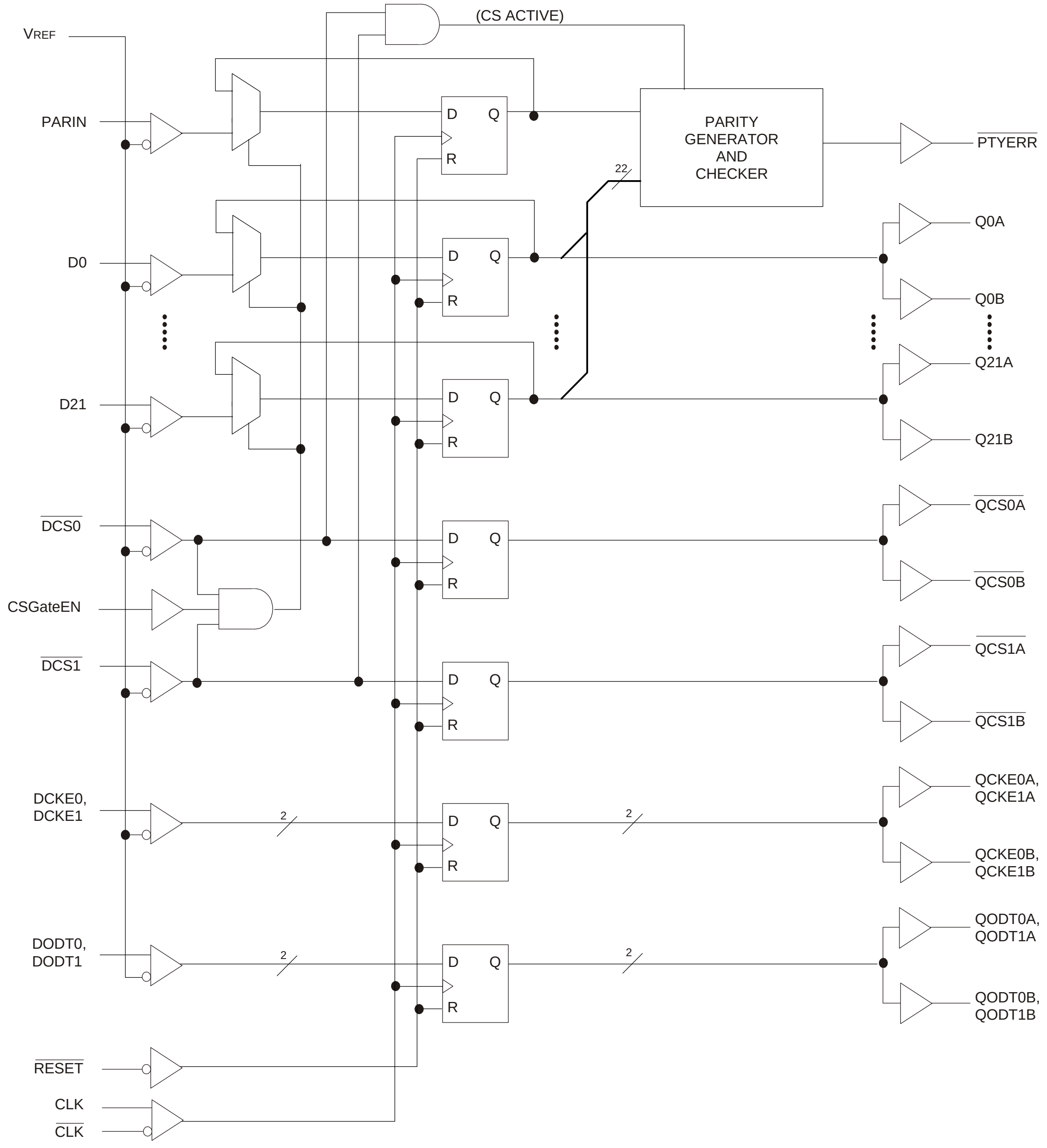
Features

- 28-bit 1:2 registered buffer with parity check functionality
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on CSGateEN and $\overline{\text{RESET}}$ inputs
- Low voltage operation: V_{DD} = 1.7V to 1.9V
- Available in 160-ball LFBGA package

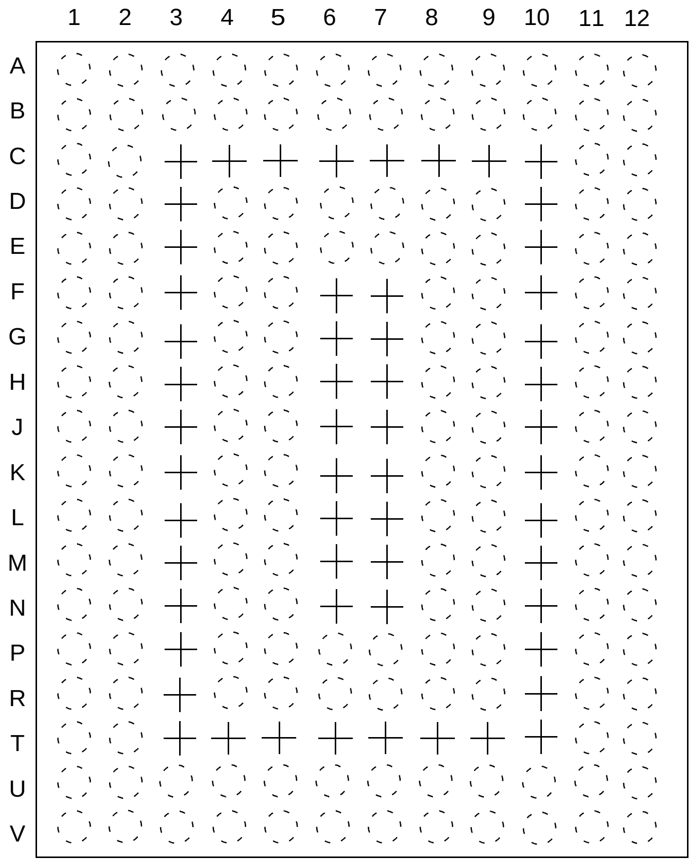
Applications

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS98ULPA877A or IDTCSPUA877A
- Ideal for DDR2 400, 533, 667, and 800

Block Diagram



Pin Configuration



**160-Ball BGA
TOP VIEW**

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGate EN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CLK	$\overline{\text{DCS0}}$		GND	GND			VDDR	VDDR		$\overline{\text{QCS0B}}$	$\overline{\text{QCS0A}}$
K	$\overline{\text{CLK}}$	$\overline{\text{DCS1}}$		VDDL	VDDL			GND	GND		$\overline{\text{QCS1B}}$	$\overline{\text{QCS1A}}$
L	$\overline{\text{RESET}}$	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	MCL	$\overline{\text{PTYERR}}$	MCH	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

NOTE:

1. An empty cell indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die). MCL denotes a pin that Must be Connected LOW. MCH denotes a pin that Must be Connected HIGH.

**160-Ball BGA
TOP VIEW**

Ball Assignment

Signal Group	Signal Name	Type	Description
Ungated Inputs	DCKE0, DCKE1, DODT0, DODT1	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select Gated Inputs	D0 ... D21	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select Inputs	$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN high) when at least one Chip Select input is LOW.
Re-Driven	Q0A...Q21A, Q0B...Q21B, $\overline{\text{QCSnA,B}}$ QCKEnA,B, QODTnA,B	SSTL_18	Outputs of the register, valid after the specified clock count outputs and immediately following a rising edge of the clock.
Parity Input	PARIN	SSTL_18	Input parity is received on pin PARIN and should maintain odd parity across the D0...D21 inputs, at the rising edge of the clock.
Parity Error	$\overline{\text{PTYERR}}$	Open Drain	When LOW, this output indicates that a parity error was output identified associated with the address and/or command inputs. $\overline{\text{PTYERR}}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program Inputs	CSGateEN	1.8V LVCMOS	Chip Select Gate Enable. When HIGH, the D0..D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0...D21 inputs will be latched and redriven on every rising edge of the clock.
Clock Inputs	CLK, $\overline{\text{CLK}}$	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CLK).
Miscellaneous Inputs	MCL, MCH		Must be connected to a logic LOW or HIGH.
	$\overline{\text{RESET}}$	SSTL_18	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{\text{RESET}}$ also resets the $\overline{\text{PTYERR}}$ signal.
	V_{REF}	0.9V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.

Function Table

Inputs[1]							Outputs			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGate EN	CLK	$\overline{\text{CLK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS0x}}$	$\overline{\text{QCS1x}}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L	L

[1] H = HIGH Voltage Level
L = LOW Voltage Level
X = Don’t Care
↑ = LOW to HIGH
↓ = HIGH to LOW

Parity and Standby Function Table

Inputs[1]							Outputs
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CLK	$\overline{\text{CLK}}$	Σ of Inputs = H (D1 - D21)	PARIN[2]	$\overline{\text{PTYERR}}$[3]
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{\text{PTYERR}}_0$
H	X	X	L or H	L or H	X	X	$\overline{\text{PTYERR}}_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	H

1 H = HIGH Voltage Level
L = LOW Voltage Level
X = Don’t Care
↑ = LOW to HIGH
↓ = HIGH to LOW

2 PARIN arrives one clock cycle after the data to which it applies.

3 This transition assumes $\overline{\text{PTYERR}}$ is HIGH at the crossing of CLK going HIGH and $\overline{\text{CLK}}$ going LOW. If $\overline{\text{PTYERR}}$ is LOW, it stays latched LOW for two clock cycles or until $\overline{\text{RESET}}$ is driven LOW.

Absolute Maximum Ratings

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Item		Rating
Supply Voltage, V_{DD}		-0.5V to 2.5V
Input Voltage Range, V_I[1]		-0.5V to V_{DD} + 2.5V
Output Voltage Range, V_O[1,2]		-0.5V to V_{DDQ} + 0.5V
Input Clamp Current, I_{IK}		±50mA
Output Clamp Current, I_{OK}		±50mA
Continuous Output Clamp Current, I_O		±50mA
Continuous Current through each V_{DD} or GND		±100mA
Package Thermal Impedance (θja)[3]	0m/s Airflow	44.3° C/W
	1m/s Airflow	38.1° C/W
Storage Temperature, T_{STG}		-65 to +150° C

1 The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
2 This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.
3 The package thermal impedance is calculated in accordance with JESD 51.

Operating Characteristics

The $\overline{\text{RESET}}$ and CSGateEN inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless $\overline{\text{RESET}}$ is LOW.

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{DD}	I/O Supply Voltage		1.7	1.8	1.9	V
V_{REF}	Reference Voltage		0.49 * V_{DD}	0.5 * V_{DD}	0.51 * V_{DD}	V
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input Voltage		0		V_{DD}	V
V_{IH}	AC High-Level Input Voltage	Dn, PARIN, $\overline{\text{DCSn}}$, DCKEn, DODTn	V_{REF} + 0.25			V
V_{IL}	AC Low-Level Input Voltage				V_{REF} - 0.25	
V_{IH}	DC High-Level Input Voltage		V_{REF} + 0.125			
V_{IL}	DC Low-Level Input Voltage				V_{REF} - 0.125	
V_{IH}	High-Level Input Voltage	$\overline{\text{RESET}}$, CSGateEN	0.65 * V_{DDQ}			V
V_{IL}	Low-Level Input Voltage				0.35 * V_{DDQ}	
V_{ICR}	Common Mode Input Range	CLK, $\overline{\text{CLK}}$	0.675		1.125	V
V_{ID}	Differential Input Voltage		600			mV
I_{OH}	High-Level Output Current				-8	mA
I_{OL}	Low-Level Output Current				8	
I_{ERROL}	$\overline{\text{PTYERR}}$ LOW Level Output Current		25			mA
T_A	Operating Free-Air Temperature		0		+70	°C

DC Electrical Characteristics Over Operating Range

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = 0°C to +70°C, V_{DD} = 1.8V ± 0.1V.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = -6mA, V_{DDQ} = 1.7V	1.2			V
V_{OL}	Output LOW Voltage	I_{OL} = 6mA, V_{DDQ} = 1.7V			0.5	V
V_{ERROL}	$\overline{PTYERR}$ Output LOW Voltage	I_{ERROL} = 25mA, V_{DD} = 1.7V			0.5	V
I_{IL}	All Inputs	V_I = V_{DD} or GND; V_{DD} = 1.9V	-5		+5	µA
I_{DD}	Static Standby	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = GND		200		µA
	Static Operating	I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK = $\overline{CLK}$ = $V_{IH(AC)}$ or $V_{IL(AC)}$			10	mA
		I_O = 0, V_{DD} = 1.9V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK = $V_{IH(AC)}$, $\overline{CLK}$ = $V_{IL(AC)}$		120		
I_{DDD}	Dynamic Operating (clock only)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle		300		µA/Clock MHz
	Dynamic Operating (per each data input)	I_O = 0, V_{DD} = 1.8V, $\overline{RESET}$ = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and $\overline{CLK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.		40		µA/Clock MHz/ Data
C_{IN}	Dn, PARIN	V_I = V_{REF} ± 350mV	2		3	pF
	CLK and $\overline{CLK}$	V_{ICR} = 1.25V, V_{IPP} = 360mV	2.5		3.5	
	$\overline{RESET}$	V_I = V_{DD} or GND		5		

Timing Requirements Over Recommended Operating Free-Air Temperature Range

Symbol	Parameter		V_{DD} = 1.8V ± 0.1V		Units
			Min.	Max.	
f_{CLOCK}	Clock Frequency			410	MHz
t_W	Pulse Duration; CLK, $\overline{\text{CLK}}$ HIGH or LOW		1		ns
t_{ACT}	Differential Inputs Active Time[1]			10	ns
t_{INACT}	Differential Inputs Inactive Time[2]			15	ns
t_{SU}	Setup Time	$\overline{\text{DCS0}}$ before CLK↑ , $\overline{\text{CLK}}$↓, $\overline{\text{DCS}}$ and CSGateEN HIGH; $\overline{\text{DCS1}}$ before CLK↑ , $\overline{\text{CLK}}$↓, $\overline{\text{DCS0}}$ and CSGateEN HIGH[3]	0.6		ns
		$\overline{\text{DCSn}}$, DODT, DCKE, and Dn after CLK↑ , $\overline{\text{CLK}}$↓	0.5		
		PARIN after CLK↑ , $\overline{\text{CLK}}$↓	0.5		
t_H	Hold Time	$\overline{\text{DCSn}}$, DODT, DCKE, and Dn after CLK↑ , $\overline{\text{CLK}}$↓	0.4		ns
		PARIN after CLK↑ , $\overline{\text{CLK}}$↓	0.4		

[1] V_{REF} must be held at a valid input voltage level and data inputs must be held at valid logic levels for a minimum time of t_{ACT}(max) after $\overline{\text{RESET}}$ is taken HIGH.

[2] V_{REF}, data, and clock inputs must be held at a valid input voltage levels (not floating) for a minimum time of t_{INACT}(max) after $\overline{\text{RESET}}$ is taken LOW.

[3] t_{SU} = 700ps for $\overline{\text{DCSx}}$ exiting Suspention Mode.

Switching Characteristics Over Recommended Free Air Operating Range (unless otherwise noted)

Symbol	Parameter	V_{DD} = 1.8V ± 0.1V		Units
		Min.	Max.	
f_{MAX}	Max Input Clock Frequency	410		MHz
t_{PDM}[1]	Propagation Delay, single bit switching, CLK↑ / $\overline{\text{CLK}}$↓to Qn	1.1	1.5	ns
t_{PDQ}[2]	Propagation Delay, single-bit switching, CLK↑ / $\overline{\text{CLK}}$↓to Qn	0.4	0.8	ns
t_{PDMSS}[1]	Propagation Delay, simultaneous switching, CLK↑ / $\overline{\text{CLK}}$↓to Qn		1.6	ns
t_{LH}	LOW to HIGH Propagation Delay, CLK↑ / $\overline{\text{CLK}}$↓to $\overline{\text{PTYERR}}$	1.2	3	ns
t_{HL}	HIGH to LOW Propagation Delay, CLK↑ / $\overline{\text{CLK}}$↓to $\overline{\text{PTYERR}}$	1.0	3	ns
t_{PHL}	HIGH to LOW Propagation Delay, $\overline{\text{RESET}}$↓to Qn↓		3	ns
t_{PLH}	LOW to HIGH Propagation Delay, $\overline{\text{RESET}}$↓to $\overline{\text{PTYERR}}$↑		3	ns

[1] Design target as per JEDEC specifications.

[2] Production Test. (See Production Test Circuit in TEST CIRCUIT AND WAVEFORM section.)

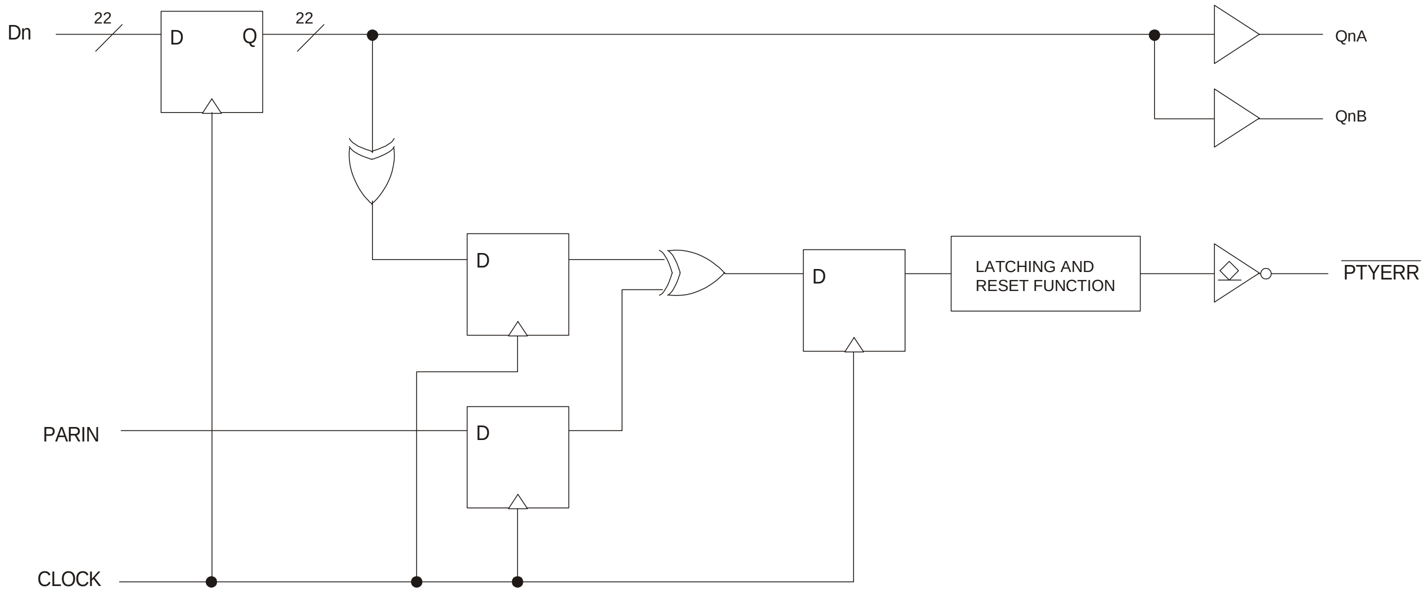
Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range

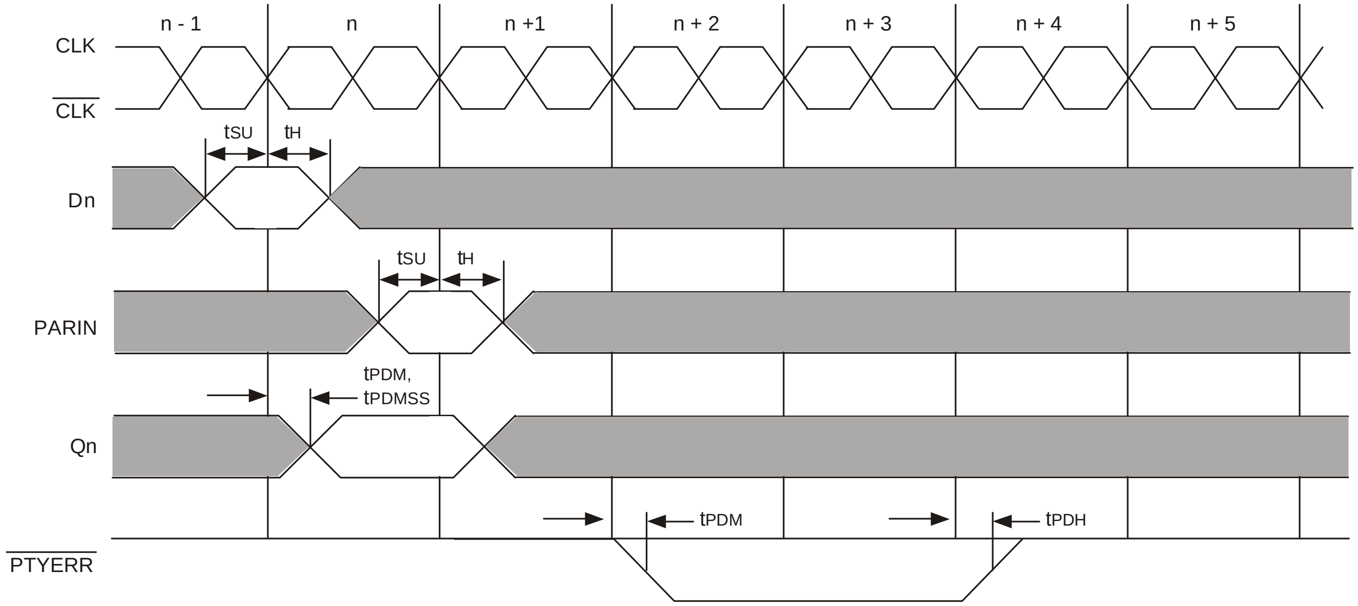
Parameter	V_{DD} = 1.8V ± 0.1V		Units
	Min.	Max.	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]		1	V/ns

[1] Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).

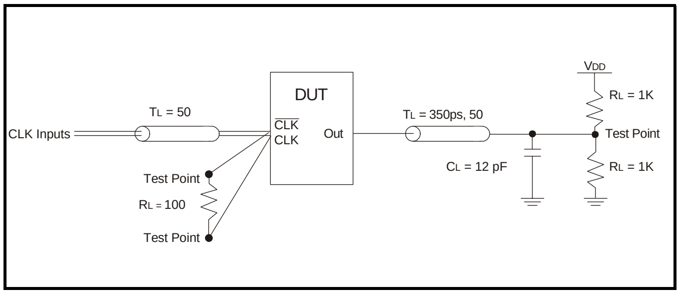
Parity Logic Diagram



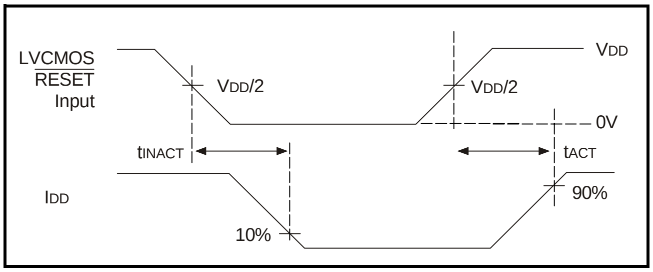
Register Timing



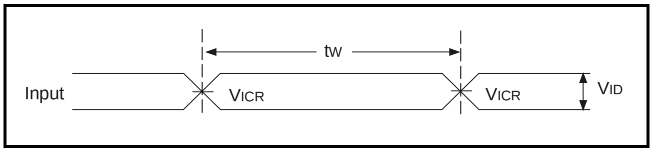
Test Circuits and Waveforms (V_{DD} = 1.8V ± 0.1V)



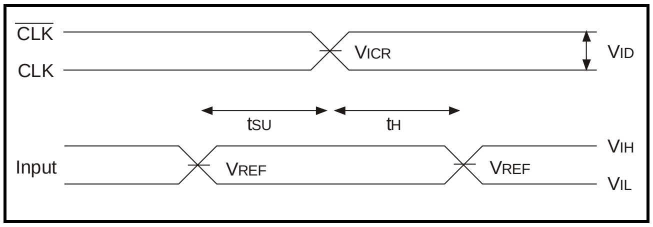
Simulation Load Circuit



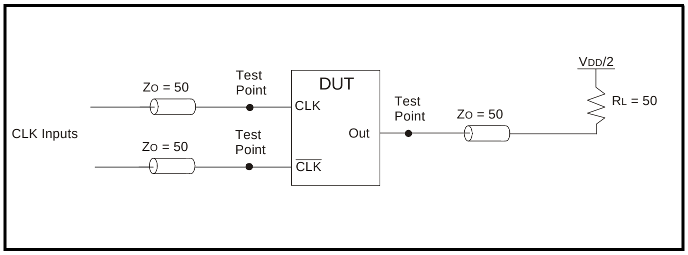
Voltage and Current Waveforms Inputs Active and Inactive Times



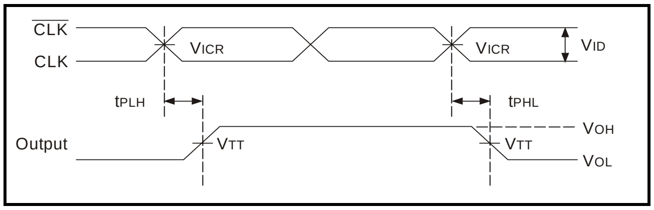
Voltage Waveforms - Pulse Duration



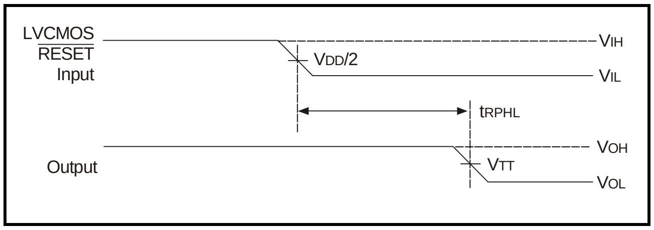
Voltage Waveforms - Setup and Hold Times



Production-Test Load Circuit



Voltage Waveforms - Propagation Delay Times

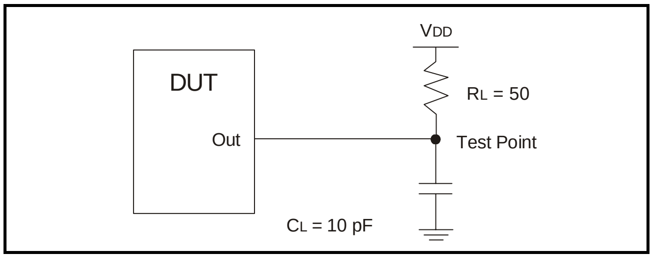


Voltage Waveforms - Propagation Delay Times

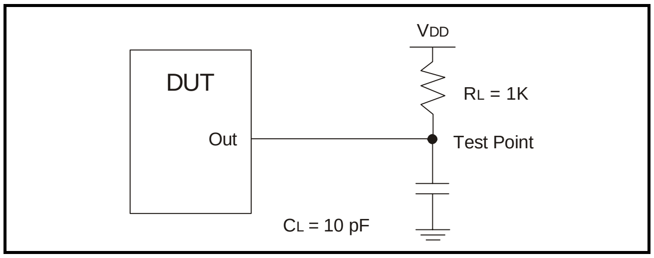
NOTES:

1. C_L includes probe and jig capacitance.
2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA
3. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. V_{TT} = V_{REF} = V_{DD}/2
6. V_{IH} = V_{REF} + 250mV (AC voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.
7. V_{IL} = V_{REF} - 250mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600mV.
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.

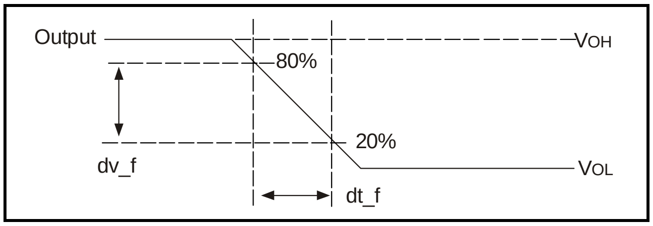
Test Circuits and Waveforms (V_{DD} = 1.8V ± 0.1V)



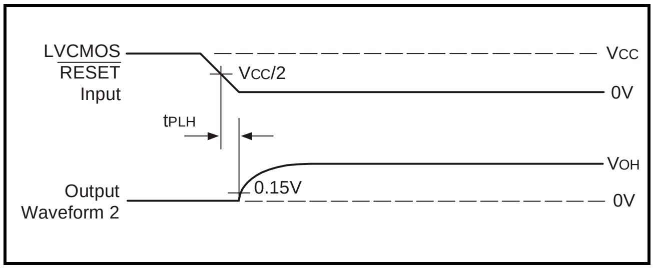
Load Circuit: High-to-Low Slew-Rate Adjustment



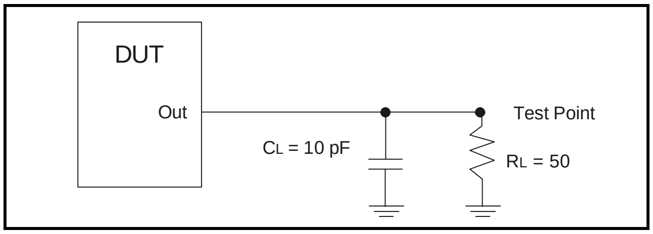
Load Circuit: Error Output Measurements



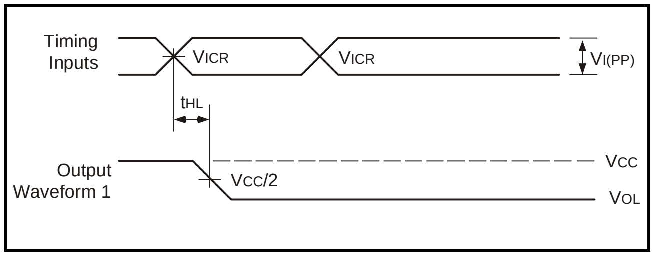
Voltage Waveforms: High-to-Low Slew-Rate Adjustment



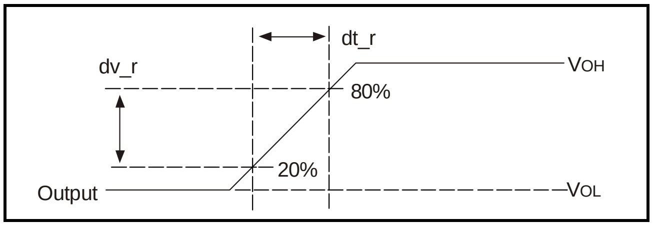
Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to RESET input)



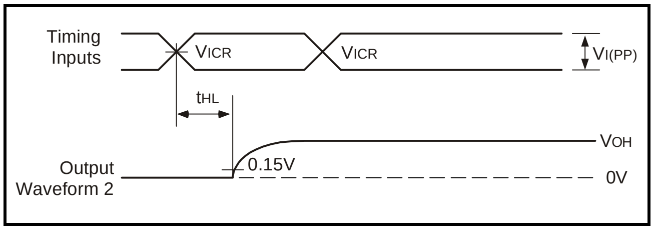
Load Circuit: Low-to-High Slew-Rate Adjustment



Voltage Waveforms: Open Drain Output High-to-Low Transition Time (with respect to clock inputs)



Voltage Waveforms: Low-to-High Slew-Rate Adjustment



Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with respect to clock inputs)

NOTES:

1. CL includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Zo = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

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