Integrated Device Technology Inc

8-BIT CMOS VIDEO DAC

IDT75C18

FEATURES:

- Graphics-ready
- Pin- and function-compatible with TRW TDC1018
- 8 bits, 1/2 LSB linearity
- 70, 100, 125MHz models available
- ECL-compatible inputs
- Low power dissipation < 400mW
- Power supply noise rejection > 50dB
- Registered data and video controls
- Differential current outputs
- Flexible video controls
- Inherently low glitch energy
- Multiplying mode capability
- Single 5V power supply
- Available in 24-pin hermetic DIP, 24-pin plastic DIP and 28-pin LCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

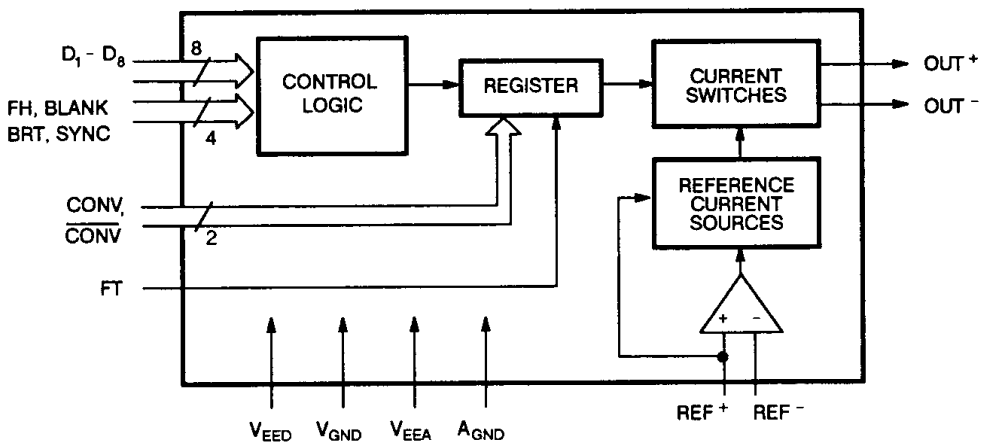
The IDT75C18 is a 70/100/125 MegaSample per Second (MSPS), 8-bit Digital to Analog Converter. It can directly drive a doubly terminated 75Ω load to levels compatible with RS-343A. Four special controls for blanking, synchronization and highlighting allow the device to be used in typical video applications with no extra components

The IDT75C18 is built using IDT's high-performance CEMOS ™ process. Innovative design methods, which include on-chip data registers and precise matching of propagation delays, as well as an improved segmenting/decoding architecture, significantly reduce glitch energy. The IDT75C18 offers high-performance and low power in a 24-pin hermetic DIP, 24-pin plastic DIP or 28-pin LCC.

The IDT75C18 is pin- and function-compatible with the TRW TDC1018, with the advantage of low power due to CMOS processing. Besides providing higher reliability by running cooler, power supply requirements are reduced. Another advantage of the lower power dissipation is that this part may be packaged in a space-saving, cost-effective, 0.3-inch plastic package.

The IDT75C18 military DAC is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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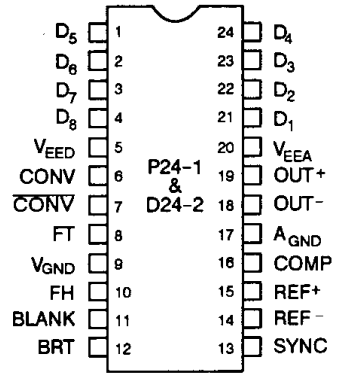
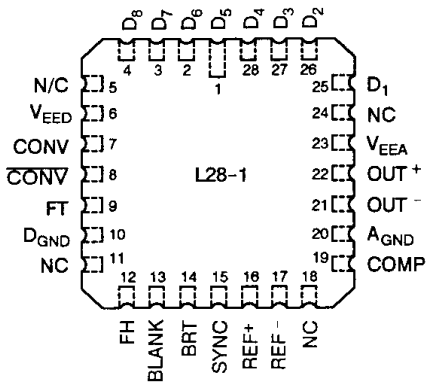
CEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

FUNCTIONAL DESCRIPTION
GENERAL INFORMATION

The IDT75C18 output current is proportional to the product of the digital input data and the analog reference current. All the digital inputs, data and control are compatible with standard ECL logic levels. The IDT75C18 is normally operated synchronously with data being latched by the rising edge of the convert clock, CONV. FT, the feedthrough control input, determines the operating mode. When FT is LOW, the part operates in the synchronous mode and the low-to-high transition of the convert clock, CONV, latches data and control values into internal D-type registers. The registered values are then decoded and presented to switched current sinks which produce the appropriate analog output values. When FT is HIGH, the part operates asynchronously and the digital inputs are not latched. The analog output, then, changes in response to the digital inputs without regard to clock. FT is the only asynchronous input and is typically tied to the appropriate DC level.

The IDT75C18 uses a 6x2 segmented DAC approach where the six MSBs of the input data are decoded into a parallel "Thermometer" code which produces sixty-four "coarse" output levels. The remaining two LSBs of the input data drive three binary weighted current switches with a total contribution of one-sixty-fourth of full scale. The MSB and LSB currents are summed at the output to produce 256 analog levels.

SYNC, BLANK, FH (Force High) and BRT (BRighT) are special control inputs which drive appropriately weighted current switches. These currents are summed at the output with the level produced by the data inputs to allow for specific levels required by video applications such as the sync pulses and the blanking levels.

POWER CONSIDERATIONS

The IDT75C18 operates from separate analog and digital supplies to provide the highest noise immunity on the analog output to digital switching spikes. All power and ground pins must be connected.

REFERENCE CONSIDERATIONS

The IDT75C18 has two reference inputs, REF^+ and REF^-, which are simply the non-inverting and inverting inputs to an internal buffer amplifier. The output of this amplifier serves as the reference for the transistors in the DAC. The feedback loop internally includes current sources which are identical to the current sink transistors, guaranteeing that the reference current will be precisely mirrored in the DAC.

Since the output currents are proportional to the digital data and the reference current, the full-scale output current may be adjusted over a limited range by varying the reference current. In the same vein, the stability of the output depends strongly on the stability of the reference. The reference current is normally applied to REF^+, while REF^- is usually connected to a negative reference through a resistor equal to the effective impedance seen on REF^+.

Through careful design of the reference amplifier, no external compensation capacitor is required and the COMP pin should be left unconnected.

CONTROLS

The IDT75C18 has four special control inputs: SYNC, BLANK, FH (Force High) and BRT (BRighT), as well as FT (Feed Through control). Typically, the IDT75C18 is operated in the synchronous mode which ensures the lowest output noise. When FT is forced HIGH, the input registers pass the data and control information through without latching, allowing the analog output to change asynchronously.

In the synchronous mode, the control inputs are registered by the rising edge of CONV in the same manner as the data inputs. The controls, like the data, must be stable for a set-up time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode, only the minimum pulse widths are relevant.

The video controls produce specific output levels which are used for frame synchronization, horizontal blanking, etc. as described in various standards such as RS-343A. The effect of these controls on the analog output is shown below. The internal logic simplifies the use of the controls in video applications. BLANK, SYNC and FH override the data inputs. SYNC overrides all other inputs and produces a full negative level. FH drives the analog output to full-scale producing a reference white level. The BRT control creates a "whiter than white" level by adding 10% of full-scale to the present output value.

VIDEO CONTROL OUTPUT VALUES[4]

DESCRIPTION	SYNC	BLANK	FH	BRT	DATA	OUT⁻(mA)[1]	OUT⁻(V)[2]	OUT⁻(IRE)[3]
Sync	1	X	X	X	X	28.57	-1.071	-40.0
Blank	0	1	X	X	X	20.83	-0.781	0.0
10% White	0	0	1	1	X	0.00	0.00	110.0
White	0	0	1	0	X	1.95	-0.073	100.0
Black	0	0	0	0	00	19.40	-0.728	7.5
White	0	0	0	0	FF	1.95	-0.073	100.0
10% Black	0	0	0	1	00	17.44	-0.654	17.5
10% White	0	0	0	1	FF	0.00	0.00	110.0

NOTES:

1. OUT^+ is complementary to OUT^-. Current is specified as conventional current when flowing into the device. $I_{OUT+} = 28.57 - I_{OUT-}$.
2. Voltage produced when driving the standard load configuration (37.5 ohms). See Figure 4.
3. 140 IRE units = 1.00V
4. RS-343A tolerance on all control values is assumed.

DATA INPUTS

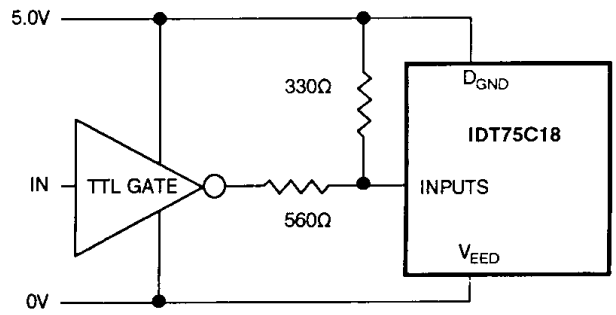
The inputs of the IDT75C18 are single ended, ECL-compatible. Internal pull down resistors force unconnected pins to a logic LOW level.

In the synchronous mode (FT is LOW), the data inputs are registered by the rising edge of CONV. The data inputs must be stable for a set-up time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode (FT is HIGH), the input registers are disabled and only the minimum pulse widths are relevant. In this mode, the analog output changes asynchronously in response to the input data.

SYMBOL	FUNCTION
D_1	Data Bit 1 (MSB)
D_2	•
D_3	•
D_4	•
D_5	•
D_6	•
D_7	•
D_8	Data Bit 8 (LSB)

The inputs of the IDT75C18 are voltage comparators with the threshold level set to approximately -1.27V, ensuring the correct logic state when driven by standard ECL outputs. It is possible to overdrive the inputs without harming the device, allowing a direct interface to CMOS logic. In general, the input signals will correctly drive the IDT75C18 as long as they remain between V_{EED}, V_{EEA} and A_{GND}, D_{GND} and meet the V_{IL} and V_{IH} specifications.

The diagram below shows a simple two resistor level shifter which allows the IDT75C18 to be driven from TTL signals.

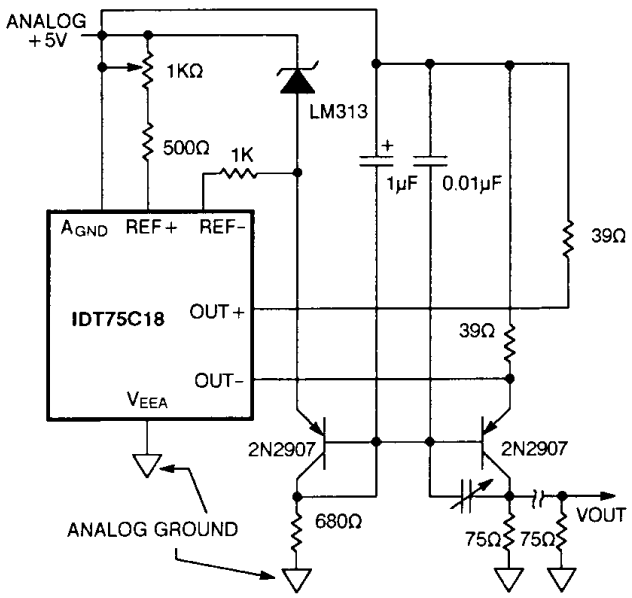


CLOCK INPUT CONV

The clock input to the IDT75C18 (CONV) is a differential ECL-compatible input. This signal may be driven single ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}) which determines the switching threshold of CONV.

ANALOG OUTPUTS

The two analog outputs of the IDT75C18 are high impedance complementary current sinks which are capable of driving a doubly terminated 75 ohm load to standard video levels. The output voltage will be the product of the output current and the effective load impedance and will usually be between 0 and -1V when the V_{EE} = -5.2V. The outputs sink current from A_{GND}, so that in the positive supply case (interfacing to CMOS or TTL), the output voltage swings between +5V and +4V. In AC coupled applications, this DC bias is unimportant. Shown below is a simple circuit which references the output voltage to the most negative supply.



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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{EED}	Measured to D_{GND}	-7.0 to +0.05	V
V_{EEA}	Measured to D_{GND}	-7.0 to +0.05	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGES			
CONV, Data & Controls	Measured to D_{GND}	V_{EED} to 0.5	V
REF Input, Applied Voltage (2)	Measured to A_{GND}	V_{EEA} to 0.5	V
REF Input, Applied Current (3,4)	REF+	6.0	mA
	REF-	0.5	mA
OUTPUT			
Analog Output, Applied Voltage (2)	Measured to A_{GND}	-2.0 to +0.4	V
Analog Output, Applied Current (3,4)		50	mA
Short Circuit Duration		Unlimited	
TEMPERATURE			
Operating, Ambient	Military	-55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	-65 to +150	°C
	Commercial	-55 to +125	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{EED}	Digital Supply Voltage (REF D_{GND})		-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (REF A_{GND})		-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (REF D_{GND})		-0.1	0	+0.1	V
V_{EEA}-V_{EED}	Supply Voltage Differential		-0.1	0	+0.1	V
V_{ICM}	CONV, Common Mode Range		-0.5	—	-2.5	V
V_{IDF}	CONV, Differential Range		0.4	—	1.2	V
V_{IL}	Input Voltage, Logic LOW		-1.49	—	—	V
V_{IH}	Input Voltage, Logic HIGH		—	—	-1.045	V
I_{REF}	Reference Current, Video Std.(1) 8-Bit Lin.		1.059 1.0	1.115 —	1.171 1.3	mA mA
T_A	Ambient Temperature	MIL.	-55	—	+125	°C
		COM'L.	0	—	+70	°C

NOTE:

1. Minimum and maximum values allowed by ±5% variation given in RS-343A and RS-170 after initial gain correction of device.

DC ELECTRICAL CHARACTERISTICS

Specified over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
I_{EEA+} I_{EED}	Supply Current	$V_{EEA} = V_{EED}$ = Max.,(1)Static	—	125	mA
C_{REF}	Equivalent Input C, REF (+), REF (-)		—	5	pF
C_I	Input Capacitance, Data & Controls		—	5	pF
V_{OCP}	Compliance Voltage, +Output		-1.2	+0.1	V
V_{OCN}	Compliance Voltage, -Output		-1.2	+0.1	V
R_O	Equivalent Out R		20	—	kΩ
C_O	Equivalent Out C		—	20	pF
I_{OP}	Max. I, +Output	V_{EEA} = Typ., SYNC = BLANK= 0 FH = BRT = 1	30	—	mA
I_{ON}	Max. I, -Output	V_{EEA} = Typ.,SYNC = 1	30	—	mA
I_{IL}	Input Current, Logic LOW, Data & Controls	V_{EED} = Max.; V_I = -1.40V	—	200	µA
I_{IH}	Input Current, Logic HIGH, Data & Controls	V_{EED} = Max.; V_I = -1.00V	—	200	µA
I_{IC}	Input Current, CONV	V_{EED} = Max.; -2.5 < V_I < -0.5	—	50	µA

NOTE:

1. Worst case for all Data and Control States. No termination on I_{OUT+} or I_{OUT-}.

AC ELECTRICAL CHARACTERISTICS

Specified over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	IDT75C18x70 MIN.	IDT75C18x70 MAX.	IDT75C18x100 MIN.	IDT75C18x100 MAX.	IDT75C18x125 MIN.	IDT75C18x125 MAX.	UNIT
F_S	Max. Conversion Rate	V_{EEA}, V_{EED} = Min.	—	70	—	100	—	125	MHz
t_{PWL}	CONV LOW Time	V_{EEA}, V_{EED} = Min.	6	—	5	—	4	—	ns
t_{PWH}	CONV HIGH Time	V_{EEA}, V_{EED} = Min.	6	—	5	—	4	—	ns
t_S	Set-up Time, Data & Control	V_{EEA}, V_{EED} = Min.	8	—	6	—	5	—	ns
t_H	Hold Time, Data & Control	V_{EEA}, V_{EED} = Min.	5	—	1	—	0	—	ns
t_{DSC}	CONV to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 0	—	14	—	10	—	8	ns
t_{DST}	DATA to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 1	—	20	—	16	—	13	ns
t_{SI}	Current Setting Time	V_{EEA}, V_{EED} = Min. FT = 0							
		0.2%	—	—	—	—	—	—	ns
		0.8%	—	—	—	—	—	—	ns
		3.2%	—	—	—	—	—	—	ns
t_{RI}	Current Rise Time	10% to 90% of Full Scale	—	3.0	—	2.1	—	1.7	ns

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SYSTEM PERFORMANCE CHARACTERISTICS

Specified over the Recommended Operating Conditions unless otherwise stated.

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
ELI	Linearity Error Integral	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.2	%FS
ELD	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	0.2	%FS
IOF	Output Offset I	V_{EEA}, V_{EED} = Max. SYNC = BLANK = 0, FH = BRT = 1	–	±10	µA
EG	Abs. Gain Error	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	±5	%FS
TCG	Gain Error Tempco		–	±0.024	%FS/°C
BWR	Ref. Bandwidth -3dB	ΔV_{REF} = 1mV	1		MHz
DP	Differential Phase	4 x NTSC	–	1.0	Deg.
DG	Differential Gain	4 x NTSC	–	2.0	%
PSRR	Power Supp. Rej. Ratio	V_{EEA}, V_{EED}, I_{REF} = Typ.(1)	–	45	dB
		V_{EEA}, V_{EED}, I_{REF} = Typ.(2)	–	55	dB
PSS	Power Supp. Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Typ.	–	120	µV/V
GC	Peak Glitch Charge	Registered Mode Typ. (3, 4)	–	800	f_c
GI	Peak Glitch Current	Registered Mode	–	1.2	mA
GE	Peak Glitch Energy	Registered Mode Typ. (4)	–	30	pV-Sec
FT_C	Clock Feedthrough	Data Constant (5)	–	-50	dB
FT_D	Data Feedthrough	Clock Constant (5)	–	-50	dB

NOTES:

1. 20kHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED} ; dB relative to full gray scale.
2. 60Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED} ; dB relative to full gray scale.
3. $f_{Coulombs}$ = microamps x nanoseconds.
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

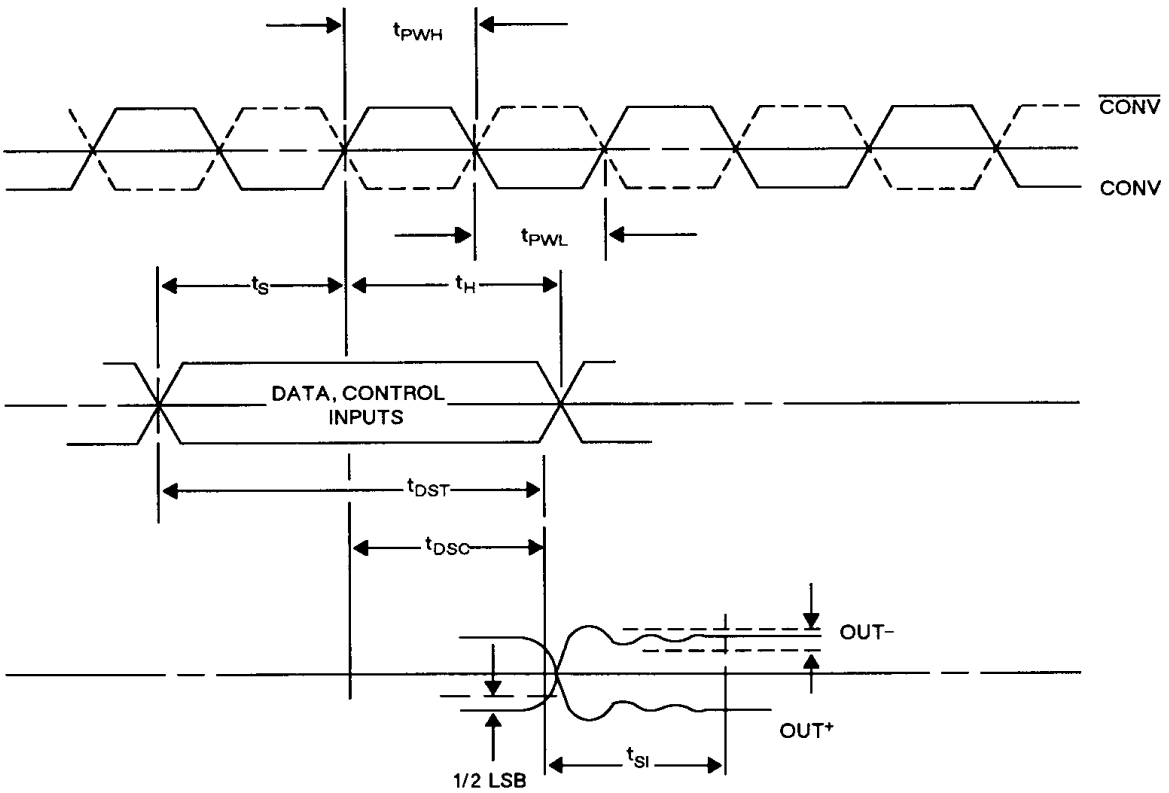

Figure 1. Timing Diagram

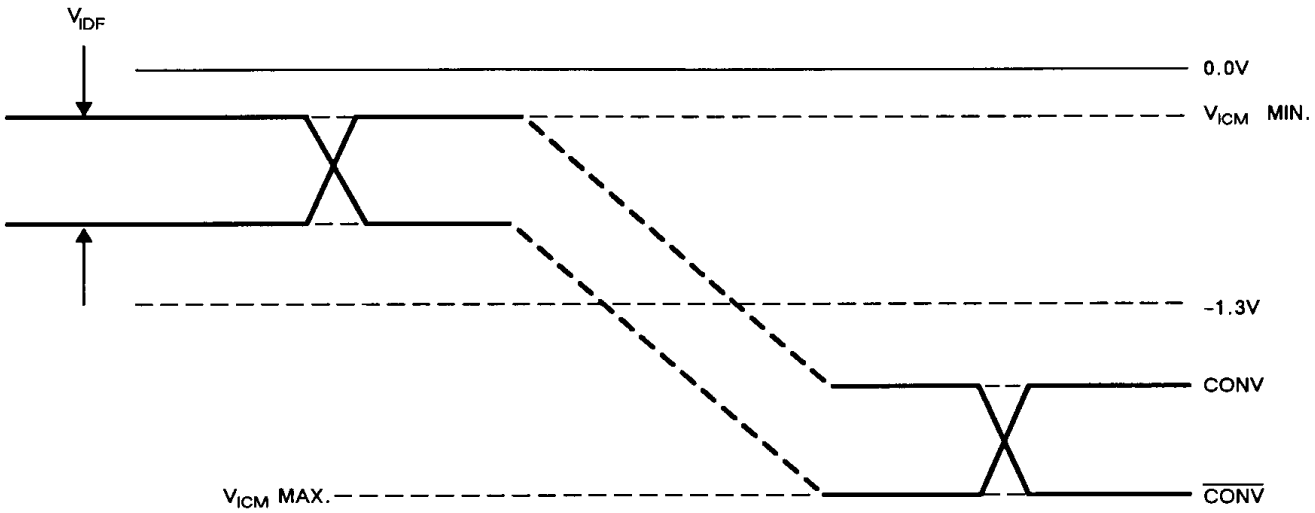

Figure 2. $\overline{CONV}$ert, CONVert Switching Levels

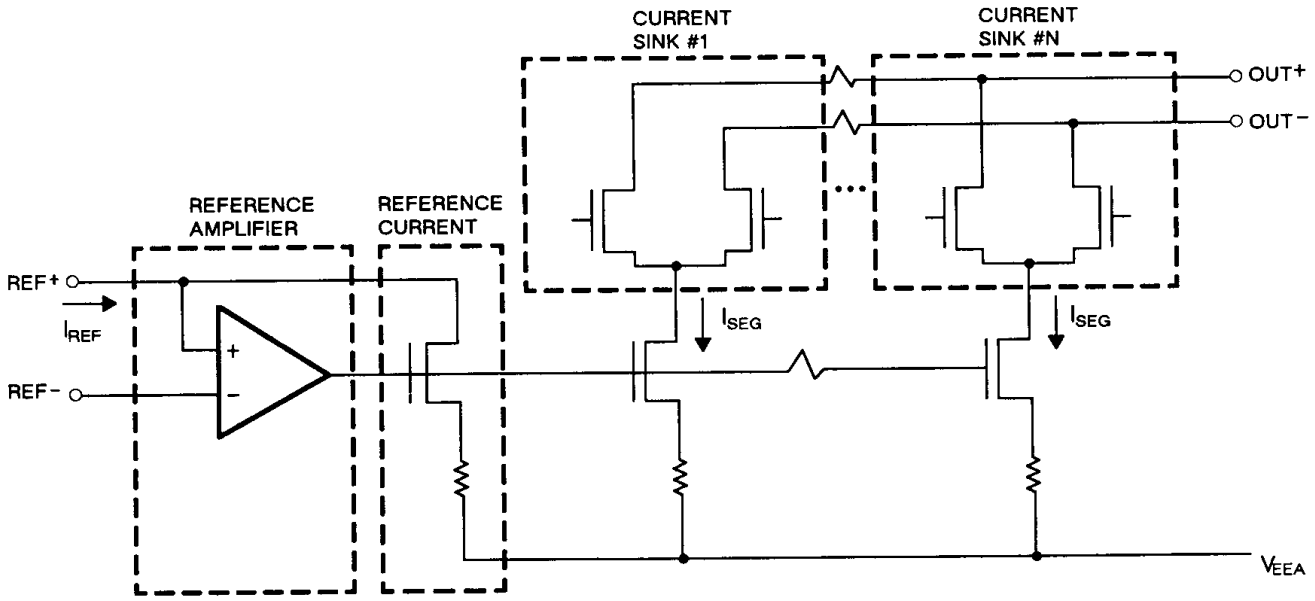

Figure 3. Equivalent Output Circuit

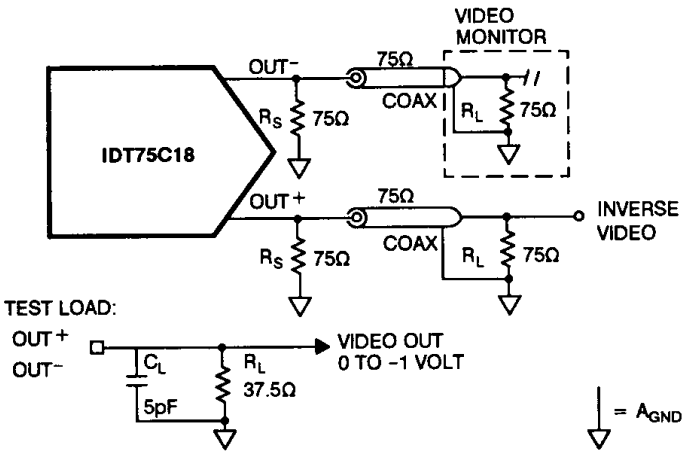

Figure 4. Standard Load Configuration

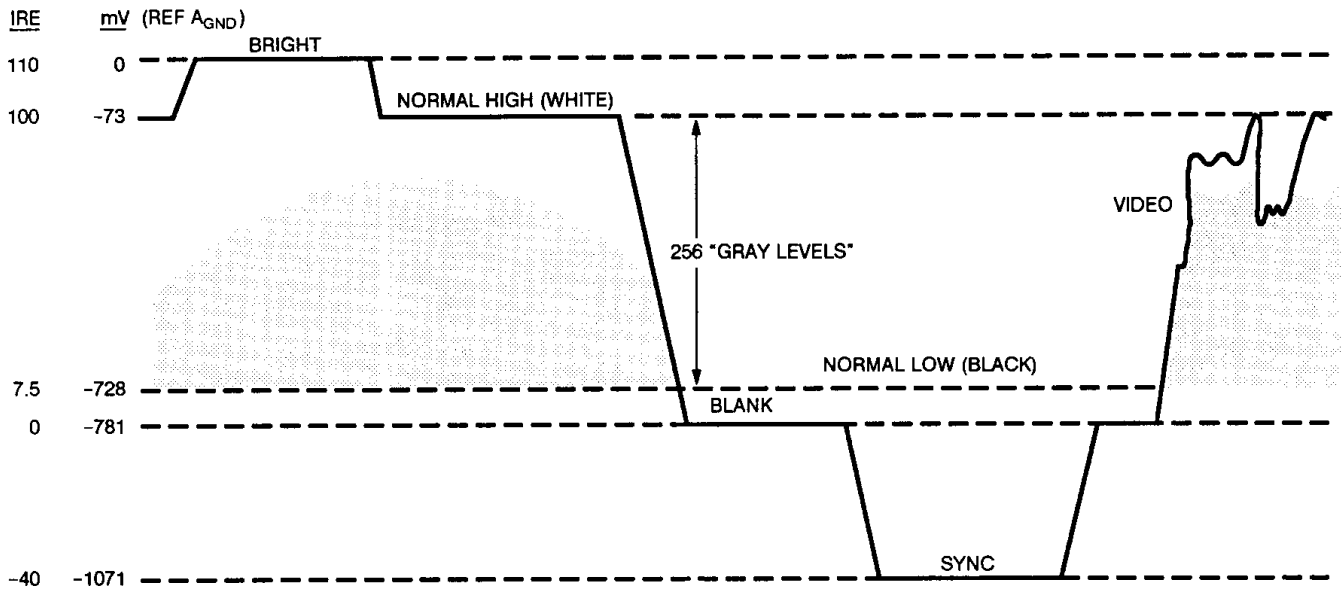

Figure 5. Video Output Waveform for Out- and Standard Load Configuration

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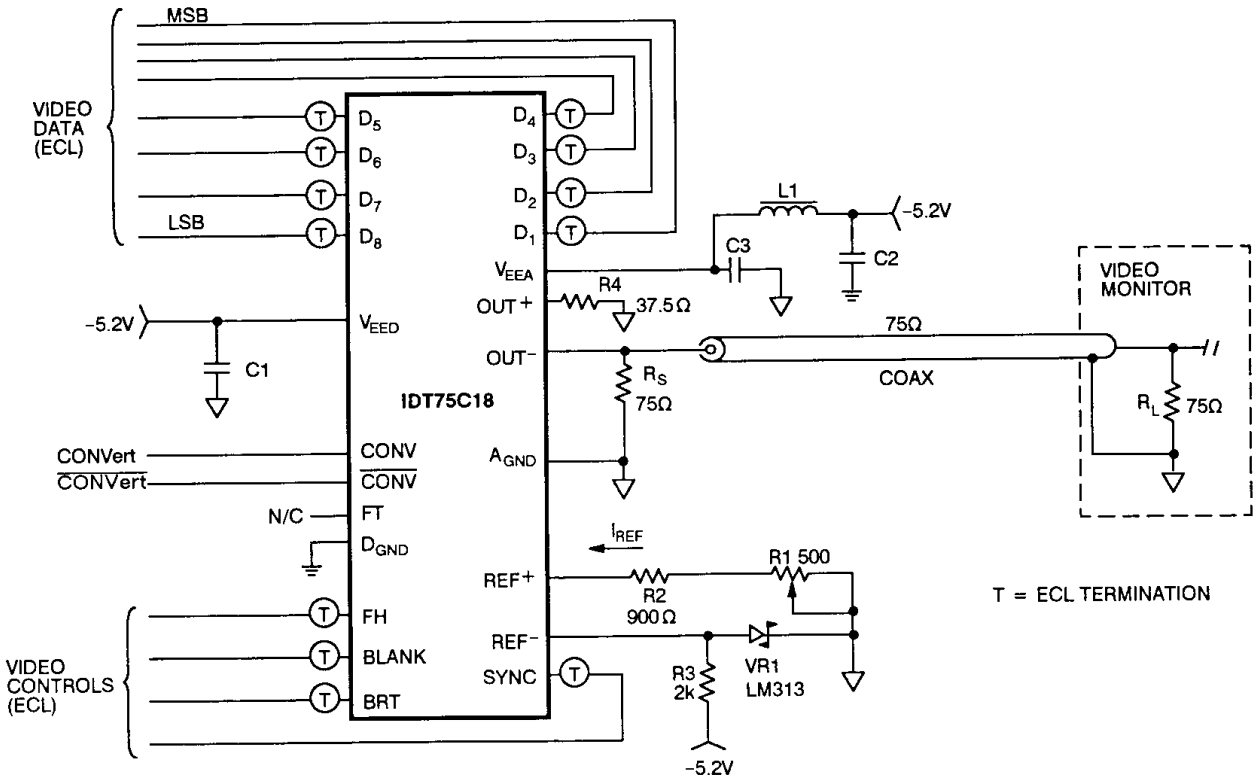
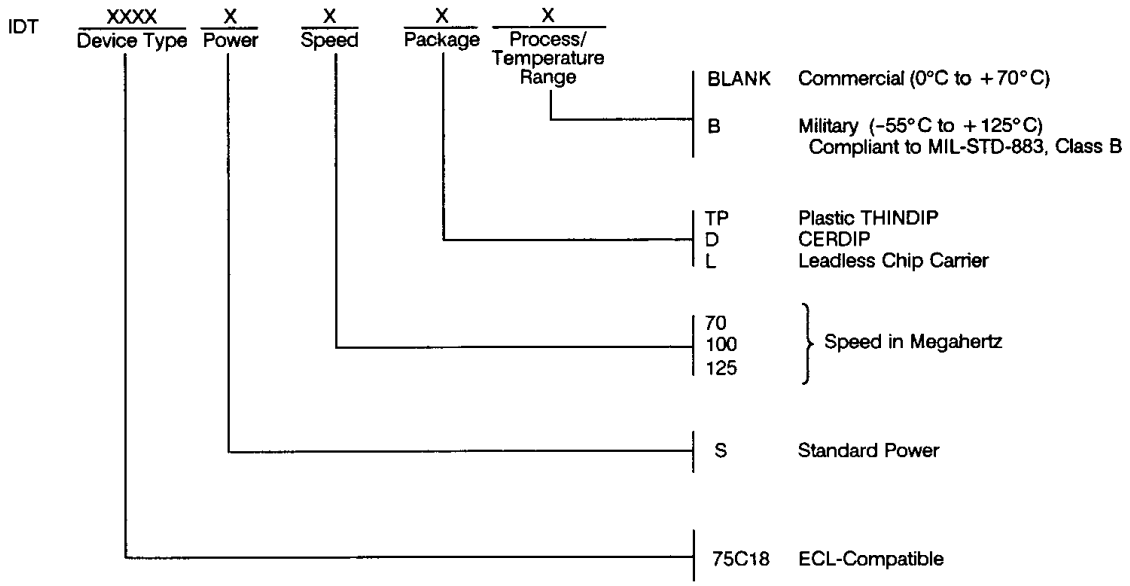


PARTS LIST

RESISTORS			
R1	1kΩ	Pot	10 Turn
R2	900Ω	1/8W	1% Metal Film
R3	2.00kΩ	1/8W	1% Metal Film
R4	37.5Ω	1/8W	1% Metal Film
CAPACITORS			
C1-C3	0.1μF	50V	Ceramic disc
INTEGRATED CIRCUITS			
U1	IDT75C18	D/A Converter	
VOLTAGE REFERENCES			
VR1	LM113 or LM313	Bandgap Reference	
INDUCTORS			
L1	Ferrite Bead Shield Inductor Fair-Rite P/N 2743001112 or Similar		

Figure 6. Typical Interface Circuit

ORDERING INFORMATION



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