8-BIT CMOS VIDEO DAC

IDT75C18
IDT75C28

Integrated Device Technology, Inc.

FEATURES:

- Graphics-ready
- Pin-compatible with TRW TDC1018
- 8 bits, 1/2 LSB linearity
- 70, 100, 125MHz models available
- ECL-compatible inputs — IDT75C18
- TTL-compatible inputs — IDT75C28
- Ultra-low power dissipation < 400mW
- Power supply noise rejection > 50dB
- Registered data and video controls
- Differential current outputs
- Flexible video controls
- Inherently low glitch energy
- Multiplying mode capability
- Single 5V power supply
- Available in 24-pin hermetic DIP, 24-pin plastic DIP and 28-pin LCC
- Military product is 100% screened to MIL-STD-883, Class B

DESCRIPTION

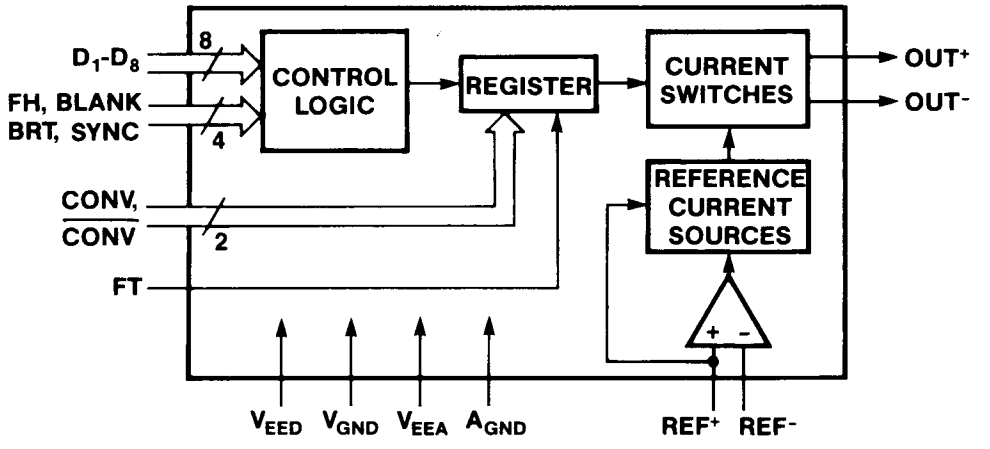
The IDT75C18/28 are 70/100/125 MegaSample per Second (MSPS), 8-bit Digital to Analog Converters, capable of directly driving a 75Ω load to standard video levels. Most applications require no extra registering, buffering or deglitching. Four special level controls simplify the interface for video applications. The IDT75C18 has ECL-compatible inputs while the IDT75C28 is TTL-compatible.

The IDT75C18/28 are built using IDT's high-performance CEMOS™ process. On chip data registers and precise matching of propagation delays, as well as an improved segmenting/decoding architecture, significantly reduce glitch energy. The IDT75C18/28 offer high-performance and ultra-low-power in a 24-pin hermetic DIP, 24-pin plastic DIP or 28-pin LCC.

The IDT75C18 is pin and functionally compatible with the TRW TDC1018, with the advantage of low power due to CMOS processing. Besides providing higher reliability by running cooler, power supply requirements are reduced. Another advantage of the lower power dissipation is that this part may be packaged in a space-saving, cost-effective, 0.3 inch plastic package.

The IDT75C18/28 Military DACs are 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

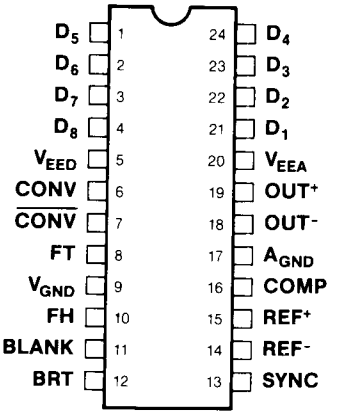
FUNCTIONAL BLOCK DIAGRAM



SSD75C18-001

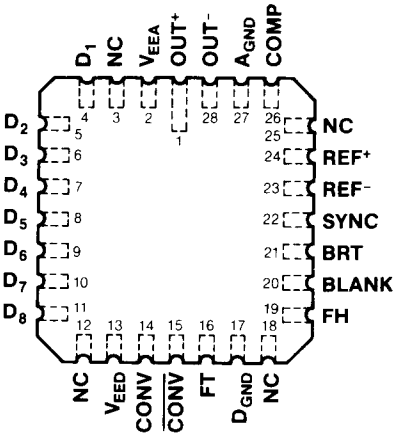
IDT75C18/28 8-BIT CMOS VIDEO DAC

PIN CONFIGURATIONS



SSD75C18-002

DIP
TOP VIEW



SSD75C18-003

LCC
TOP VIEW

FUNCTIONAL DESCRIPTION
GENERAL INFORMATION

The IDT75C18/28 develops complementary analog output currents proportional to the product of the digital input data and analog reference current. All data and control inputs are compatible with standard ECL logic levels (IDT75C18) or standard TTL logic levels (IDT75C28). FT, the feedthrough control input, determines whether the data and control inputs are synchronous or asynchronous. On the low-to-high transition of the convert clock CONV, the decoded data and control values are latched into an internal D-type register when FT is low. The registered values are then converted into the appropriate analog output by switched current sinks. When FT is HIGH, data and control inputs are not registered and the analog output asynchronously tracks the inputs. FT is the only asynchronous input and is normally tied to the appropriate DC level.

The IDT75C18/28 uses a 6x2 segmented DAC approach where the six MSBs or the input data are decoded into a parallel "Thermometer" code which produces sixty-four "coarse" output levels. The remaining two LSBs of the input data drive four binary weighted current switches with a total contribution of one-sixty-fourth of full scale. The MSB and LSB currents are summed at the output to produce 256 analog levels.

SYNC, BLANK, FH (Force High), and BRT (BRighT) are special control inputs which drive appropriately weighted current switches. These switches are summed at the output with the level produced by the data inputs to allow for specific levels required by video applications such as the sync pulses and the blanking levels.

POWER CONSIDERATIONS

The IDT75C18/28 operates from separate analog and digital supplies to provide the highest noise immunity on the analog output to digital switching spikes. In addition, supply levels are different between the IDT75C18 and IDT75C28 to provide ECL and TTL compatibility. All power and ground pins must be connected. The required power supply levels are shown below.

POWER SUPPLY LEVELS

SYMBOL	FUNCTION	IDT75C18 VALUE	IDT75C28 VALUE
V_{EEA}	Analog - Supply	-5.2V	0V
V_{EED}	Digital- Supply	-5.2V	0V
A_{GND}	Analog + Supply	0V	5V
D_{GND}	Digital + Supply	0V	5V

REFERENCE CONSIDERATIONS

The IDT75C18/28 have two reference current inputs, REF^+ and REF^- which are simply the non-inverting and inverting inputs to an internal buffer amplifier. The output of this amplifier serves as the reference for the transistors in the DAC. The feedback loop internally includes a transistor which is identical to the current sink transistors, guaranteeing that the reference current will be precisely mirrored in the DAC.

Since the output currents are proportional to the digital data and the reference current, the full-scale output current may be adjusted over a limited range by varying the reference current. In the same vein, the stability of the output depends strongly on the stability of the reference. The reference current is normally applied to REF^+, while REF^- is usually connected to a negative reference through a resistor equal to the effective impedance seen on REF^+.

Through careful design of the buffer amplifier, no external compensation capacitor is required. Although a COMP pin is provided, there is no internal connection and it should be left open.

CONTROLS

The IDT75C18/28 have four special control inputs: SYNC, BLANK, FH (Force High) and BRT (BRighT) as well as FT (Feed Through control). Typically, the IDT75C18/28 is operated in the synchronous mode which ensures the lowest output noise. When FT is forced HIGH, the input registers pass the data and control information through, without latching, allowing the analog output to change asynchronously.

In the synchronous mode, the control inputs are registered by the rising edge of CONV in the same manner as the data inputs. The controls, like the data, must be stable for a setup time (t_S) before, and a hold time (t_H) after, the rising edge of CONV. In the asynchronous mode, only the minimum pulse widths are relevant.

The video controls produce specific output levels which are used for frame synchronization, horizontal blanking, etc. as described in various standards such as RS-343A. The effect of these controls on the analog output is shown below. The internal logic simplifies the use of the controls in video applications. BLANK, SYNC and FH override the data inputs. SYNC overrides all other inputs and produces a full negative level. FH drives the analog output to full-scale producing a reference white level. The BRT control creates a "whiter than white" level by adding 10% of full-scale to the present output value.

VIDEO CONTROL OUTPUT VALUES

DESCRIPTION	SYNC	BLANK	FH	BRT	DATA	OUT^- (mA)(1)	OUT^- (V)(2)	OUT^- (IRE)(3)
Sync	1	X	X	X	X	28.57	-1.071	-40.0
Blank	0	1	X	X	X	20.83	-0.781	0.0
10% White	0	0	1	1	X	0.00	0.00	110.0
White	0	0	1	0	X	1.95	-0.073	100.0
Black	0	0	0	0	00	19.40	-0.728	7.5
White	0	0	0	0	FF	1.95	-0.073	100.0
10% Black	0	0	0	1	00	17.44	-0.654	17.5
10% White	0	0	0	1	FF	0.00	0.00	110.0

NOTES

1. OUT^+ is complementary to OUT^-. Current is specified as conventional current when flowing into the device.
2. Voltage produced when driving the standard load configuration (37.5 Ohms). See Figure 5.
3. 140 IRE units = 1.00V.
4. RS-343A tolerance on all control values is assumed.

DATA INPUTS

The inputs to the IDT75C18 are single ended, ECL compatible. Internal pull down resistors force unconnected pins to a logic LOW level. The inputs to the IDT75C28 are TTL compatible.

In the synchronous mode (FT is LOW), the data inputs are registered by the rising edge of CONV. The data inputs must be stable for a setup time (t_S) before, and a hold time (t_H), after the rising edge of CONV. In the asynchronous mode (FT is HIGH), the input registers are disabled and only the minimum pulse widths are relevant. In this mode, the analog output changes asynchronously in response to the input data.

DATA INPUTS

SYMBOL	FUNCTION
D_1	Data Bit 1 (MSB)
D_2	
D_3	•
D_4	•
D_5	•
D_6	
D_7	
D_8	Data Bit 8 (LSB)

CLOCK INPUT CONV

The clock input to the IDT75C18 (CONV) is a differential ECL compatible input. This signal may be driven single ended by connecting $\overline{CONV}$ to a suitable bias voltage (V_{BB}) which determines the switching threshold of CONV. The IDT75C28, which is TTL compatible, uses only the CONV pin. $\overline{CONV}$ should be connected to ground.

ANALOG OUTPUTS

The two analog outputs of the IDT75C18/28 are high impedance complementary current sinks which are capable of driving a doubly terminated 75 ohm load to standard video levels. The output voltage will be the product of the output current and the effective load impedance and will usually be between 0V and -1V (IDT75C18) or 5V and 4V (IDT75C28).

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
POWER SUPPLIES			
V_{EED}	Measured to D_{GND}	-7.0 to +0.05	V
V_{EEA}	Measured to D_{GND}	-7.0 to +0.05	V
A_{GND}	Measured to D_{GND}	-0.5 to +0.5	V
INPUT VOLTAGES			
CONV, Data & Controls	Measured to D_{GND}	V_{EED} to 0.5	V
REF Input, Applied Voltage	Measured to A_{GND}	V_{EEA} to 0.5	V
REF Input, Applied Current	REF^+ REF^-	6.0 0.5	mA mA
OUTPUT			
Analog Output, Applied Voltage	Measured to A_{GND}	-2.0 to +2.0	V
Analog Output, Applied Current		50	mA
Short Circuit Duration		Unlimited	
TEMPERATURE			
Operating, Ambient Junction		-60 to +140 +175	°C °C
Lead Soldering	10 secs	+300	°C
Storage		-60 to +150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

RECOMMENDED OPERATING CONDITIONS IDT75C18

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{EED}	Digital Supply Voltage (REF D_{GND})	-4.9	-5.2	-5.5	V
V_{EEA}	Analog Supply Voltage (REF A_{GND})	-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (REF D_{GND})	-0.1	0	+0.1	V
V_{EEA}- V_{EED}	Supply Voltage Differential	-0.1	0	+0.1	V
V_{ICM}	CONV, Common Mode Range	-0.5	—	-2.5	V
V_{IDF}	CONV, Differential Range	0.4	—	1.2	V
t_{PWL}	CONV, pulse width LOW	4	—	—	ns
t_{PWH}	CONV, pulse width HIGH	4	—	—	ns
t_S	Setup Time, Data & Controls	5	—	—	ns
t_H	Hold Time, Data & Controls	0	—	—	ns
V_{IL}	Input Voltage, Logic LOW	-1.49	—	—	V
V_{IH}	Input Voltage, Logic HIGH	—	—	-1.045	V
I_{REF}	Reference Current, Video Std.(1) 8-Bit Lin.	1.059 1.0	1.115 —	1.171 1.3	mA
T_A	Ambient Temperature	0	—	70	°C

RECOMMENDED OPERATING CONDITIONS IDT75C28

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{DGND}	Digital Supply Voltage (REF V_{EED})	4.5	5.0	5.5	V
V_{AGND}	Analog Supply Voltage (REF V_{EEA})	4.5	5.0	5.5	V
V_{EEA}	Analog Ground Voltage (REF V_{EED})	-0.1	0	+0.1	V
V_{AGND}- V_{DGND}	Supply Voltage Differential	-0.1	0	+0.1	V
t_{PWL}	CONV, pulse width LOW	4	—	—	ns
t_{PWH}	CONV, pulse width HIGH	4	—	—	ns
t_S	Setup time, data & controls	5	—	—	ns
t_G	Hold time, data & controls	0	—	—	ns
V_{IL}	Input Voltage, Logic LOW	0.8	—	—	V
V_{IH}	Input Voltage, Logic HIGH			1.5	V
I_{REF}	Reference Current, Video Std.(1) 8-Bit Lin.	1.059 1.0	1.115 —	1.171 1.3	mA
T_A	Ambient Temperature	0	—	70	°C

NOTE:

1. Minimum and Maximum values allowed by ±5% variation given in RS-343A and RS-170 after initial gain correction of device.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNITS
I_{EEA}^+ I_{EED}	Supply Current	$V_{EEA} = V_{EED}$ = Max,(1) static	—	—	—
		T_A = 0° C to 70° C	—	—	mA
		T_A = 70° C	—	—	mA
C_{REF}	Equivalent Input C, REF(+), REF(–)	—	—	5	pF
C_I	Input Capacitance, Data & Controls	—	—	5	pF
V_{OCP}	Compliance Voltage, + Output	—	-1.2	+0.1	V
V_{OCN}	Compliance Voltage, - Output	—	-1.2	+0.1	V
R_O	Equivalent Out R	—	20	—	kΩ
C_O	Equivalent Out C	—		20	pF
I_{OP}	Max I, +Output	V_{EEA} = Typ., SYNC = BLANK = 0 FH = BRT = 1	30	—	mA
I_{ON}	Max I, -Output	V_{EEA} = Typ., SYNC = 1	30	—	mA
I_{IL}	Input Current, Logic LOW, Data & Controls	V_{EED} = Max. IDT75C18; V_i = -1.40V IDT75C28; V_i = 0.8V	— —	200 100	μA μA
I_{IH}	Input Current, Logic HIGH, Data & Controls	V_{EED} = Max, IDT75C18; V_i = -1.00V IDT75C28 - V_i = 1.5V	— —	200 100	μA μA
I_{IC}	Input Current, CONV	V_{EED} = Max; IDT75C18; -2.5 < V_i < -0.5 IDT75C28; 0 < V_i < 2.0	— —	50 50	μA μA

NOTE: Worst case for all Data and Control States. No termination on I_{OUT+} or I_{OUT-}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNITS
F_S	Max. Conv Rate	V_{EEA}, V_{EED} = Min.	125	—	MHz
t_{DSC}	CONV to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 0	—	8	ns
t_{DST}	CONV to OUT Delay	V_{EEA}, V_{EED} = Min. FT = 1	—	13	ns
t_{SI}	Current Settling	V_{EEA}, V_{EED} = Min. FT = 0 0.2% 0.8% 3.2%	— — —	— — —	ns ns ns
t_{RI}	Current Rise Time	10% to 90% of full scale	—	1.7	ns

SYSTEM PERFORMANCE CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNITS
ELI	Linearity Error Integral	V_{EEA}, V_{EED}, I_{REF} = Typ.	—	0.2	%FS
ELD	Linearity Error Differential	V_{EEA}, V_{EED}, I_{REF} = Typ.	—	0.2	%FS
IOF	Output Offset I	V_{EEA}, V_{EED} = Max SYNC = BLANK = 0, FH = BRT = 1	—	±10	μA
EG	Abs. Gain Error	V_{EEA}, V_{EED}, I_{REF} = Typ.	—	±5	%FS
TCG	Gain Error Tempco		—	±0.024	%FS/°C
BWR	Ref. Bandwidth -3dB	ΔV_{REF} = 1mV	1		MHz
DP	Differential Phase	4 x NTSC	—	1.0	Deg.
DG	Differential Gain	4 x NTSC	—	2.0	%
PSRR	Power Supp. Rej. Ratio	V_{EEA}, V_{EED}, I_{REF} = Typ.(1)	—	45	dB
PSS	Power Supp. Sensitivity	V_{EEA}, V_{EED}, I_{REF} = Typ.(2)	—	120	uV/V
GC	Peak Glitch Charge	Registered ModeTyp.(3,4)	—	800	f_C
GI	Peak Glitch Current	Registered Mode	—	1.2	mA
GE	Peak Glitch Energy	Registered Mode(4)	—	30	pV-Sec
FT_C	Clock Feedthrough	Data Constant(5)	—	-50	dB
FT_D	Data Feedthrough	Clock Constant(5)	—	-50	dB

NOTES:

1. 20kHz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
2. 6Hz, ±0.3V ripple superimposed on V_{EEA}, V_{EED}; dB relative to full gray scale.
3. $f_{Coulombs}$ = microamps x nanoseconds.
4. 37.5Ω load. Because glitches tend to be symmetric, average glitch area approaches zero.
5. dB relative to full gray scale, 250MHz bandwidth limit.

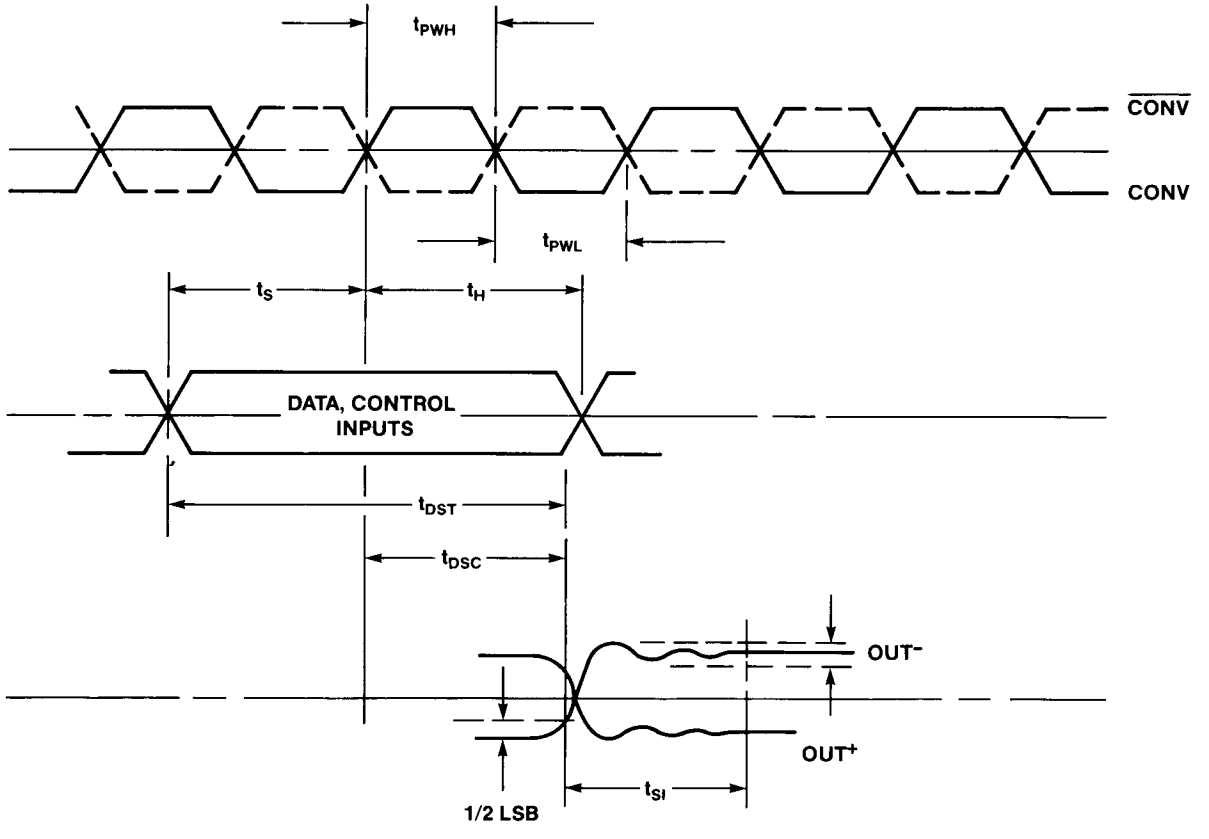


Figure 1. Timing Diagram

SSD75C18-004

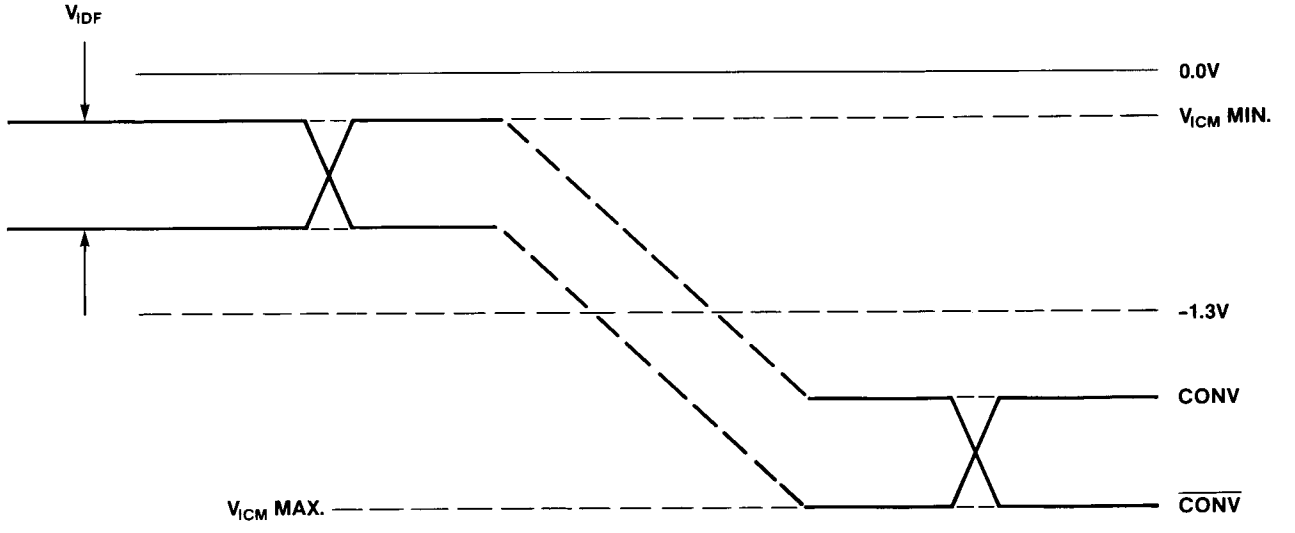


Figure 2. CONVert, $\overline{CONV}$ert Switching Levels IDT75C18 Only SSD75C18-005

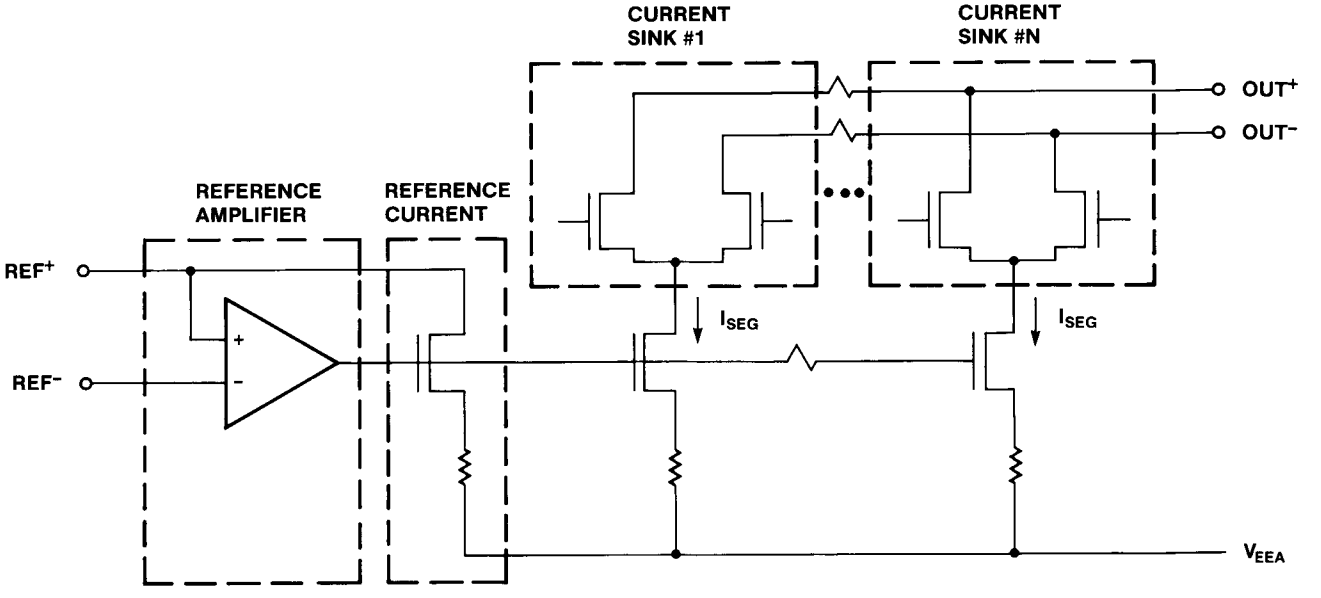


Figure 3. Equivalent Output Circuit SSD75C18-007

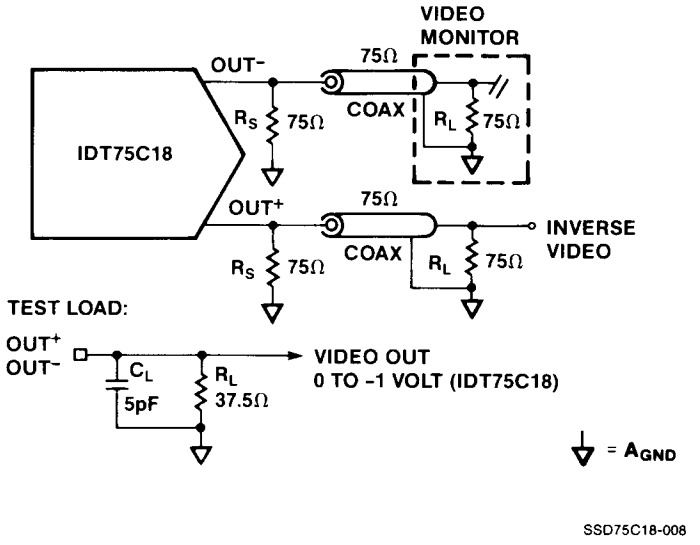


Figure 4. Standard Load Configuration

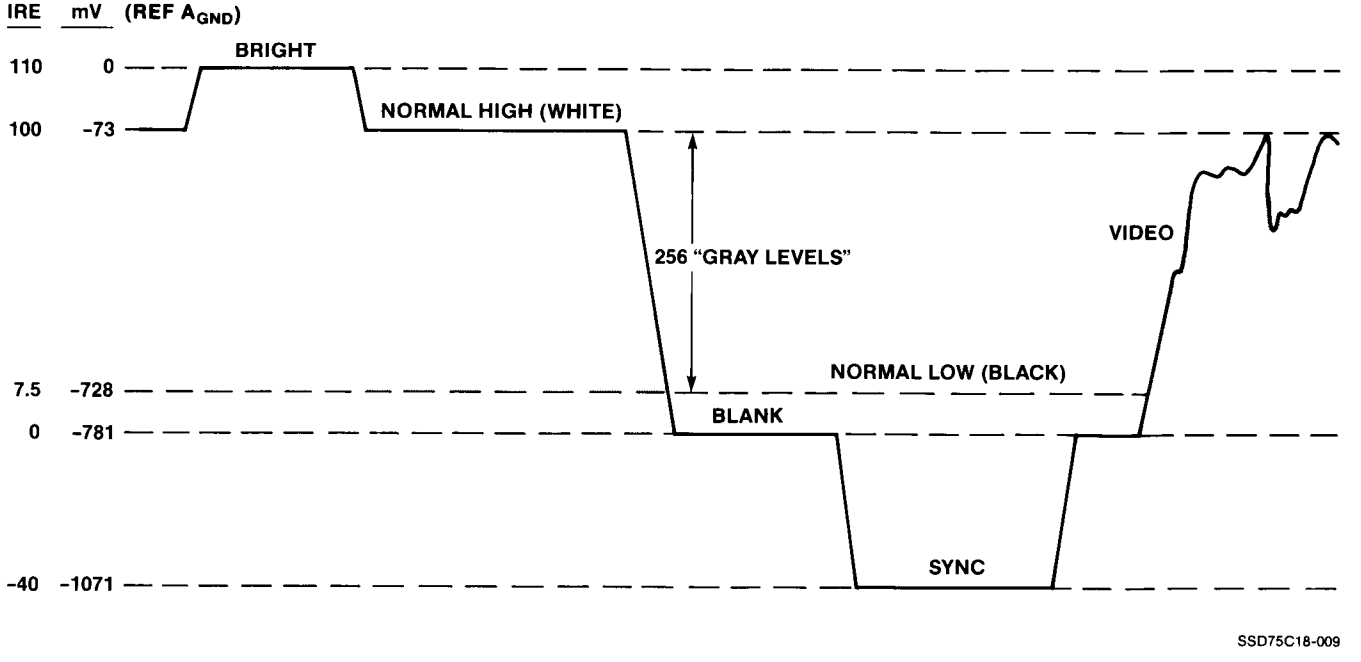


Figure 5. Video Output Waveform for Out- and Standard Load Configuration

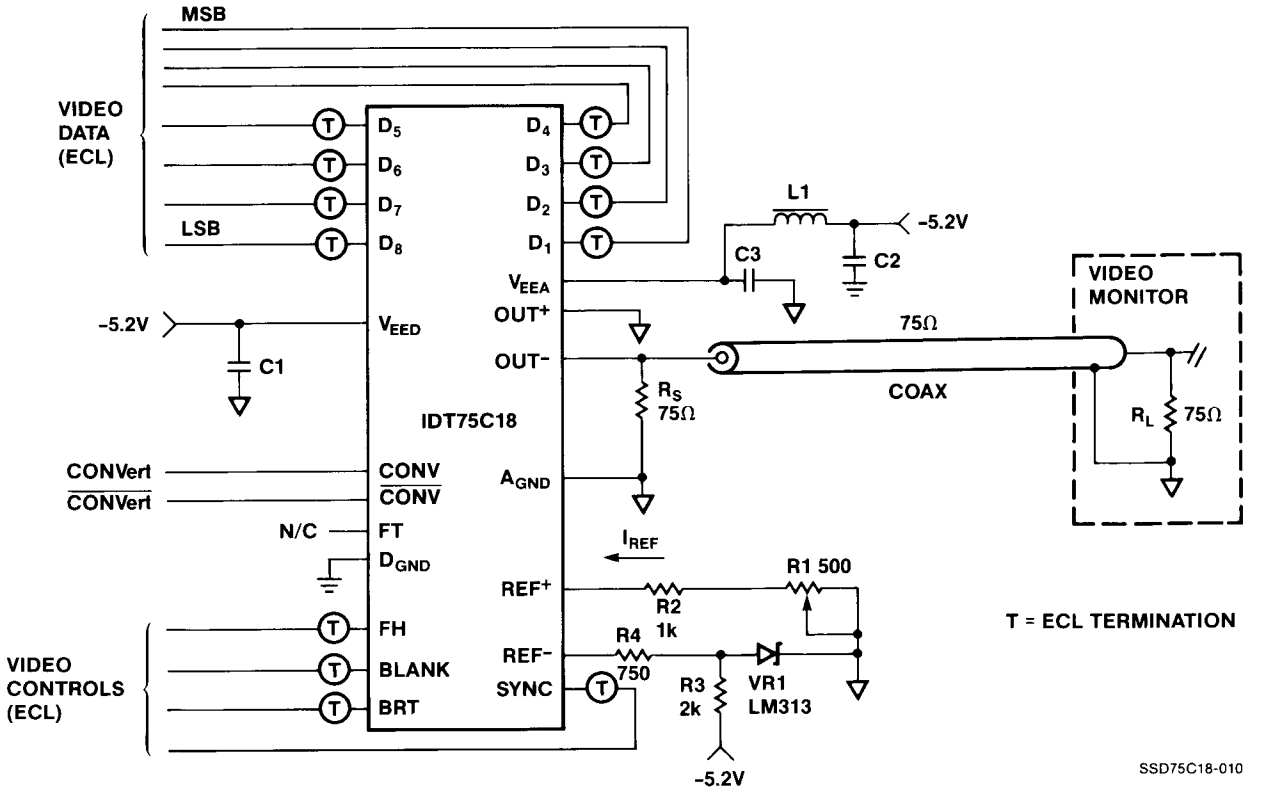


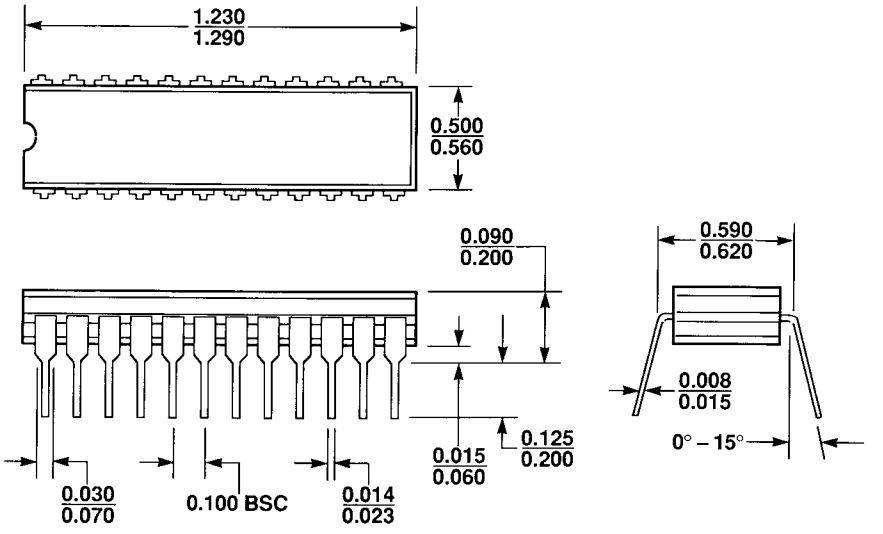
Figure 6. Typical Interface Circuit IDT75C18

PARTS LIST

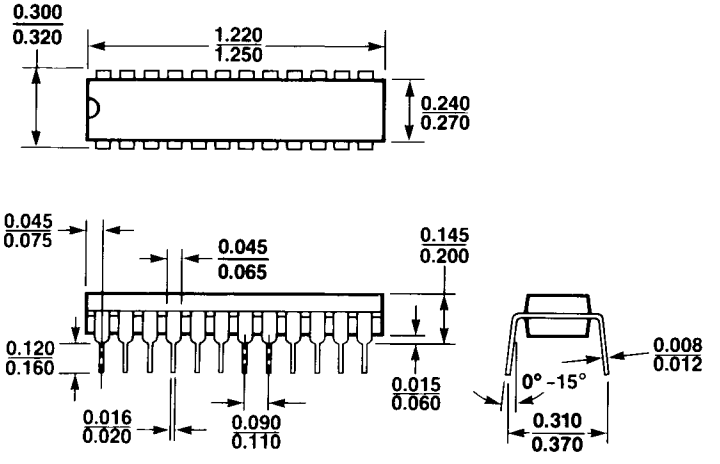
RESISTORS			
R1	1kΩ	Pot	10 Turn
R2	1.00kΩ	1/8W	1% Metal Film
R3	2.00kΩ	1/8W	1% Metal Film
R4	1.00kΩ	1/8W	1% Metal Film
CAPACITORS			
C1-C3	0.1μF	50V	Ceramic disc
INTEGRATED CIRCUITS			
U1	IDT75C18	D/A Converter	
VOLTAGE REFERENCES			
VR1	LM113 or LM313	Bandgap Reference	
INDUCTORS			
L1	Ferrite Bead Shield Inductor Fair-Rite P/N 2743001112 or Similar		

PACKAGE DIAGRAMS

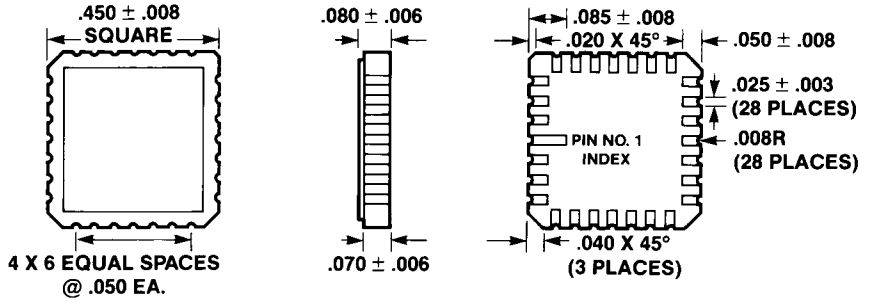
D24-3 24-PIN CERDIP (.600 mil)



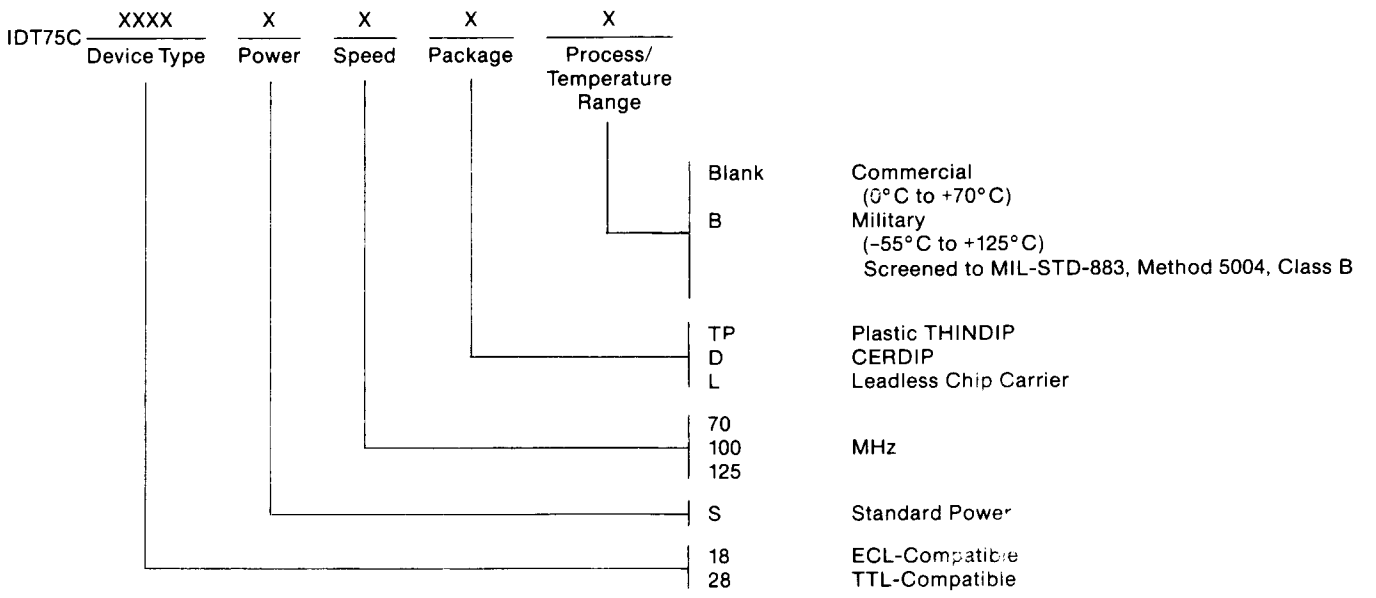
P24-2 24-PIN PLASTIC DIP (300 mil.)



L28-1 28-PIN LCC



ORDERING INFORMATION



IDT PROCESSING SUMMARY:

Maintaining the highest standards of quality in our monolithic hermetic products is the basis of IDT's standard manufacturing systems and procedures. IDT products begin with stringent design rules derived for use in high reliability programs. This is followed by a dedicated commitment to reliable workmanship as well as rigid controls throughout wafer fab, device assembly and electrical test, all of which are designed to produce products that are inherently reliable.

SCREENING FLOW — METHOD 5004

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal visual	2010 Condition B	100%
High-temperature storage	1008 Condition C	100%
Temperature cycle	1010 Condition C	100%
Constant acceleration	2001 Condition E (Y_1 only)	100%
Hermeticity	1014	
Fine	Condition A or B	100%
Gross	Condition C	100%
Burn-In		
Pre-burn-in electrical	Per applicable device specifications at T_A = +25°C	100%
Burn-in	MIL-STD-883 Grade Product	
	Method 1015, Condition D	100%
	Standard Grade Product	
	48 hours minimum to same burn-in conditions as Military Grade Product	100%
Final Electrical Tests[1]	5004	
Static (dc)	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A = +25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A = +25°C nominal power supply	100%
Percent Defective Allowable (PDA)	Method 5004	
Calculated at post burn-in	Military Grade	5%
@ T_A = +25°C	Standard Grade	10%
Quality Conformance	5005 Sample section as applicable	Sample
External Visual	2009 Per IDT or customer specification	100%

NOTE:

1. Commercial Grade Products are sample tested to the applicable temperature extremes.

All military grade products are manufactured and screened to the demanding requirements of MIL-STD-883, Method 5004, Class B. Commercial and industrial grade products differ from military grade only in burn-in time and electrical test temperature

IDT supplies a full line of military grade products completely screened to the Class B criteria of Method 5004, with inspection lots tested to the Quality Conformance Requirements of Method 5005 as shown. This includes 100% 160-hour burn-in at T_A = +125°C (or equivalent) per Method 1015. Cond. D, followed by 100% temperature testing of all DC, AC and functional characteristics over the full -55°C to +125°C temperature range.

Samples of the military grade products which have been processed to Method 5004 100% screening requirements are submitted to the Quality Conformance inspection requirements of MIL-STD-883. These Quality Conformance Inspections are performed to the specific requirements of Method 5005 Group A (electrical), Group B (mechanical), Group C (chip integrity), and Group D (package environmental integrity).

Documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

Specification of IDT monolithic hermetic products will ensure the user not only of high performance products, but also components tested to meet stringent reliability requirements.

QUALITY CONFORMANCE TESTING

Per MIL-STD-883, Method 5005, Class B

SCREEN	TEST METHOD	LEVEL
Quality Conformance Sample Tests	Group A (Electrical Tests)	Sample
	Group B (Mechanical Tests)	Sample
	Group C (Chip Integrity Tests)	Sample
	Group D (Module Integrity Tests)	Sample

For special customer specifications or Quality requirements beyond Class B levels of MIL-STD-883, such as SEM analysis, X-Ray, or other screening flows to meet specific user needs, contact your local IDT sales office.

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