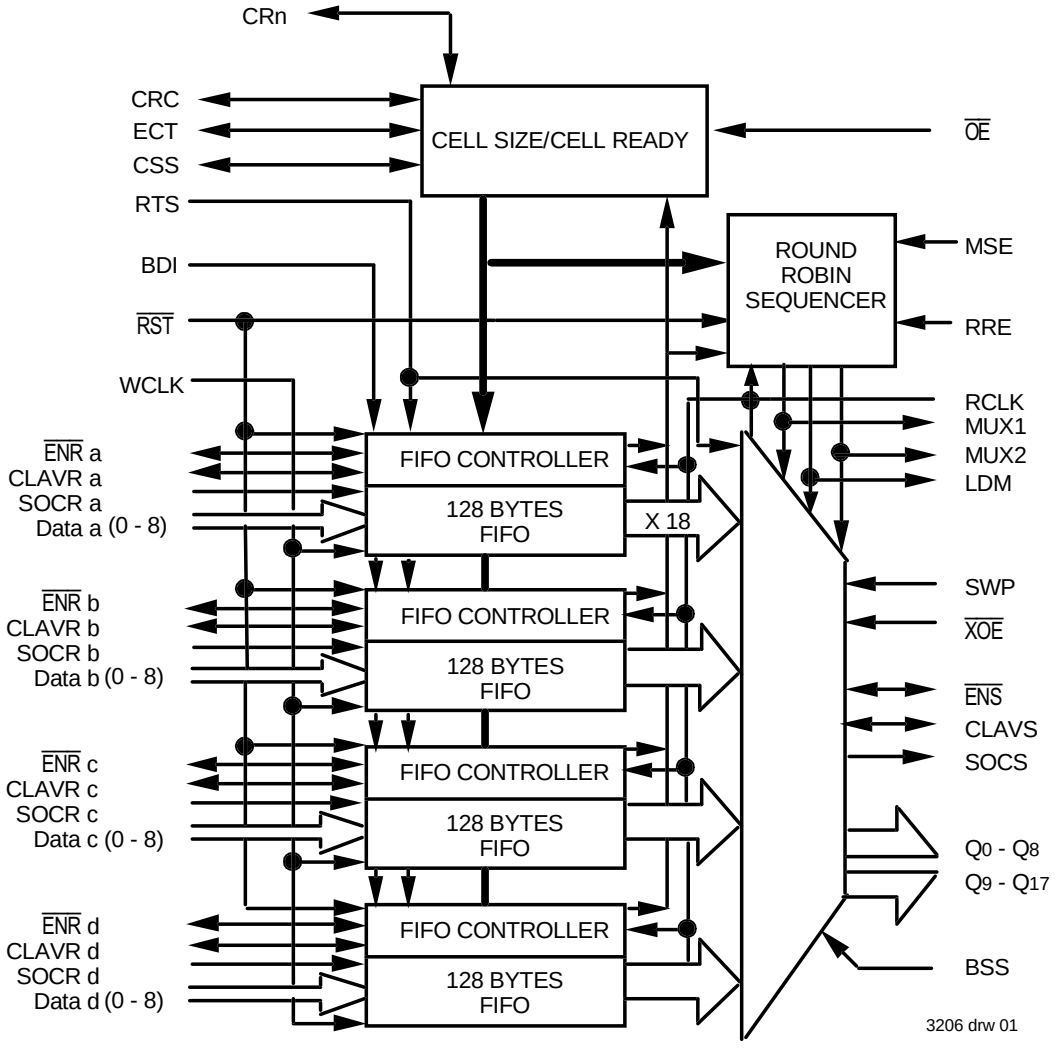
UTOPIAFIFO™ 4-PORT (128 X 9 X 4) MULTIPLEXER-FIFO

IDT77305

Features

- Four Independent Input 128 x9 FIFO Queues
- Nine bit wide input FIFOs
- Single selectable 9 or 18 bit output bus
- "UtopiaRx" or "UtopiaTx" Utopia compliant interface signaling options
- Separate clocks for input and output
- Selectable Automatic byte insertion for 8-bit Receive Utopia to 16-bit Receive Utopia compliance
- Four 155Mbs ATM input channels can be consolidated into a single 622Mbs channel with no additional glue logic
- Maximum through put per device over 1.4Gbps
- In a building block configuration multiple input channels can be multiplexed onto a 32, 64 or 128 bit bus.
- User programmable:
  - *byte insert/delete, UtopiaTx/UtopiaRx mode, master/slave configuration, byte swapping*
- Selectable Round Robin Sequencer output control
- Data clock rates to 80 MHz; access times 8.5 ns
- 100-pin TQPF package
- Separate cell ready signals for each FIFO and cell ready composite signal
- End of cell transfer flag

Functional Block Diagram



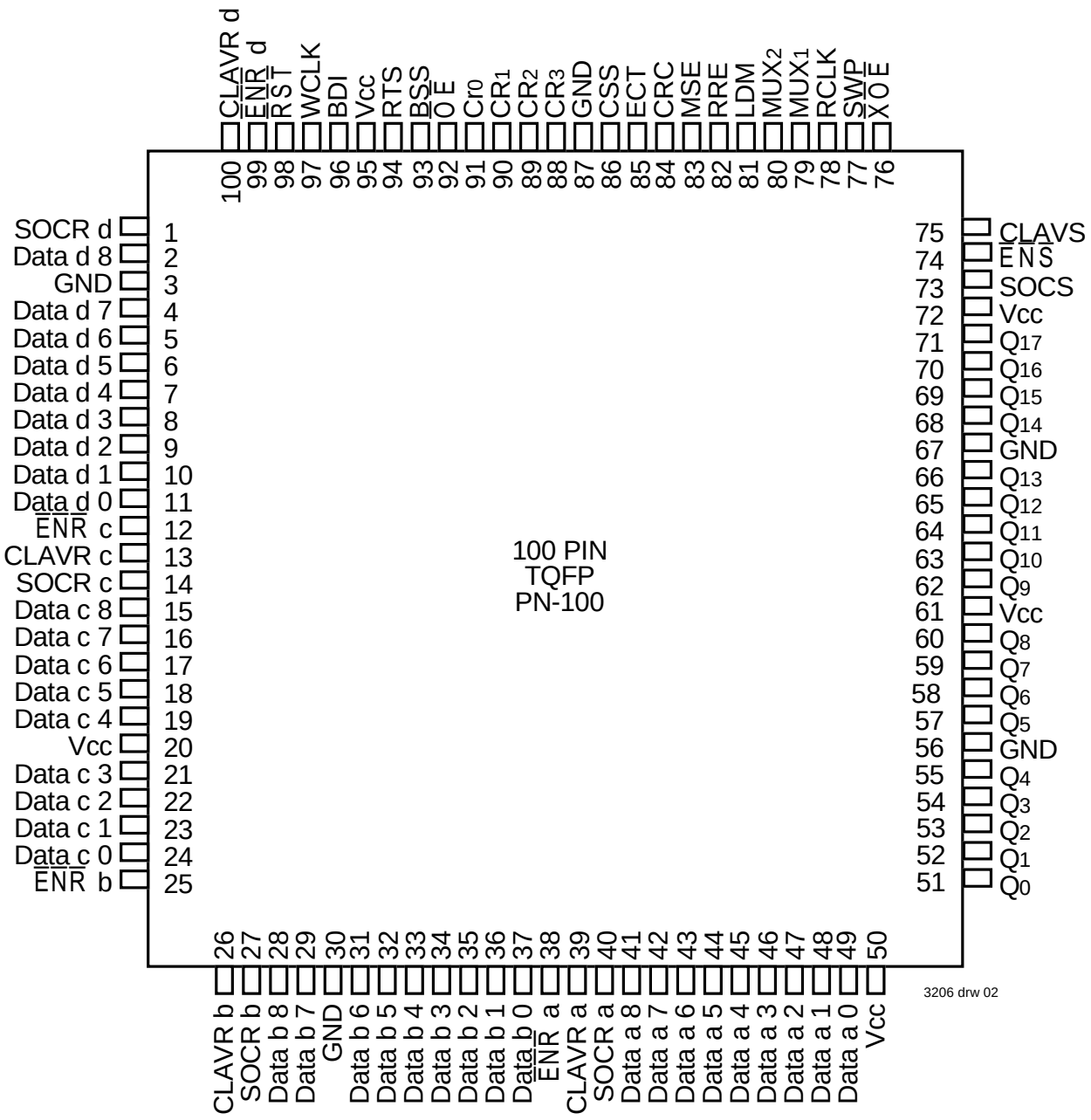
MARCH 2001

General Description

The IDT77305 UtopiaFIFO is a high-speed, low power, four to one, muxed FIFO with multiple programmable modes of operation. The IDT77305 can be used as a stand alone device or as a building block element. Within the UtopiaFIFO, the input FIFOs act as intermediate queues for the input streams to allow synchronization with a common output stream (see Functional Block Diagram). Each of the four input synchronous (clocked) FIFOs are 64 words (128 bytes) in depth. Separate input and output clocks are supported to 80 MHz. As a stand alone element four independent 9-bit input streams are concentrated onto one selectable 9 or 18-bit output bus. The Bus Size Select pin (BSS) determines the desired output bus width. In a building block configuration, multiple devices can be used to multiplex larger numbers of input streams onto output buses greater than 18 bits. The principle application is in ATM networking based systems, but can be used in any data or telecommunications application requiring the merging of independent data streams into a single output.

FIFO selection for data output can be made internally via a round robin which sequentially selects one of the four FIFOs. Alternatively, external

Pin Configuration



3206 drw 02

Pin Description

Name	I/O	Description
BDI	I	Byte Deletion/Insertion. BDI = "1" insert byte 6 or delete byte 5, BDI = "0" no change to bytes 5 or 6 (see Table 4).
BSS	I	Bus Size Selection. BSS = "0" 18-bit output bus, BSS = "1" 9-bit output bus.
CLAVR a	I/O	Cell Available (FIFO-a)—Receive side. Rx mode: CLAVR notifies UtopiaFIFO an entire cell is available for transfer. It is an input signal. Tx mode: CLAVR notifies sending agent the UtopiaFIFO can accept an entire cell. It is an output signal.
CLAVR b	I/O	Cell Available (FIFO-b)—Receive side. Rx mode: CLAVR notifies UtopiaFIFO an entire cell is available for transfer. It is an input signal. Tx mode: CLAVR notifies sending agent the UtopiaFIFO can accept an entire cell. It is an output signal.
CLAVR c	I/O	Cell Available (FIFO-c)—Receive side. Rx mode: CLAVR notifies UtopiaFIFO an entire cell is available for transfer. It is an input signal. Tx mode: CLAVR notifies sending agent the UtopiaFIFO can accept an entire cell. It is an output signal.
CLAVR d	I/O	Cell Available (FIFO-d)—Receive side. Rx mode: CLAVR notifies UtopiaFIFO an entire cell is available for transfer. It is an input signal. Tx mode: CLAVR notifies sending agent the UtopiaFIFO can accept an entire cell. It is an output signal.
CLAVS	I/O	Cell Available (sender side). Notifies controlling agent a cell is available.
CR0 - CR3	I/O	Cell Ready, FIFO-n. For $\overline{OE}$ LOW and $\overline{RST}$ HIGH, CR-n is an output (HIGH if FIFO-n has a cell available, LOW if no cell available). For $\overline{RST}$ and $\overline{OE}$ both HIGH, CR-n are tri-stated. For $\overline{RST}$ LOW and $\overline{OE}$ HIGH, CRn are inputs. See Table 1.
CRC	I/O	Cell Ready Composite. For $\overline{OE}$ LOW and $\overline{RST}$ HIGH, CRC is an output (HIGH if any FIFO has cell available). For $\overline{RST}$ and $\overline{OE}$ both HIGH, CRC is tri-stated. For $\overline{RST}$ LOW AND $\overline{OE}$ HIGH, CRC is a cell size selection input [MSB].
CSS	I/O	Cell Size selection for (MSB-2).
DATA a	I	9-bit data bus inputs for FIFO-a.
DATA b	I	9-bit data bus inputs for FIFO-b.
DATA c	I	9-bit data bus inputs for FIFO-c.
DATA d	I	9-bit data bus inputs for FIFO-d.
ECT	I/O	End Cell Transfer. For $\overline{OE}$ LOW and $\overline{RST}$ HIGH, ECT is an output asserted one cycle before end of current cell transfer. ECT goes LOW upon cell transfer completion. For $\overline{RST}$ and $\overline{OE}$ both HIGH, ECT is tri-stated. For $\overline{RST}$ LOW and $\overline{OE}$ HIGH, ECT is a cell size selection input [MSB-1].
$\overline{ENR}$ a	I/O	Enable (FIFO-a)—Receive Side. Rx mode: $\overline{ENR}$ is an output initiating data transfer to the receiver (input) side. Tx mode: $\overline{ENR}$ is an input initiating data transfer to the receiver side.
$\overline{ENR}$ b	I/O	Enable (FIFO-b)—Receive Side. Rx mode: $\overline{ENR}$ is an output initiating data transfer to the receiver (input) side. Tx mode: $\overline{ENR}$ is an input initiating data transfer to the receiver side.
$\overline{ENR}$ c	I/O	Enable (FIFO-c)—Receive Side. Rx mode: $\overline{ENR}$ is an output initiating data transfer to the receiver (input) side. Tx mode: $\overline{ENR}$ is an input initiating data transfer to the receiver side.
$\overline{ENR}$ d	I/O	Enable (FIFO-d)—Receive Side. Rx mode: $\overline{ENR}$ is an output initiating data transfer to the receiver (input) side. Tx mode: $\overline{ENR}$ is an input initiating data transfer to the receiver side.
$\overline{ENS}$	I/O	Enable (sender side). Enables current word transfer. Rx mode: an input to UtopiaFIFO. Tx mode: an output to receiving system.
GND	—	Logic and supply ground.

3206 tbl 01

Pin Description (con't.)

Name	I/O	Description
LDM	I/O	Load Mux. RRE = "1" and MSE = "1": LDM is an output telling Slave to latch the Mux select address on the next clock cycle, RRE = "0" and MSE = "1": LDM is an input that latches the Mux address for the next cell transfer.
MSE	I	Master/Slave Enable. MSE = "1" master mode, MSE = "0" slave mode.
MUX1	I/O	MUX1 address. With RRE = "1": MUX1 outputs FIFO address LSB: with RRE = "0": MUX1 is input address LSB of selected FIFO.
MUX2	I/O	MUX2 address. With RRE = "1": MUX2 outputs FIFO address MSB: with RRE = "0": MUX2 is input addre MSB of selected FIFO.
$\overline{OE}$	I	Output Enable. In combination with RST, it sets CR0-3 as either output cell available signals, input cell size values or tri-state outputs (see Table 1).
Qn	O	Data bus output.
RCLK	I	Data read clock.
RRE	I	Round Robin Enable. RRE = "1" round robin sequencer enabled. RRE = "0" sets mux select lines and LDM as inputs to provide user control over selected FIFO.
$\overline{RST}$	I	Reset. Clears all FIFO memory locations, read/write pointers, RR sequencer.
RTS	I	Receive/Transmit mode Selection RTS = "0" Utopia Rx mode, RTS = "1" UtopiaTx mode.
SOCR a	I	Start Of Cell (FIFO-a)—Receive side. Active on first byte when CLAVR and $\overline{ENR}$ are asserted. After first byte read, SOCR is ignored until full cell has been received.
SOCR b	I	Start Of Cell (FIFO-b)—Receive side. Active on first byte when CLAVR and $\overline{ENR}$ are asserted. After first byte read, SOCR is ignored until full cell has been received.
SOCR c	I	Start Of Cell (FIFO-c)—Receive side. Active on first byte when CLAVR and $\overline{ENR}$ are asserted. After first byte read, SOCR is ignored until full cell has been received.
SOCR d	I	Start Of Cell (FIFO-d)—Receive side. Active on first byte when CLAVR and $\overline{ENR}$ are asserted. After first byte read, SOCR is ignored until full cell has been received.
SOCS	O	Start of Cell (sender side). Assertion: first word is currently on output bus.
SWP	I	Swap Enable. Swaps high byte and low byte of current word. SWP = "0": First word is placed in lower byte (Q0-Q7) of 16-bit output (little endian), SWP = "1": first word is placed in upper byte (Q9-Q16) of 16-bit output (big endian Utopia compliant cell format).
V_{CC}	—	Logic and supply V_{CC}.
WCLK	I	Data write clock.
$\overline{XOE}$	I	Data bus output enable.

3206 tbl 02

Absolute Maximum Ratings

Symbol	Rating	Commercial	Industrial	Unit
V_{TERM}	Terminal Voltage with respect to ground	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-40 to +85	C
T-Bias	Temperature under Bias	-55 to +155	-55 to +155	C
T-STG	Storage Temperature	-55 to +155	-55 to +155	C
I_{OUT}	DC Output Current	50	50	mA

3206 tbl 03

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	V_{CC}+0.3	V
V_{IL}	Input Low Voltage Commercial	-0.3	—	0.8	V

3206 tbl 04

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	-1	—	1	µA
I_{LO}	Output Leakage Current	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH}=-4mA@2.4V	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL}=+4mA@0.4V	—	—	0.4	V
I_{CC1}	Active Power Supply Current	—	—	150	mA

3206 tbl 05

Capacitance

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

3206 tbl 06

AC Electrical Characteristics[1]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C)

RX Mode		Commercial				
		77305L12		77305L15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CLAVS}	Cell Available Set-up Time, CLAVR to WCLK	5	—	5	—	ns
t_{CLAVH}	Cell Available Hold Time, WCLK to CLAVR	0	—	0	—	ns
t_{ENSS}	Enable Set-up Time, $\overline{ENS}$ to RCLK	4.5	—	5	—	ns
t_{ENSH}	Enable Hold Time, RCLK to $\overline{ENS}$	0	—	0	—	ns
t_{PEN}	WCLK to $\overline{ENR}$	—	8	—	10	ns
t_{PCLAV}	RCLK to CLAVS	—	10	—	10	ns

3206 tbl 07

TX Mode		Commercial				
		77305L12		77305L15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{ENRS}	Enable Set-up Time, $\overline{ENR}$ to WCLK	4.5	—	5	—	ns
t_{ENRH}	Enable Hold Time, WCLK to $\overline{ENR}$	0	—	0	—	ns
t_{CLAVS}	Cell Available Set-up Time, CLAVS to RCLK	5	—	5	—	ns
t_{CLAVH}	Cell Available Hold Time, RCLK to CLAVS	0	—	0	—	ns
t_{PCLAV}	WCLK to CLAVS	—	10	—	10	ns
t_{PENS}	RCLK to $\overline{ENS}$	—	10	—	10	ns

3206 tbl 08

(Industrial: Vcc = 5V ± 10%, TA = -40°C to +85°C)

RX Mode		Industrial				
		77305L12		77305L15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{CLAVS}	Cell Available Set-up Time, CLAVR to WCLK	5	—	5	—	ns
t_{CLAVH}	Cell Available Hold Time, WCLK to CLAVR	0	—	0	—	ns
t_{ENSS}	Enable Set-up Time, $\overline{ENS}$ to RCLK	5	—	5	—	ns
t_{ENSH}	Enable Hold Time, RCLK to $\overline{ENS}$	0	—	0	—	ns
t_{PENS}	WCLK to $\overline{ENR}$	—	10	—	10	ns
t_{PCLAV}	RCLK to CLAVS	—	10	—	10	ns

3206 tbl 09

TX Mode		Industrial				
		77305L12		77305L15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
t_{ENRS}	Enable Set-up Time, $\overline{ENR}$ to WCLK	4.5	—	5	—	ns
t_{ENRH}	Enable Hold Time, WCLK to $\overline{ENR}$	0	—	0	—	ns
t_{CLAVS}	Cell Available Set-up Time, CLAVS to RCLK	5	—	5	—	ns
t_{CLAVH}	Cell Available Hold Time, RCLK to CLAVS	0	—	0	—	ns
t_{PCLAV}	RCLK to CLAVS	—	10	—	10	ns
t_{PENS}	RCLK to $\overline{ENS}$	—	10	—	10	ns

3206 tbl 10

AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1

3240 tbl 11

AC Test Load

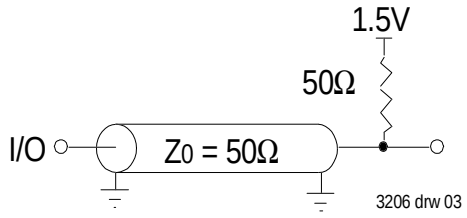


Figure 1: AC Test Load

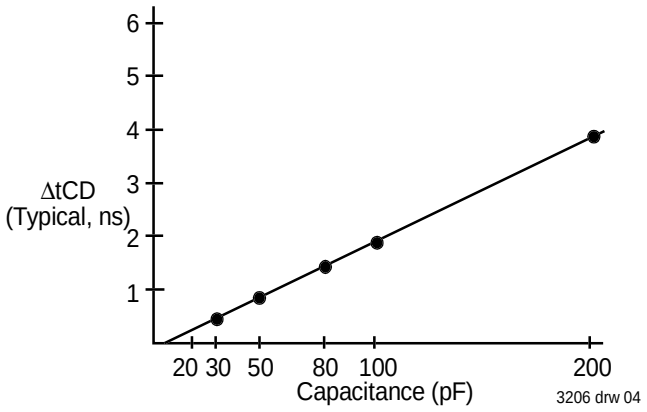


Figure 2: Lumped Capacitive Load, Typical Derating

AC Electrical Characteristics[1]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C)

Rx Mode		Commercial				
		77305L12		77305L15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	80	—	66.7	MHz
t_A	Data Access Time	2	10	2	10	ns
t_{CLK}	Clock Cycle Time	12.5	—	15	—	ns
t_{CLKH}	Clock High Time	5	—	6	—	ns
t_{CLKL}	Clock Low Time	5	—	6	—	ns
t_{RS}	Reset Pulse Width[1]	12	—	15	—	ns
t_{RSS}	Reset Set-up Time	12	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	14	—	ns
t_{PRS}	Reset to Output Time	—	8	—	10	ns
t_{SKEW1}	Skew time between RCLK and WCLK[2]	11	—	14	—	ns
t_{SKEW2}	Skew time between WCLK and RCLK[2]	11	—	14	—	ns
t_{DS}	Data Set-up Time, Data to WCLK	5	—	5	—	ns
t_{DH}	Data Hold Time, WCLK to DATA	0	—	0	—	ns
t_{SOCS}	SOCR Set-up Time, SOCR to WLCK	4.5	—	5	—	ns
t_{SOCH}	SOCR Hold Time, WCLK to SOCR	0	—	0	—	ns
t_{CSS}	Cell Size Set-up Time (CRC, ECT, CSS or CRn to $\overline{RST}$)	6	—	8	—	ns
t_{CSH}	Cell Size Hold Time (CRC, ECT, CSS, CRn to $\overline{RST}$)	0	—	0	—	ns
t_{LDMS}	Load MUX Set-up Time, LDM to RCLK	5	—	5	—	ns
t_{LDMH}	Load MUX Hold Time, RCLK to LDM	0	—	0	—	ns
t_{MUXS}	MUX Set-up Time, MUX to RCLK	5	—	5	—	ns
t_{MUXH}	MUX Hold Time, RCLK to MUX	0	—	0	—	ns
t_{PSOC}	RCLK to SOCS	—	10	—	10	ns
t_{PCS}	Cell Status Response, RCLK to CRC, ECT, CSS or CRn	—	10	—	10	ns
t_{PLDM}	RCLK to LDM (as RREN=1)	—	10	—	10	ns
t_{PMUX}	RCLK to MUX (as RREN-1)	—	10	—	10	ns
t_{XOE}	$\overline{XOE}$ to Qn Valid	1	10	1	10	ns
t_{OE}	$\overline{OE}$ to CRC, ECT, CSS or CRn	1	10	1	10	ns
t_{XOHZ}	$\overline{XOE}$ to Qn in High Z[2]	—	10	—	10	ns
t_{OHZ}	$\overline{OE}$ to CRC, ECT, CSS or CRn in High Z[2]	—	10	—	10	ns
t_{XOLZ}	$\overline{XOE}$ to Qn in Low Z[2]	0	—	0	—	ns
t_{OLZ}	$\overline{OE}$ to CRC, ECT, CSS or CRn in Low Z[2]	0	—	0	—	ns

3206 tbl 12

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC Electrical Characteristics[1]

(Industrial: Vcc = 5V ± 10%, TA = -40°C to +85°C)

Rx Mode		Industrial				
		77305L12		77305L15		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	80	—	66.7	MHz
t_A	Data Access Time	2	10	2	10	ns
t_{CLK}	Clock Cycle Time	12.5	—	15	—	ns
t_{CLKH}	Clock High Time	5	—	6	—	ns
t_{CLKL}	Clock Low Time	5	—	6	—	ns
t_{RS}	Reset Pulse Width[1]	12	—	15	—	ns
t_{RSS}	Reset Set-up Time	12	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	14	—	ns
t_{PRS}	Reset to Output Time	—	10	—	10	ns
t_{SKEW1}	Skew time between RCLK and WCLK[2]	11	—	14	—	ns
t_{SKEW2}	Skew time between WCLK and RCLK[2]	11	—	14	—	ns
t_{DS}	Data Set-up Time, Data to WCLK	5	—	5	—	ns
t_{DH}	Data Hold Time, WCLK to DATA	0	—	0	—	ns
t_{SOCS}	SOCR Set-up Time, SOCR to WLCK	5	—	5	—	ns
t_{SOCH}	SOCR Hold Time, WCLK to SOCR	0	—	0	—	ns
t_{CSS}	Cell Size Set-up Time (CRC, ECT, CSS or CRn to $\overline{RST}$)	6	—	8	—	ns
t_{CSH}	Cell Size Hold Time (CRC, ECT, CSS, CRn to $\overline{RST}$)	0	—	0	—	ns
t_{LDMS}	Load MUX Set-up Time, LDM to RCLK	5	—	5	—	ns
t_{LDMH}	Load MUX Hold Time, RCLK to LDM	0	—	0	—	ns
t_{MUXS}	MUX Set-up Time, MUX to RCLK	5	—	5	—	ns
t_{MUXH}	MUX Hold Time, RCLK to MUX	0	—	0	—	ns
t_{PSOC}	RCLK to SOCS	—	10	—	10	ns
t_{PCS}	Cell Status Response, RCLK to CRC, ECT, CSS or CRn	—	10	—	10	ns
t_{PLDM}	RCLK to LDM (as RREN=1)	—	10	—	10	ns
t_{PMUX}	RCLK to MUX (as RREN=1)	—	10	—	10	ns
t_{XOE}	$\overline{XOE}$ to Qn Valid	1	10	1	10	ns
t_{OE}	$\overline{OE}$ to CRC, ECT, CSS or CRn	1	10	1	10	ns
t_{XOHZ}	$\overline{XOE}$ to Qn in High Z[2]	—	10	—	10	ns
t_{OHZ}	$\overline{OE}$ to CRC, ECT, CSS or CRn in High Z[2]	—	10	—	10	ns
t_{XOLZ}	$\overline{XOE}$ to Qn in Low Z[2]	0	—	0	—	ns
t_{OLZ}	$\overline{OE}$ to CRC, ECT, CSS or CRn in Low Z[2]	0	—	0	—	ns

3206 tbl 13

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

mux select lines provide user control of FIFO selection.

Functional Description

SINGLE DEVICE OPERATION

The two programmable interface signaling modes of operation are Utopia Receive (UtopiaRx) and Utopia transmit (UtopiaTx). Both modes can concentrate four nine-bit channels (up to 720 Mbs) to one 18-bit output channel (up to 1.44 Gbs). In a building block implementation, multiple streams over 10 Gbs (with 32, 64, or 128 bit buses) can be obtained. Mode one, UtopiaRx, follows UtopiaRx protocols; and Mode two, UtopiaTx, follows UtopiaTx protocols. The Receive/Transmit Select (RTS) pin sets the UtopiaFIFO into the desired mode. The difference between these modes relates to the Utopia specification for signal handshaking. In UtopiaRx mode, the device receiving data controls the data flow through ENR (or $\overline{ENS}$ on the output side). In UtopiaTx mode, the device sending data controls the data flow through ENR (or $\overline{ENS}$ on the output side). This is described in the Utopia ATM-PHY Level2 version 1 Document.

In either mode, data is transferred in "cells". ATM cell size is 53 bytes. However, for applications other than ATM the cell size can be programmed through the cell size register. Programming this register allows cell sizes from 8 bytes to 128 bytes. With $\overline{RST}$ and $\overline{OE}$ both HIGH, CR(0-3), CSS, ECT and CRC are cell size inputs. The default cell size of 53 bytes is selected when both $\overline{RST}$ and $\overline{OE}$ are LOW. In either case the values are latched on the rising edge of $\overline{RST}$. To load a specific cell size value from 8 bytes to 128 bytes use CR(0-3), CSS, ECT and CRC as inputs with $\overline{RST}$ and $\overline{OE}$ both HIGH. The bit order is CR0, CR1, CR2, CR3, CSS, ECT, CRC, with CR0 being LSB and CRC being MSB. Set all input pins LOW to program a cell size of 128 bytes. See Table 1 for cell size programming truth table.

Control signals for the input data (receive) side consists of CLAVR, $\overline{ENR}$ and SOCR (see Table 2a). Prior to cell transfer, the controlling agent (data source for transmit mode, data destination for receive mode) is notified a cell transfer can take place through the assertion of the CLAVR signal. Each data transfer of a cell is completed by assertion of $\overline{ENR}$. The $\overline{ENR}$ signal is supplied by the controlling agent. During the first data byte transfer, the data source asserts SOCR to mark the beginning of the cell. Data transfer continues until the cell is completed. When the cell size is reached, further writes are blocked until new CLAVR and SOCR signals are received.

$\overline{OE}$	$\overline{RST}$	FUNCTION
1	0	CR(0-3), CSS, ECT, CRC are cell size inputs
0	0	sets default cell size of 53 bytes
1	1	CR(0-3), CSS ECT, CRC are tristated
0	1	CR(0-3), CSS, ECT, CRC are outputs CR(0-3) = "0" then no cell in FIFO = "1" then cell in FIFO CSS = no function: don't care ECT asserts one cycle before the end of a cell transfer CRC = "0" then no FIFO(s) has a cell CRC = "1" then at least one FIFO has cell

3206 tbl 14

TABLE 1: Truth table for cell size programming
Note values are loaded on the rising edge of $\overline{RST}$

RXMODE

In UtopiaRx mode (see Figure 2a), $\overline{ENR}$ is an output to the sending device and assertion of $\overline{ENR}$ results in data writes to the UtopiaFIFO in a pipelined fashion. Once enabled, data is written on the following rising clock edge. CLAVR controls data from the sender side. While this signal remains HIGH, data is valid. If CLAVR goes LOW, data continues to be valid after cell transfer is started. After cell transfer begins, if $\overline{ENR}$ is deasserted, data writes halt until subsequent assertions (see Figures 3).

The I/O status of the output pins are listed in Table 3 for both UtopiaRx and UtopiaTx modes in either Master or Slave configuration. As a stand-alone device, the UtopiaFIFO has The I/O status of the output pins are listed in Table 3 for both UtopiaRx and UtopiaTx modes in either Master or Slave configuration. As a stand-alone device, the UtopiaFIFO has the same description as shown for a device in a master setting—the MSE signal is set HIGH (slave operation is described later in building block mode section).

In UtopiaTx mode, the CLAVS is an input to the UtopiaFIFO signaling a complete cell can be transferred. As the controlling agent, the UtopiaFIFO asserts an output signal, $\overline{ENS}$ to transfer data on the same rising clock edge (see Figure 6).

ADDITIONAL CONTROL SIGNALS—RX AND TX MODES

Three additional control signals provide added device functionality. The global reset ($\overline{RST}$) pin clears all register values. The byte swapping (SWP) pin provides the ability to swap byte positions on the output. SWP is a dynamic signal—once this signal is changed, output high and low bytes are swapped on the next clock cycle. If SWP is high the first byte of data is put in the upper byte of output bus, and if low the first byte is placed in the lower byte. SWP high will make the output bus Utopia compliant. The function is disabled when output bus size is set to 9-bits. The Byte Delete/Insert (BDI) pin enables byte delete/insert to comply with ATM bus matching. The input bus is Utopia compliant 9-bit bus with the output an 18-bit bus. Data is transferred to each FIFO in 53 byte cells. The Utopia spec defines 53 bytes per cell for 8-bit transfer and 54 bytes per cell for 16 bit transfer. Compatibility with 53 byte ATM cell formatting during bus matching is maintained. With the BDI selected, depending on the byte size and interface signaling mode, the UtopiaFIFO will automatically insert and/or delete dummy or header bytes according to Table 4; thus maintaining data integrity and Utopia specification compatibility. With BDI asserted HIGH, cell size is limited to 126 bytes. When output bus size is set to 9-bits, BDI must be deasserted LOW.

The round robin sequencer sequentially selects one of four FIFOs to output data. The sequencer is enabled by asserting the Round Robin Enable (RRE) HIGH. The sequencer will poll each FIFO in turn to determine which has data to send and selects the appropriate FIFO.

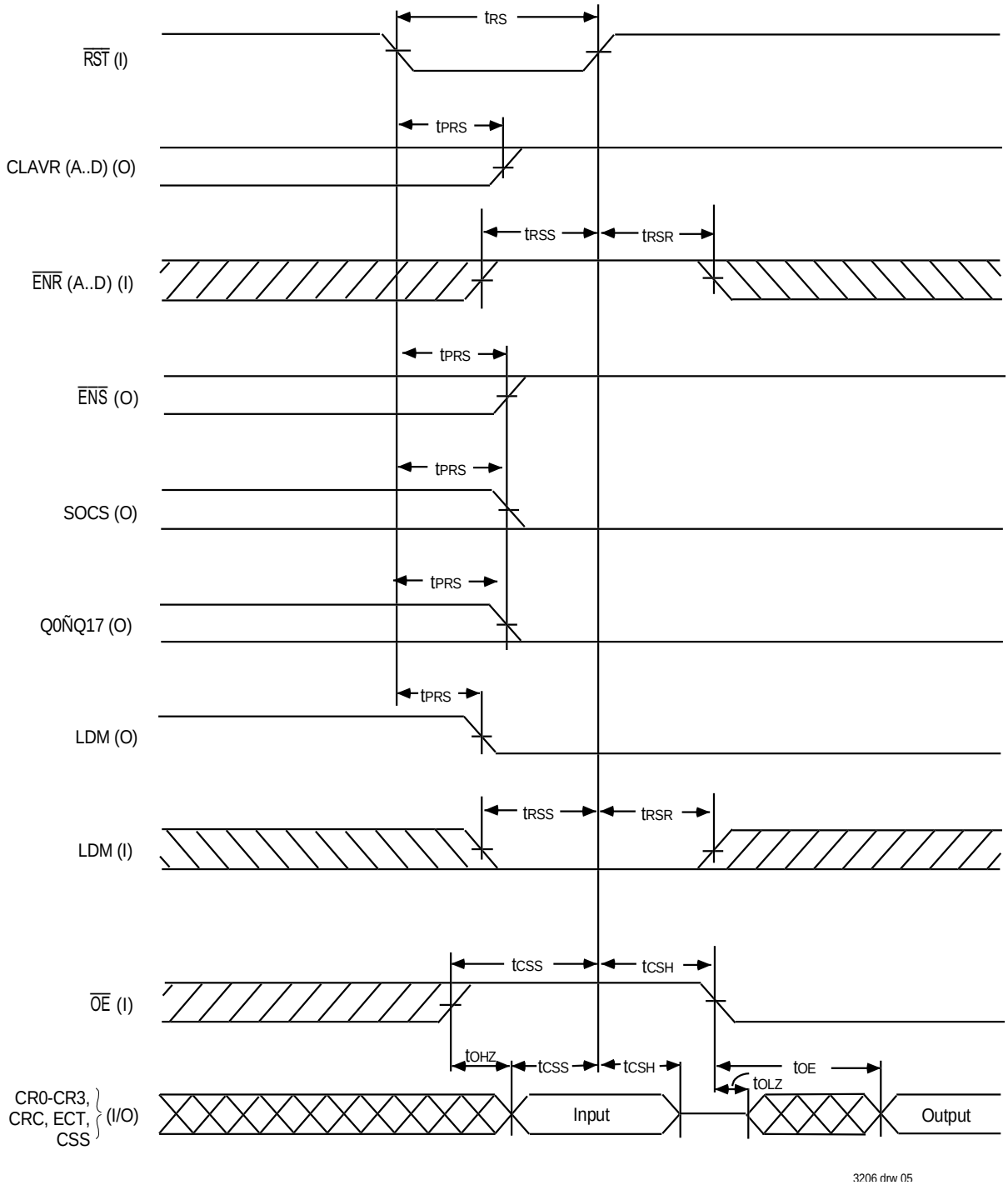


Figure 1a. Transmit Mode Reset Timing

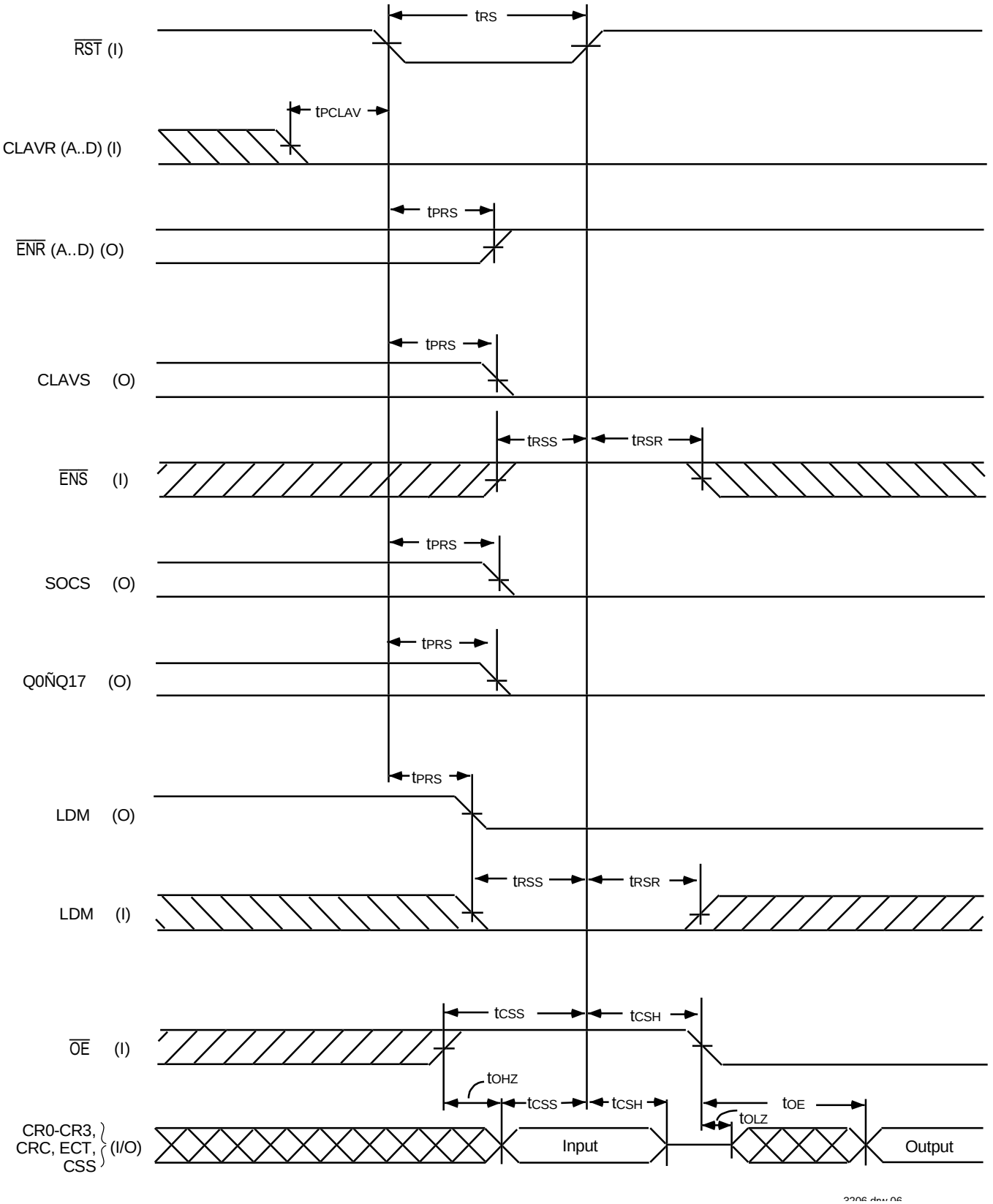


Figure 1b. Receive Mode Reset Timing

The selection process begins one cycle prior to the completion of the current FIFOs cell transfer (as defined by the Cell Size Register). On one cycle, the UtopiaFIFO determines if a FIFO has a cell and its identity. If a cell is ready, the counter will hold the value and present it to the output of the mux select lines prior to the last word transfer of the current cell and assert the output CLAVS signal. See Figure 7 for round robin state machine.

If the RRE signal is deasserted LOW, the mux select lines and LDM become inputs defining which FIFO will transfer data. Interrogation of the select signals will take place at the beginning of each clock cycle. Four cell ready pins (CR0-3) are provided so it can be determined if the port being polled has a cell ready to transfer. With $\overline{OE}$ set LOW, CR0-3 signals indicate cell available for the four FIFOs. If a particular FIFO has a complete cell ready for output, the appropriate CR pin is asserted HIGH. All four FIFOs cell ready signals are independent of each other. CR-0, 1, 2, 3, signal cell available status for FIFO-A, B, C, D respectfully. The Cell Ready Composite (CRC) signal is a composite of all CR-n signals. If any of the FIFOs have a cell available, CRC is asserted HIGH. CRC and CR(0-3) de-assert LOW on the last byte of the current cell transfer, if there is not another complete cell to transfer.

Once it has been determined that a particular FIFO has a cell to transfer the Load Mux (LDM) is asserted HIGH while that address is on

TABLE 2: Pin I/O status for Receiver and Sender Signals for Rx and Tx Modes

	Receiver (Input) I/O	
	RX	TX
CLAVR	I	O
$\overline{ENR}$	O	I
SOCR	I	I
Data	I	I
Clock	I	I

3206 tbl 15

	Receiver (Input) I/O	
	RX	TX
CLAVR	O	I
$\overline{ENR}$	I	O
SOCR	O	O
Data	O	O
Clock	I	I

3206 tbl 16

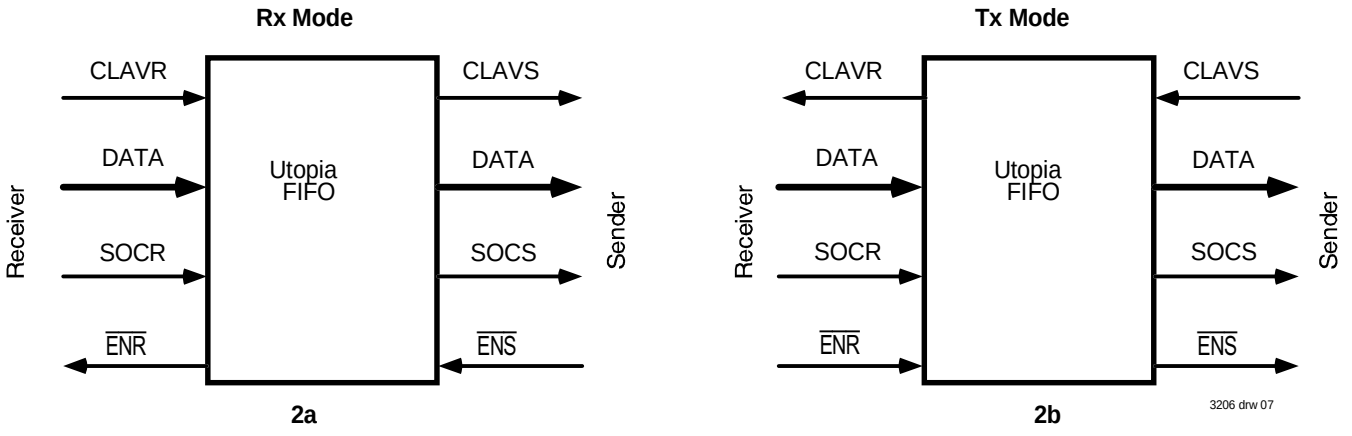


Figure 2. Signal and Data I/O Directions for Rx, Tx Modes.

the Mux1 and Mux 2 lines. This will latch the address. There must be a cell to transfer in the selected FIFO once LDM is asserted, as a new FIFO port address cannot be selected until a cell is read from the currently selected FIFO port. LDM is an input when RRE is LOW (disabled), regardless of the condition of MSE.

The End of Cell Transfer (ECT) flag asserts HIGH with SOCS on the first word of the cell. ECT will de-assert LOW on the fourth to last word of the cell.

Building Block Implementation

Combining more than four data flows and/or using larger bus widths is accomplished by using the device as a building block. Multiple UtopiaFIFOs are interconnected to supply the desired bus widths and streams to be merged. Widths up to 128 bits and 32 channels are possible. Figures 8 and 9 show the control signals between Master and Slave devices and the downstream "target system" for 4 independent 9-bit channels merging to one 36-bit output bus.

The Slave UtopiaFIFO output pin status is shown in Table 3. In this setup, the RRE must be disabled, and all output side control lines are inputs or not connected. As shown in Figure 8, in UtopiaRx mode, the "target" device receiving data sends the $\overline{ENS}$ signals to the Master and Slave. Output data from each UtopiaFIFO is available on the output bus on the following rising clock edge. The SOCS signal originates from the Master to alert the receiving device that respective bytes start a new cell for both UtopiaFIFOs. The MUX lines are inputs from the Master. The Master's CLAVS notifies the receiving device that both Master and Slave UtopiaFIFOs have cells available for transfer.

In UtopiaTx mode (see Figure 9), the $\overline{ENS}$ originates from the Master and is an input to the receiving device. On each assertion of $\overline{ENS}$, data from both UtopiaFIFOs is presented to the respective output buses on the same clock cycle. The SOCS signal originates from the Master to alert the receiving device that byte starts a new cell for both UtopiaFIFOs. The receiving device sends a CLAVS to the Master and Slave to signal it can accept a new cell from both Master and Slave devices.

An example of a sixteen (9-bit) channel to one (36-bit) output channel is shown in Figure 10a. Here, the first rank of UtopiaFIFOs are connected with their output low bytes each connected to 2nd rank UtopiaFIFO-5 and all output high bytes connected as inputs to 2nd rank UtopiaFIFO-6. This allows 16 (155 Mbs) channels to be multiplexed onto one 36-bit output bus (2.4Gbs).

Figure 11 shows sixteen 9-bit channels multiplexed onto one 18-bit output channel.

BUILDING BLOCK MODE: 16 CHANNELS TO ONE 36-BIT OUTPUT CHANNEL FOR RX SIGNALS

The target system $\overline{ENS}$ signal in an Rx protocol feeds into all UtopiaFIFOs $\overline{ENS}$ inputs within Rank 2 (as shown in Figure 10b). As a result, a deasserted $\overline{ENS}$ will prevent data transfer from rank 2 to the target system. Data can only transfer in a pipelined fashion when $\overline{ENS}$ is active.

TABLE 3: Output Side of UtopiaFIFO

RR Status	Master/Slave Status	Pin Name	Rx Mode I/O	Tx Mode I/O
Enabled	Master	$\overline{ENS}$	I-case B	O-case A
Enabled	Master	CLAVS	O-case B	I-case A
Enabled	Master	SOCS	O-case B	O-case A
Enabled	Master	MUX	O-case B	O-case A
Enabled	Slave	$\overline{ENS}$	(not allowed)	(not allowed)
Enabled	Slave	CLAVS	(not allowed)	(not allowed)
Enabled	Slave	SOCS	(not allowed)	(not allowed)
Enabled	Slave	MUX	(not allowed)	(not allowed)
Disabled	Master	$\overline{ENS}$	I	O
Disabled	Master	CLAVS	O	I
Disabled	Master	SOCS	O	O
Disabled	Master	MUX	I	I
Disabled	Slave	$\overline{ENS}$	I-case D	N/C-case C
Disabled	Slave	CLAVS	N/C-case D	I-case C
Disabled	Slave	SOCS	N/C-case D	N/C-case C
Disabled	Slave	MUX	I-case D	I-case C

3206 tbl 17

All first Rank UtopiaFIFOs are set as Masters with the second Rank having one Master and one Slave. The master/slave control signaling for the Rx mode is shown in Figure 10c. After the Mux select signals are set, they are loaded into the Slave from the Master on the LDM rising clock edge. Once the mux signals are loaded either externally or internally via Round Robin Sequencer, the CLAVS from either Rank 1 or Rank 2 devices goes HIGH once a cell is available. The receiving system must issue an active $\overline{ENS}$ signal once it can accept a cell. When the CLAVS from Rank 2 and the receiving $\overline{ENS}$ signal are both asserted, data will be put on the output bus (from both the Master and Slave devices) on the clock cycle following assertion of $\overline{ENS}$. In this setup, $\overline{ENS}$ from the receiving system MUST be asserted when it can accept data regardless of the CLAVS signals (the target must not monitor CLAVS before asserting $\overline{ENS}$). As shown in Figure 10c, if $\overline{ENS}$ is low prior to CLAVS assertion, then once CLAVS is asserted, data is placed on the 36-bit bus on the same cycle. If CLAVS is asserted before $\overline{ENS}$, then once $\overline{ENS}$ is active, data is placed on the output bus on the next cycle. With the first output word, SOCS is asserted for one cycle. Data is synchronized between the Master and Slave internally. The Master will assert LDM and Mux1 and Mux2 to the Slave two cycles prior to data transfer to allow the Slave time to transfer data through internal registers; it places data on the output bus two cycles later. The receiving system can throttle data via the $\overline{ENS}$ signal.

BUILDING BLOCK MODE: 16 CHANNELS TO ONE 36-BIT OUTPUT CHANNEL FOR TX SIGNALS

In transmit Utopia mode, the data transmitter controls data flow. For the case of 16 channels to one 36-bit output channel, the second rank of UtopiaFIFOs controls data flow to the downstream system via the $\overline{ENS}$ signals. The data flow from rank 1 to rank 2 is controlled by rank 1. Data flow into rank 1 is controlled by the upstream system as described earlier for a single device mode. This signal control is shown in Figure 10d. Initially, the Mux select lines for the Master (either via round robin or through external selection) are selected and then loaded into the Slave on the rising edge of LDM. Once both $\overline{ENS}$ from the Master and CLAVS from the receiver are asserted, valid data is placed on the bus in 2 cycles. Data from the Slave is placed on the bus two cycles after the LDM signal is received and when CLAVS is asserted. For the first data word, SOCS is asserted. Until an entire cell is transferred, CLAVS can be HIGH or LOW. The transmitting device starts to monitor the CLAVS signal four cycles prior to a completed cell transfer. If the receiving device (either downstream system or rank 1 or rank 2 devices) cannot accept another cell transfer, it must de-assert the CLAVS signal no later than this cycle. The Utopia FIFO devices will determine if a second cell can be sent on the second cycle prior to last word transfer.

Cell Length Error Recovery

After the start of cell signal (SOCR) is received, future SOCR assertions prior to the end of current cell transfers are ignored. A counter keeps track of byte transfer. If a "short cell" occurs (where a SOCR signal is received prior to the end of cell transfer), the SOCR is ignored and the data from the next incoming cell is loaded into the existing "short cell" until it is filled to normal cell size. Any additional bytes from the incoming cell are ignored. The short cell and next subsequent cell contents are bad data. Recovery occurs on the third incoming cell. If a "long cell" occurs (where the number of bytes exceeds the defined cell size and no new SOCR signal received indicating a new cell), the extra bytes are ignored by the UtopiaFIFO. The FIFO receiving the long cell will wait for a new SOCR (and assertion of $\overline{ENR}$ and CLAVR) before continuing data transfer.

TABLE 4: Truth Table — Byte Insertion/Deletion Locations

Mode	Tx/Rx Mode	Byte Size	Ins/Del Selected	Result
1	Don't Care	Even	0	No added or deleted bytes
2	Don't Care	Odd	0	Byte insert to last high byte position
3	Tx	Even	1	Delete byte 5, insert byte to last high byte position
4	Rx	Even	1	Insert byte 6, insert byte to last high byte position
5	Tx	Odd	1	Delete byte 5
6	Rx	Odd	1	Insert byte 6

3206 tbl 18

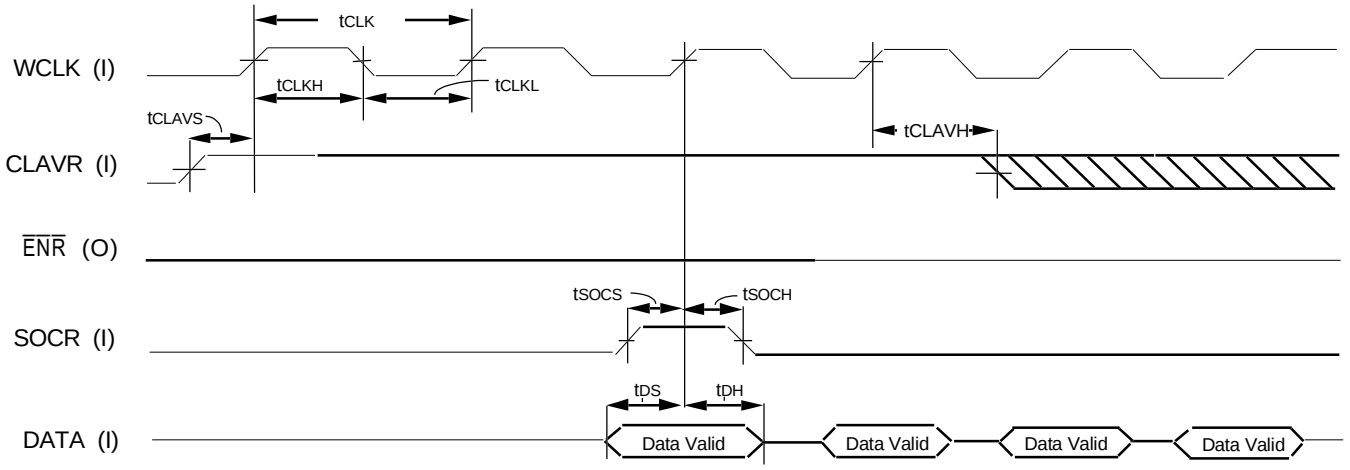
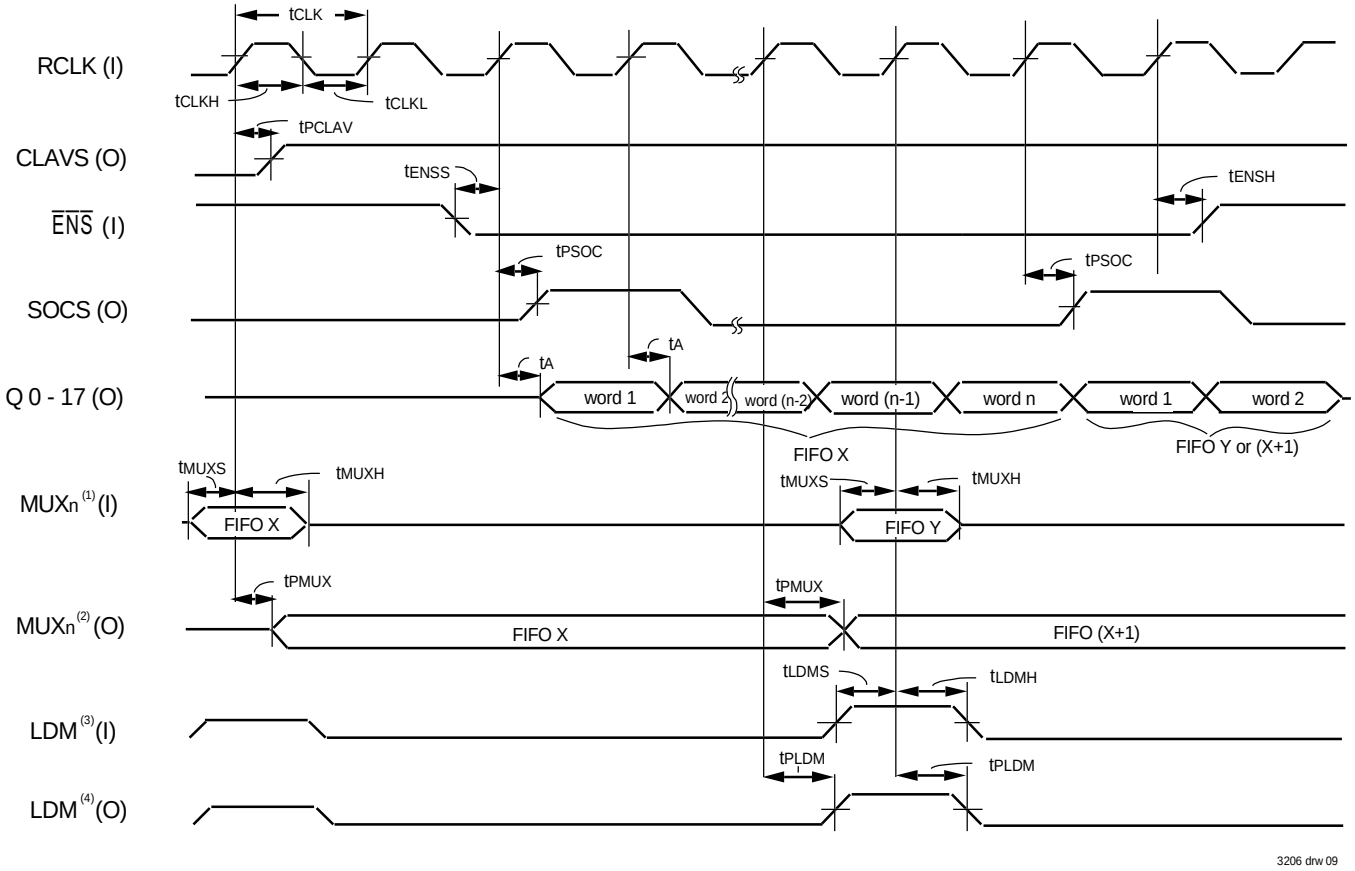


Figure 3. UtopiaFIFO Rx Mode Input Waveforms

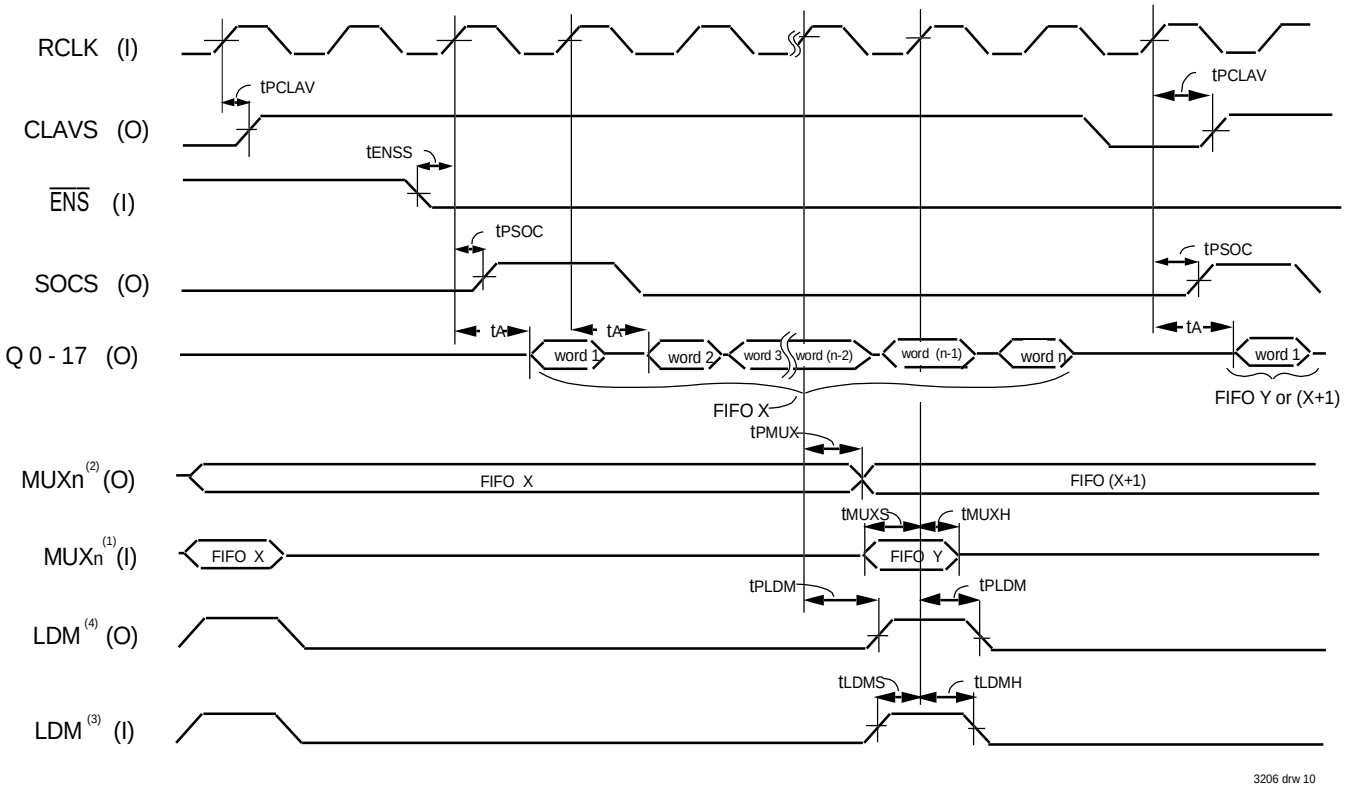
3206 drw 08



3206 drw 09

Figure 4a. UtopiaFIFO Rx Mode Output Waveforms (CLAVS Stays High)

NOTES:
1. RR = LOW
2. RR = HIGH
3. MSE = LOW
4. MSE = HIGH
5. n = cell size (in words)



NOTES:
1. RR = LOW
2. RR = HIGH
3. MSE = LOW
4. MSE = HIGH
5. n = cell size (in words)

Figure 4b. UtopiaFIFO Rx Mode Output Waveforms (Data Validity for Variable CLAVS)

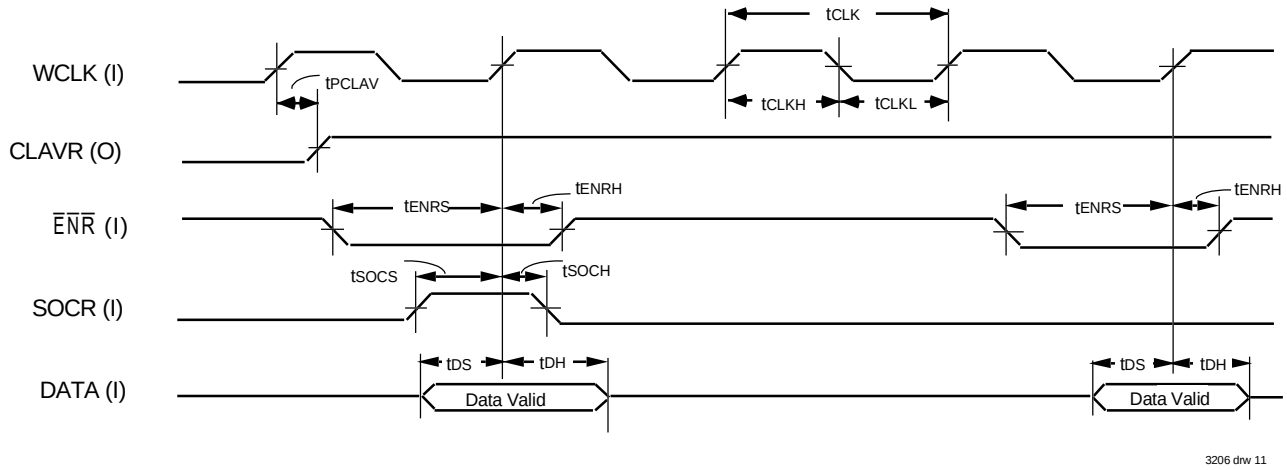


Figure 5a. UtopiaFIFO Tx Mode Input Waveforms

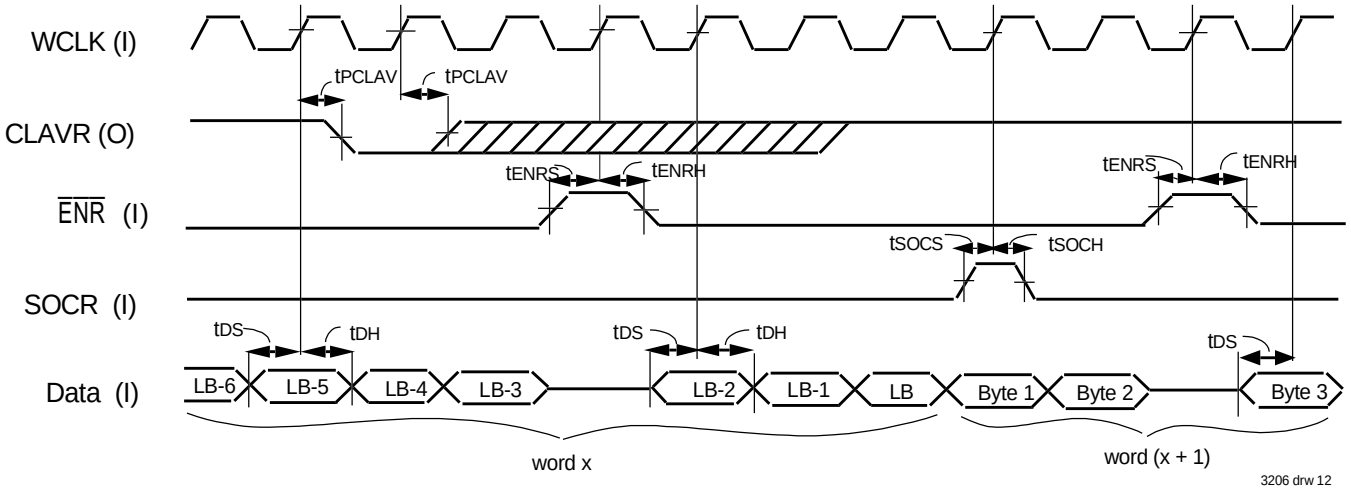


Figure 5b. UtopiaFIFO Tx Mode Input Waveforms (Continuous Cell Transfers)

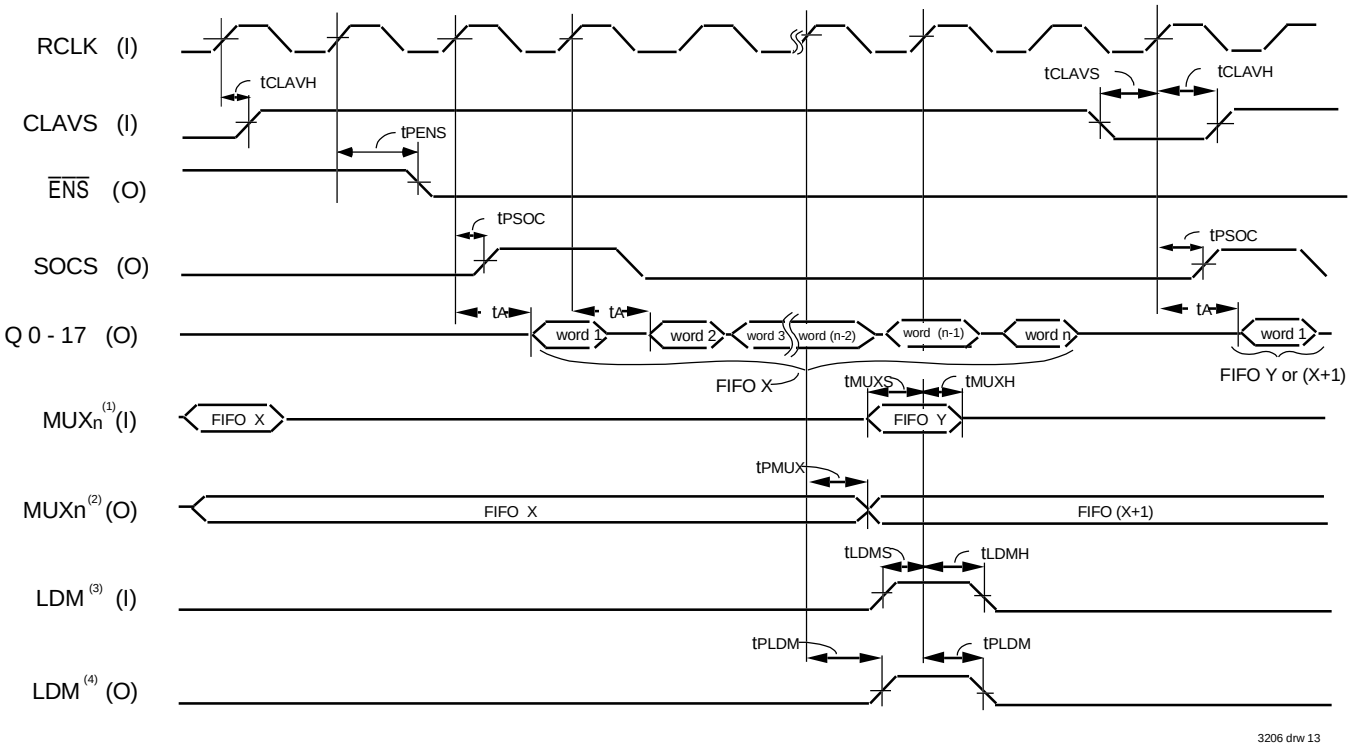
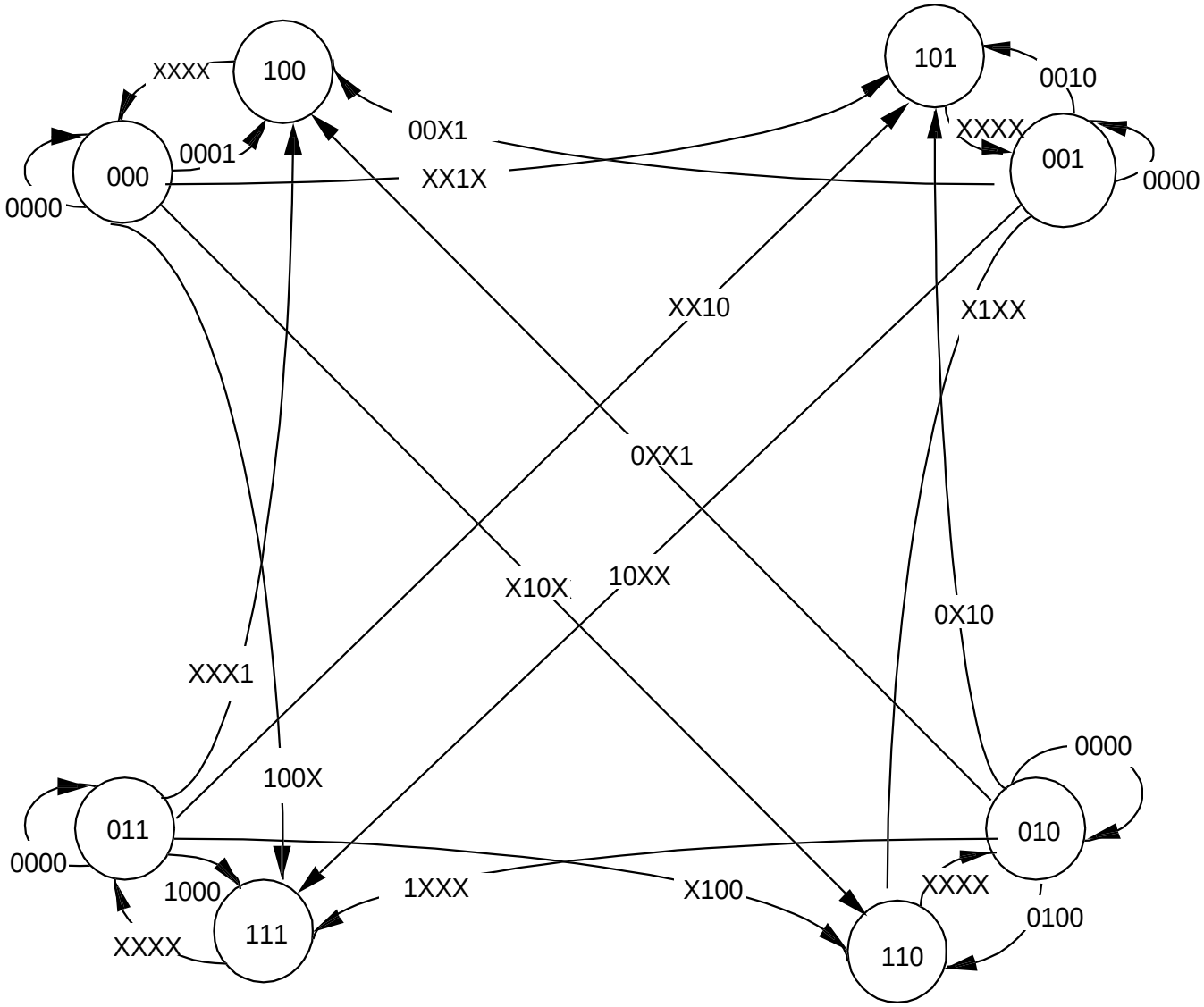


Figure 6. UtopiaFIFO Tx Mode Output Waveforms

NOTES:
1. RR = LOW
2. RR = HIGH
3. MSE = LOW
4. MSE = HIGH
5. n = cell size (in words)



NOTE:

LDM Mux2 Mux1 ⟷ CLAV[3:0]

Initial Condition
Set the Mux2, Mux1 = 11
Reset the LDM = 0
Reset CLAV[3:0] = 0000

3206 drw 14

Figure 7. Round Robin State Machine

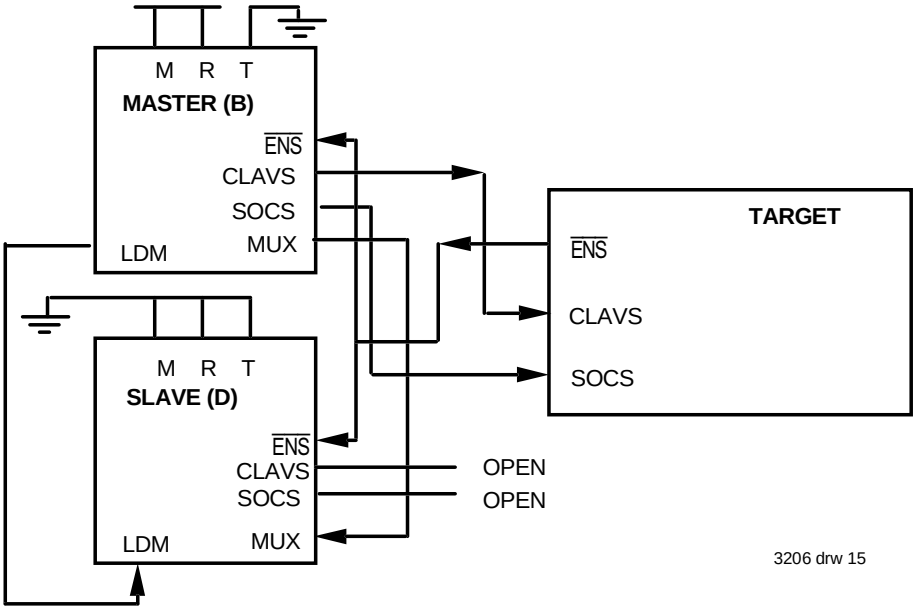


Figure 8. UtopiaRx Output Signaling: Master/Slave Building-Block Configuration for 4 Channel Input to 1 36-bit Output

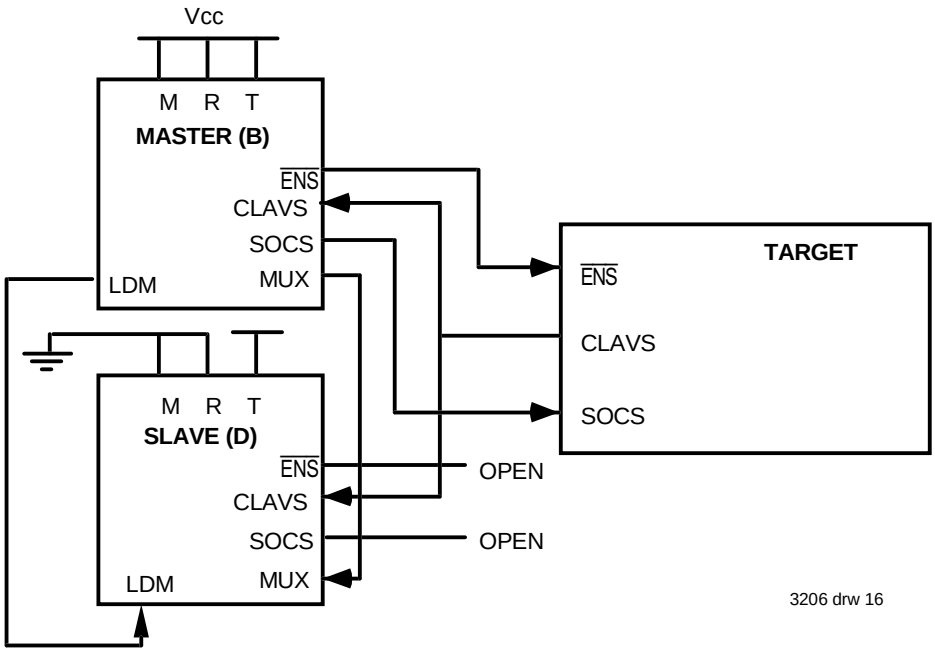


Figure 9. UtopiaTx Output Signaling: Master/Slave Building-Block Configuration for 4 Channel Input to 1 36-bit Output

NOTES:
M — Master/Slave Enable (MSE) pin
R — Round Robin Enable (RRE) pin
T — Rx/Tx Select (CRTS) pin

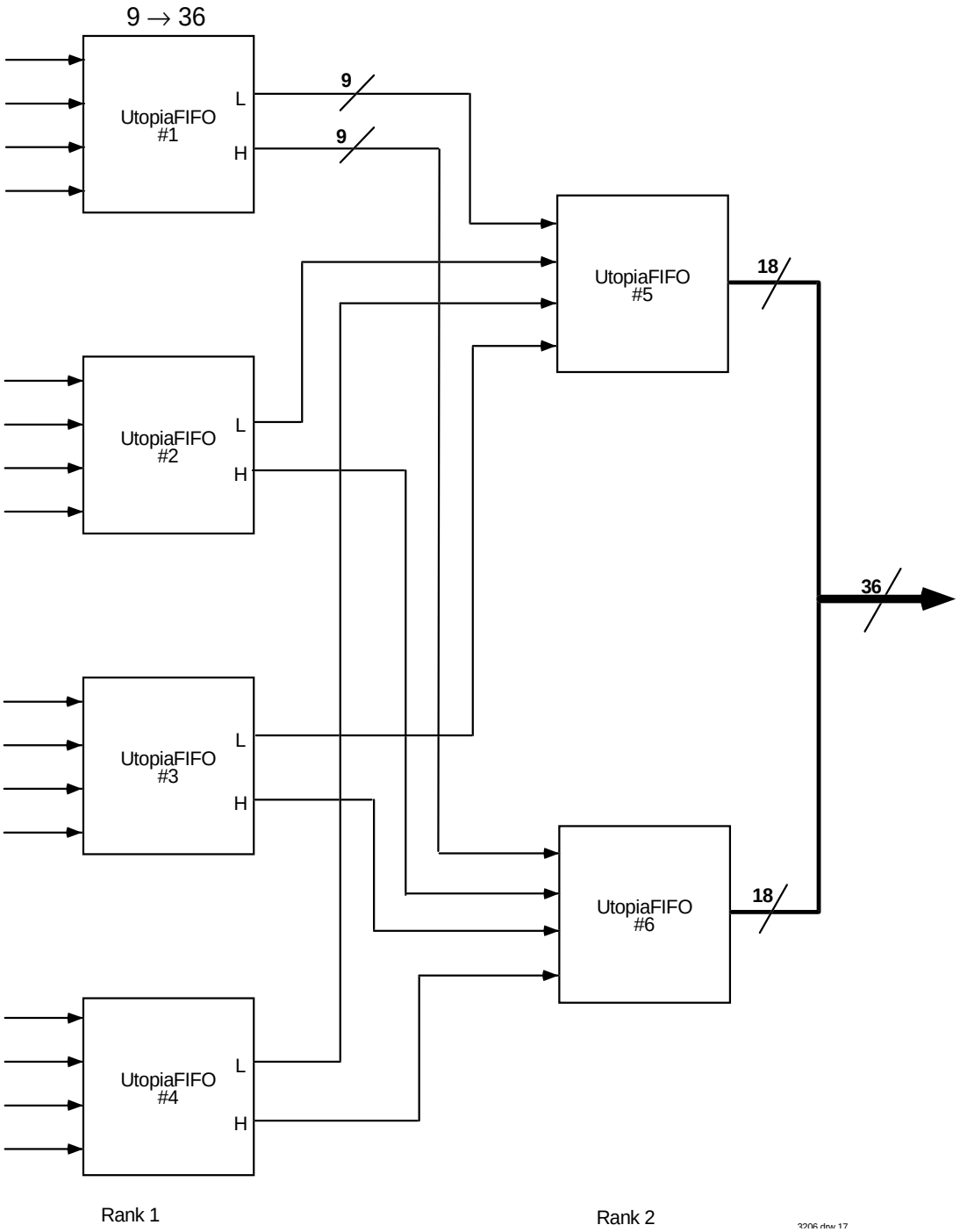


Figure 10a. 16 9-bit Channels to One 36-bit Channel Implementation

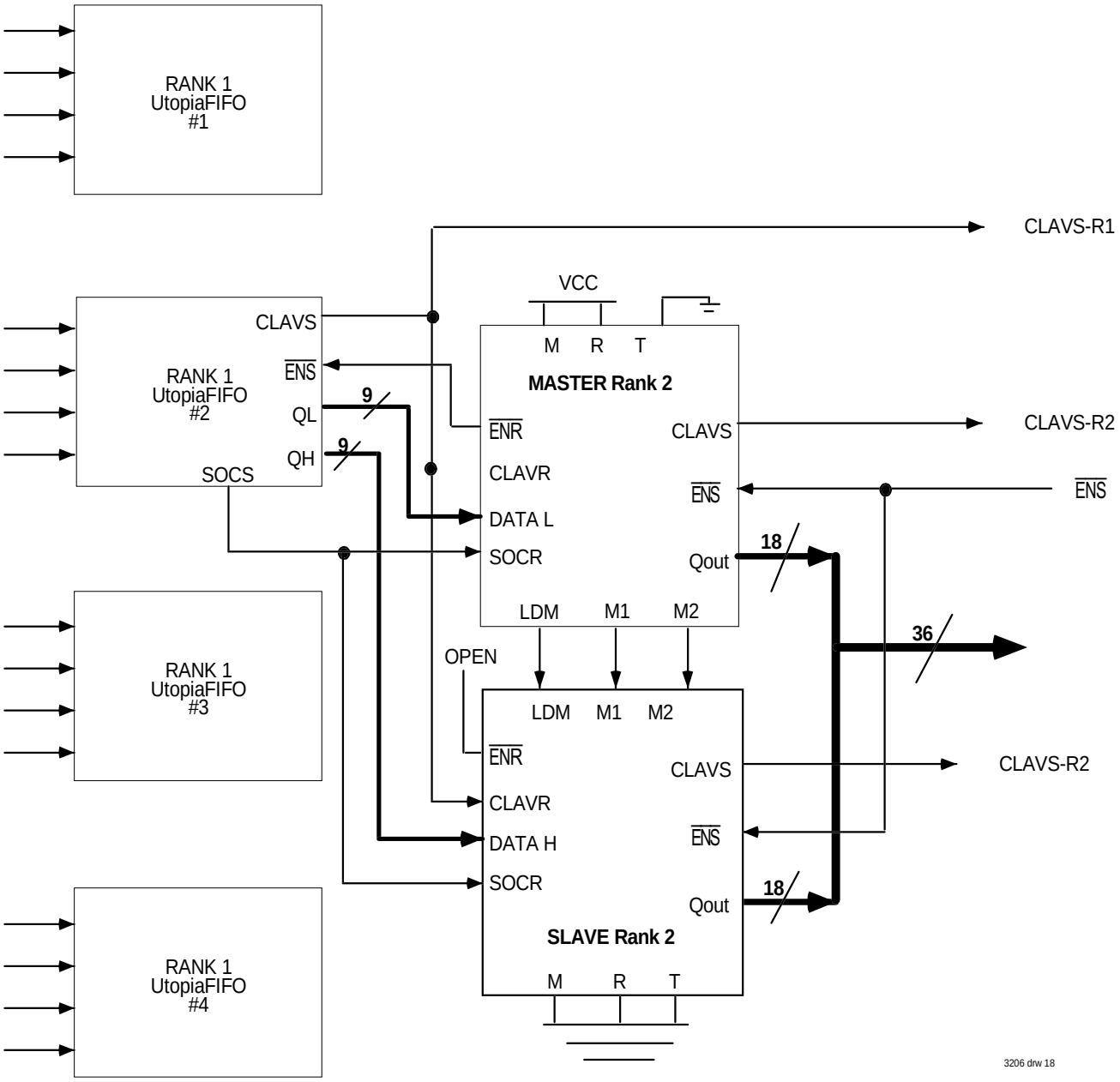


Figure 10b. Rx Mode — Data/Control Signaling

NOTE:

1. Rank 1 devices 1, 3, and 4 connect the same as device 2.
2. Control Signals shown pertain to connections from Rank 1—Utopia #2 to Rank 2 Master, Slave devices. Each Rank 2 device has additional identical connections to both Master/Slave devices from each Rank 1 device.

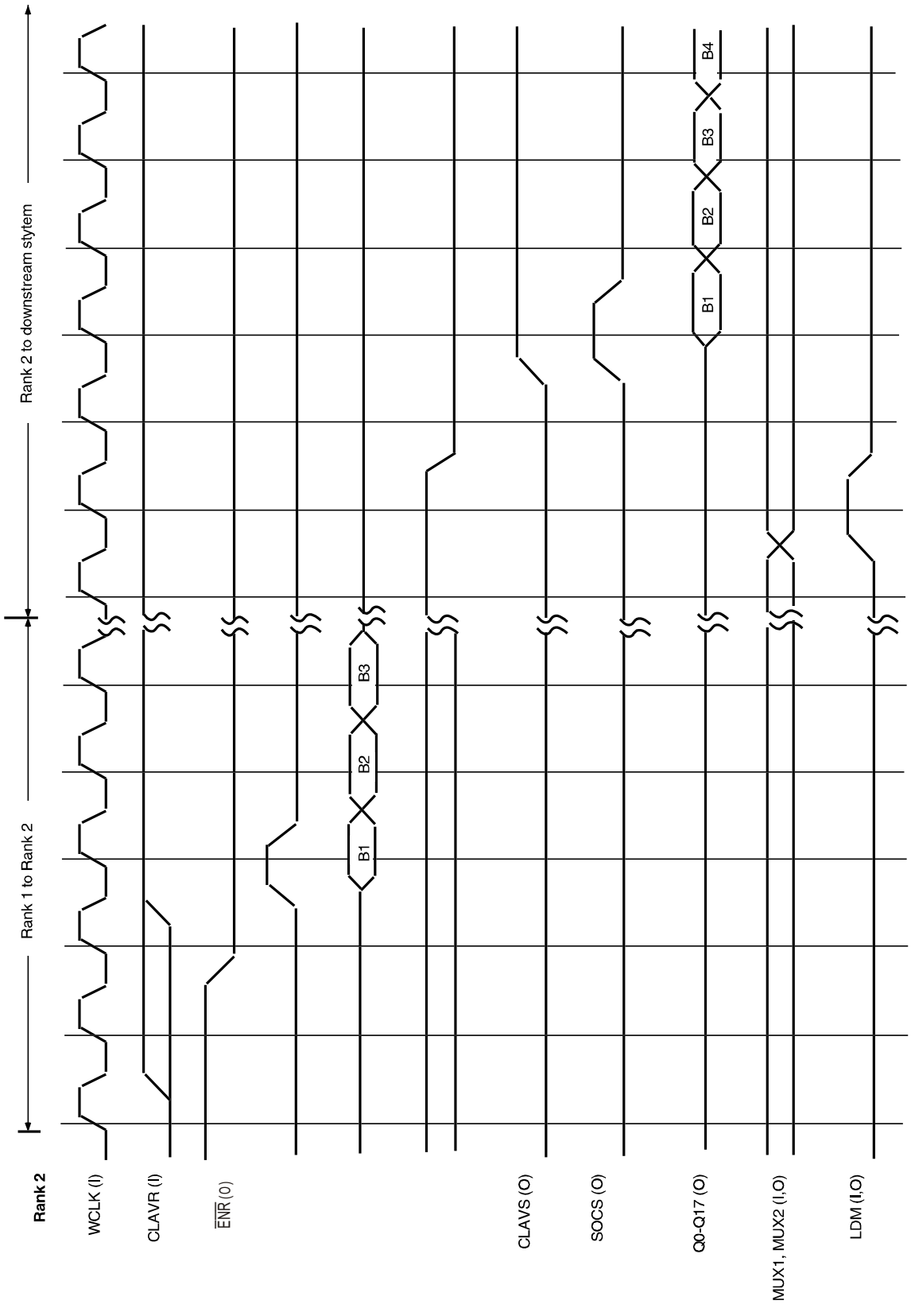


Figure 10c. Rx Mode—Rank 1 to Rank 2 and Rank 2 to Downstream System Output Timing

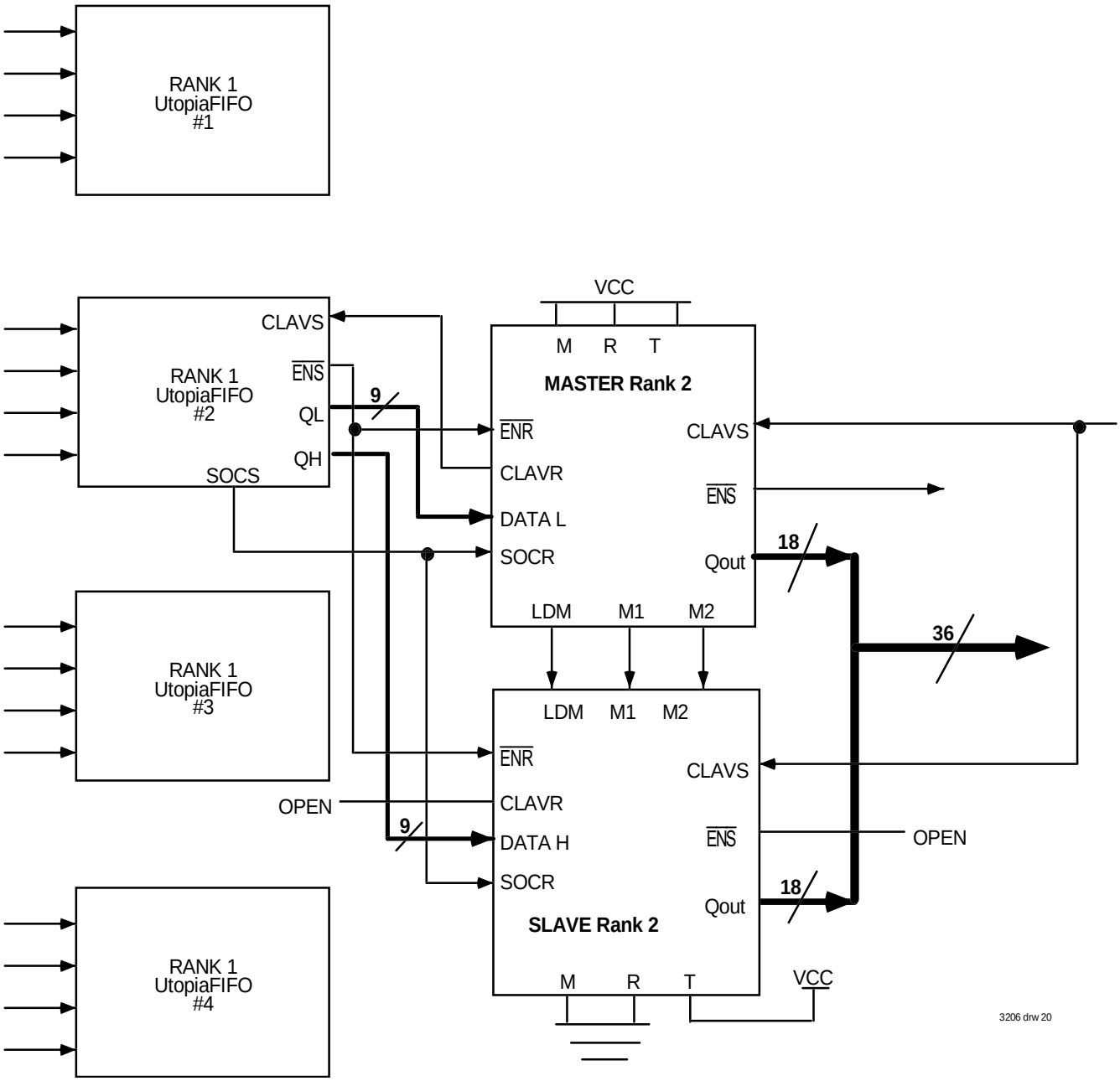


Figure 10d. Tx Mode — Data/Control Signaling

NOTE:

1. Rank 1 devices 1, 3, and 4 connect the same as device 2.
2. Control Signals shown pertain to connections from Rank 1—Utopia #2 to Rank 2 Master, Slave devices. Each Rank 2 device has additional identical connections to both Master/Slave devices from each Rank 1 device.

RANK 2

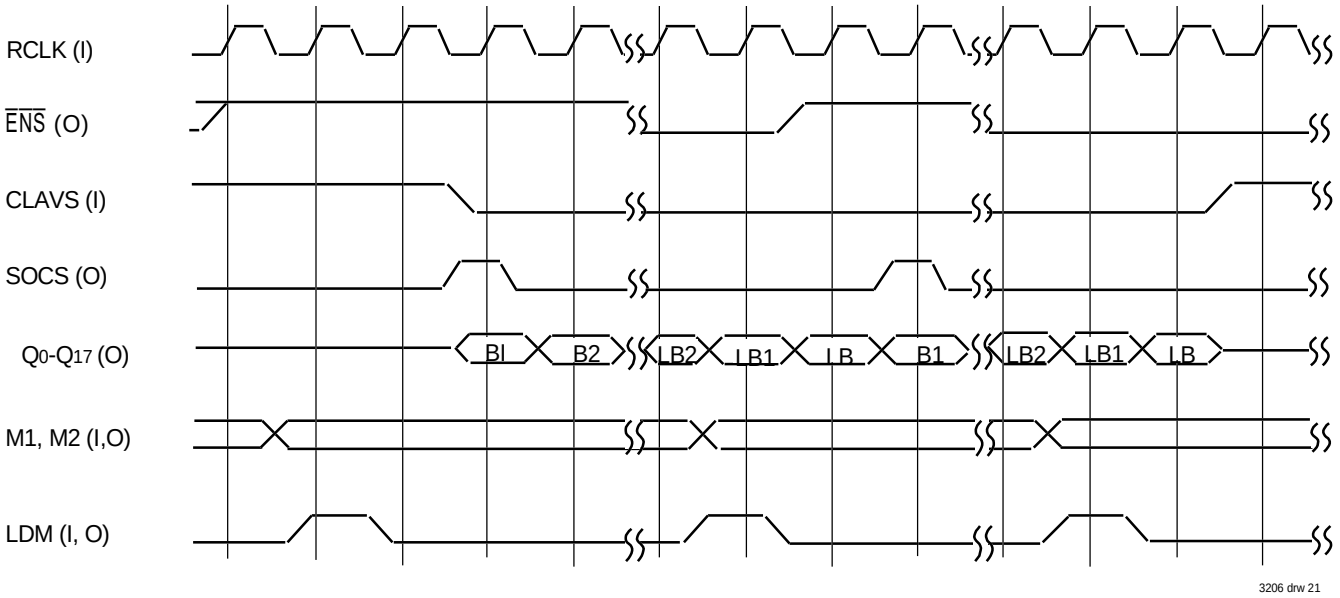


Figure 10e. Tx Mode—Output Timing

RANK 2

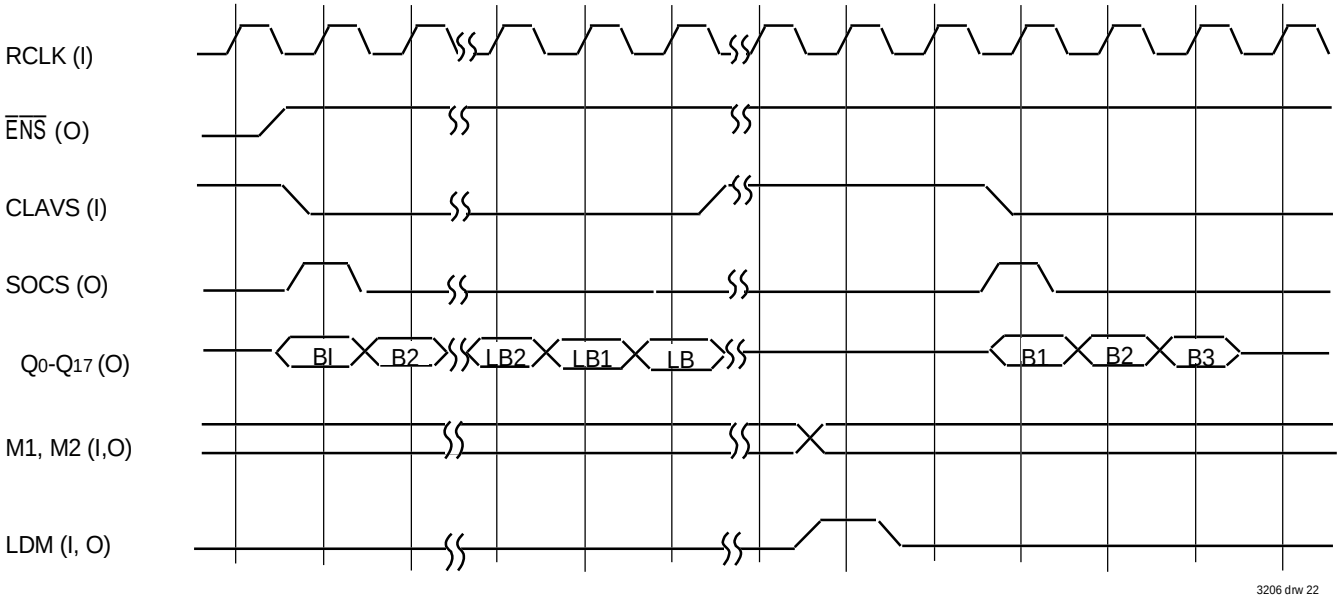


Figure 10e. Tx Mode—Output Timing (cont.)

NOTE:
1. B1 - Byte One of cell
   LB - Last Byte of cell
   LB1 - Second to Last Byte of cell

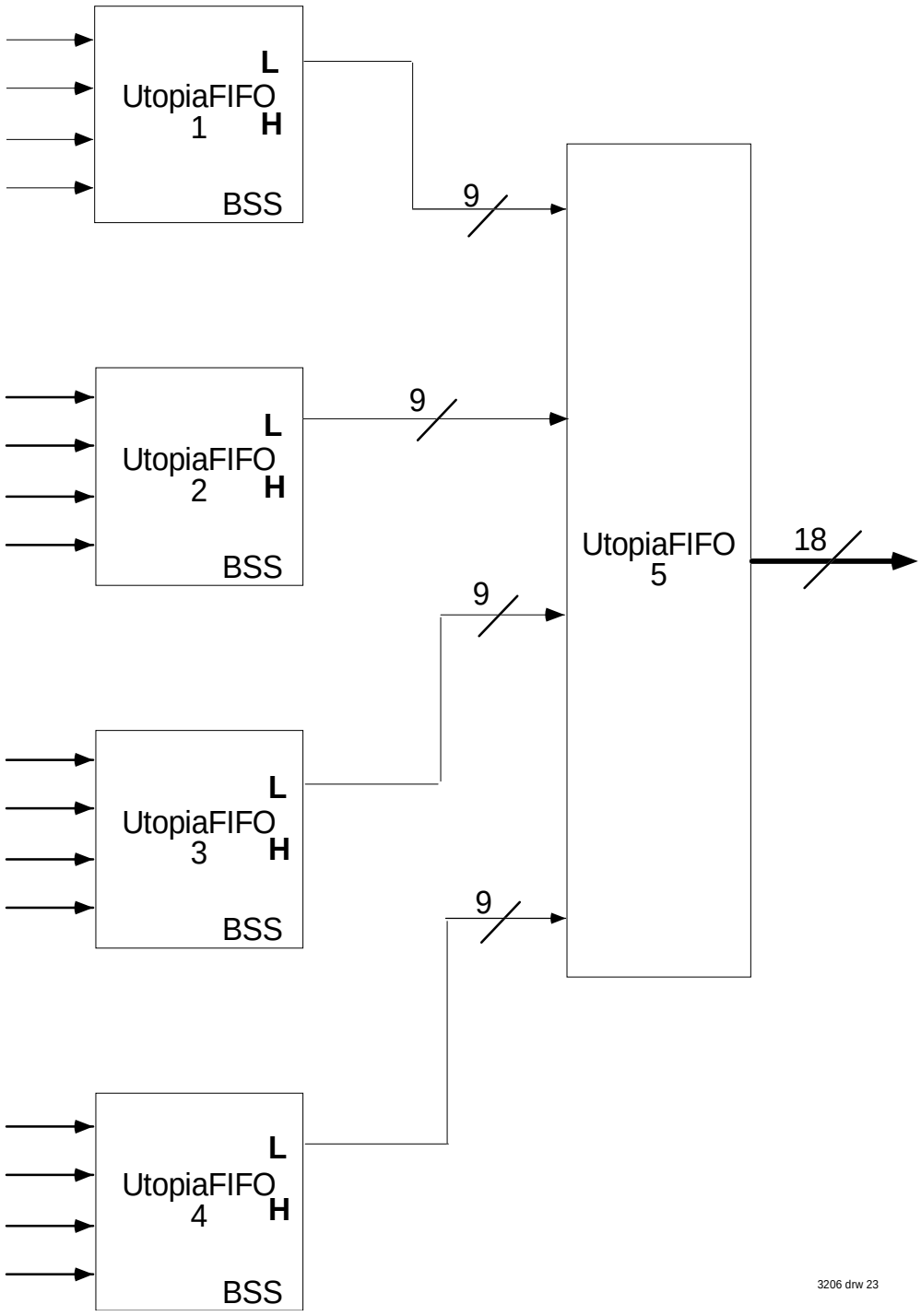
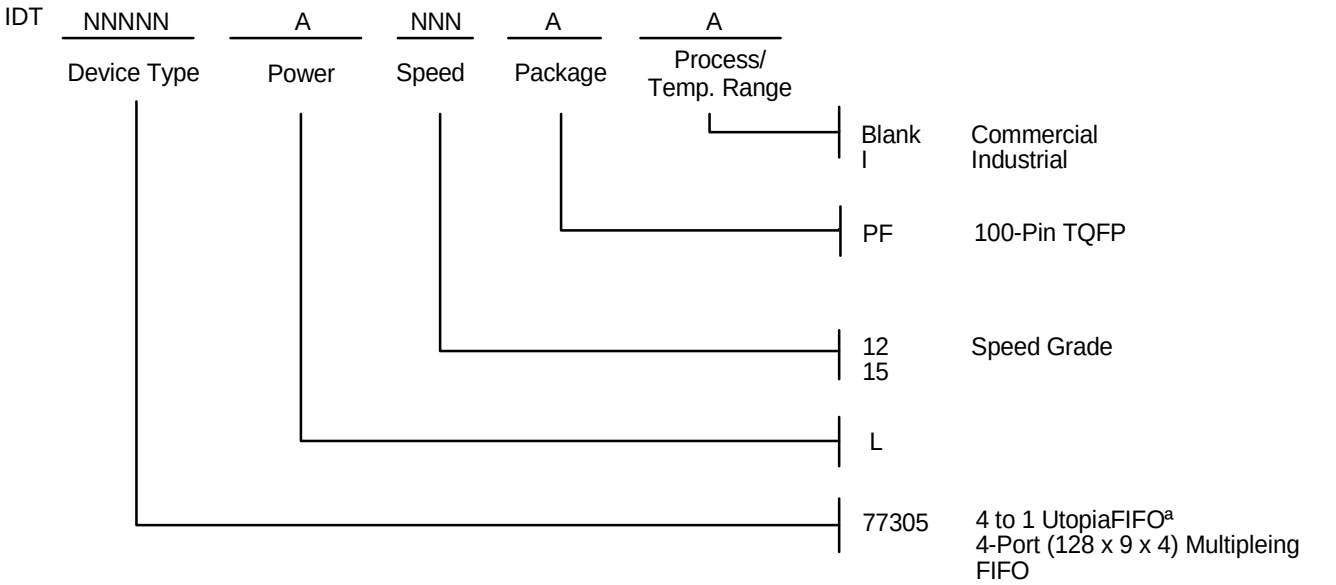


Figure 11. 16 9-bit Channels to One 18-bit Channel Implementation

Ordering Information



3206 drw 24

Datasheet Document History

12/1/95: Initial Draft
1/15/95: Corrected Typographical Errors
8/14/95: Added AC specs and correct diagrams and upgraded to "PRELIMINARY"
12/3/96: Changed the definition of LDM to reflect correct funtionallity
1/12/98: Corrected multiple errors in text and timing diagrams
3/14/00: Changed datasheet design format
3/26/01: Changed Preliminary to Final. In AC Characteristics Table, changed maximum from 8 to 10 for following pins: t_{PCLAV}, t_{PENS}, t_{PSOC}, t_{PLDM}, t_{PMUX}, t_{XOE}, t_{OE}, t_{XOHZ}, t_{OHZ}, t_{PRS}, and t_A. In same table, changed minimum from 4.5 to 5 for pins t_{MUXS}, t_{LDMS}, t_{SOCS}, t_{DS}, t_{CLAVS}, and t_{ENSS}.

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
408-330-1752
sarhelp@idt.com