Integrated Device Technology, Inc.

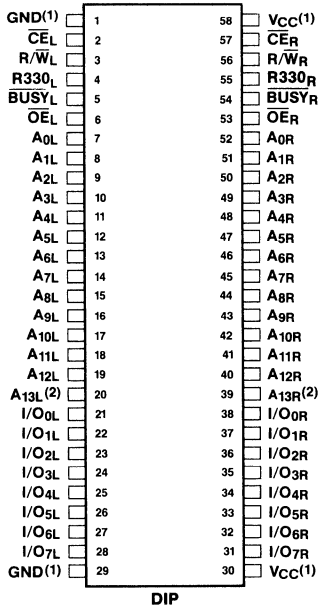
CMOS DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

PRELIMINARY
IDT7M134S
IDT7M135S

FEATURES:

- High-density 64K/128K-bit CMOS dual-port RAM module
- 16K x 8 organization (IDT7M135) with 8K x 8 option (IDT7M134)
- Low-power consumption
- CEMOS™ process virtually eliminates alpha particle soft errors rates (with no organic die coating)
- On-chip port arbitration logic
- $\overline{BUSY}$ flags
- Fully asynchronous operation from either port
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- On-chip pull up resistors for open-drain $\overline{BUSY}$ flag option
- Inputs and output directly TTL-compatible
- Fully static operation
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirement

PIN CONFIGURATION



DIP
TOP VIEW

NOTES

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On 8Kx8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.

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DESCRIPTION:

The IDT7M134/135 are 64K/128K-bit high-speed CMOS dual-port static RAM modules constructed on a multi-layered ceramic substrate using four IDT7132 2K x 8 dual-port RAMs (IDT7M134) or eight IDT7132 dual-port RAMs (IDT7M135) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M134 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.) Extremely high speeds are achieved in this fashion due to the use of the IDT7132 dual-port RAM, fabricated in IDT's high-performance CEMOS technology.

The IDT7M134/IDT7M135 provide two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. The on-chip arbitration logic will determine which port has access and sets the $\overline{BUSY}$ flag of the delayed port. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive).

The IDT7M134/135 are available with access times as fast as 70ns commercial and 90ns military temperature range, with operating power consumption of only 2.1W/3.5W (max.). The module also offers a standby power mode of 1.4W/2.8W (max.) and a full standby mode of 660mW/1.3W (max.).

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
$R/\overline{W}_L$	$R/\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	$\overline{BUSY}$ FLAG (OPEN DRAIN)
$R330_L$	$R330_R$	PULL-UP RESISTORS for Open-drain $\overline{BUSY}$ FLAG option
A_{0L}-A_{13L}	A_{0R}-A_{13R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

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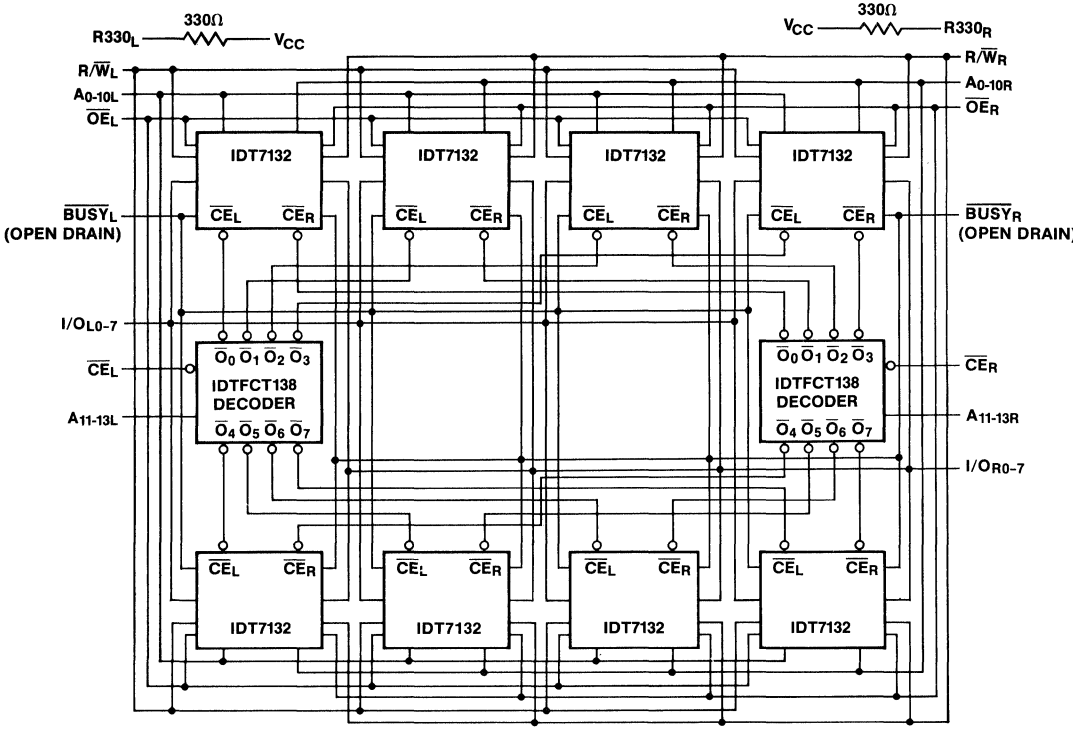
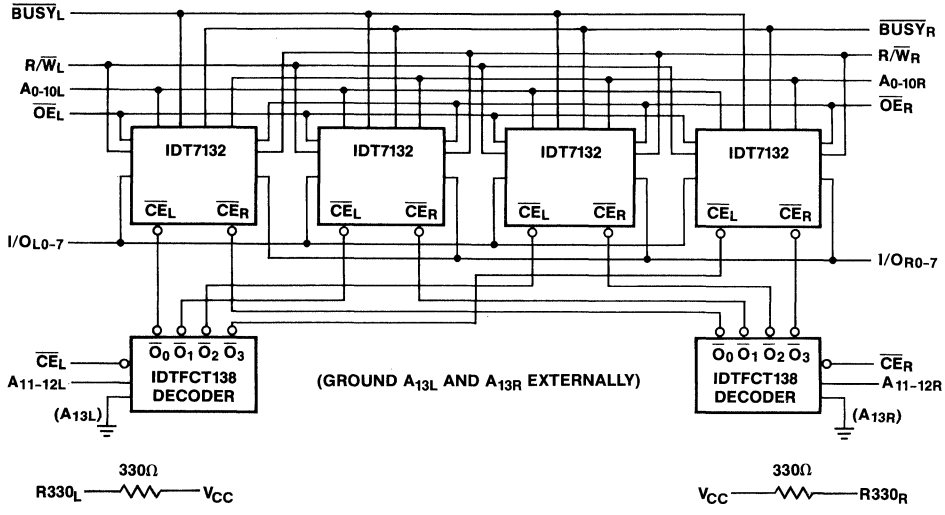
Printed in U.S.A.

FUNCTIONAL BLOCK DIAGRAMS

(A) IDT7M135 (16K x 8-BIT)



(B) IDT7M134 (8K x 8-BIT)



ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	8.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} = -3.5V for pulse width less than 30ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M134S MIN.	IDT7M134S TYP.(1)	IDT7M134S MAX.	IDT7M135S MIN.	IDT7M135S TYP.(1)	IDT7M135S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	—	—	20	µA
V_{IH}	Input High Voltage		2.2	—	6.0	2.2	—	6.0	V
V_{IL}	Input Low Voltage		-1.0(2)	—	0.8	-1.0(2)	—	0.8	V
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open	—	190	380	—	320	640	mA
I_{SB}	Standby Current (Both Ports Standby)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$	—	130	260	—	260	520	mA
I_{SB_1}	Standby Current (One Port Standby)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open	—	160	320	—	290	580	mA
I_{SB_2}	Full Standby Current (Both Ports Full Standby)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	—	4	120(3)	—	10	240(3)	mA
V_{OL}	Output Low Voltage (I/O_0 - I/O_7)	I_{OL} = 3.5mA, V_{CC} = 4.5V	—	—	0.4	—	—	0.4	V
		I_{OL} = 8mA, V_{CC} = 4.5V	—	—	0.5	—	—	0.5	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA, V_{CC} = 4.5V	—	—	0.5	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = 4.5V	2.4	—	—	2.4	—	—	V

NOTES:

1. V_{CC} = 5V, T_A = +25°C.
2. V_{IL} min. = -3.5V for pulse width less than 30ns.
3. I_{SB_2} max. of IDT7M134/IDT7M135 at commercial temperature = 80mA/150mA.

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AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M134S70 IDT7M135S70 COM'L. ONLY		IDT7M134S90 IDT7M135S90		IDT7M134S100 IDT7M135S100		IDT7M134S120 IDT7M135S120		IDT7M134S140 IDT7M135S140 MIL. ONLY		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	70	—	90	—	100	—	120	—	140	—	ns
t_{AA}	Address Access Time	—	70	—	90	—	100	—	120	—	140	ns
t_{ACE}	Chip Enable Access Time	—	70	—	90	—	100	—	120	—	140	ns
t_{AOE}	Output Enable Access Time	—	40	—	45	—	50	—	60	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	10	—	10	—	10	—	10	—	ns
t_{CLZ}	Chip Select to Output in Low Z	10	—	15	—	15	—	15	—	15	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	35	—	45	—	50	—	50	—	60	ns
t_{OHZ}	Output Enable to Output in High Z	—	30	—	40	—	40	—	40	—	50	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Enable to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time	—	50	—	50	—	50	—	50	—	50	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	70	—	90	—	100	—	120	—	140	—	ns
t_{CW}	Chip Selection to End of Write	60	—	80	—	95	—	110	—	120	—	ns
t_{AW}	Address Valid to End of Write	60	—	80	—	95	—	110	—	120	—	ns
t_{AS}	Address Setup Time	10	—	10	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	55	—	65	—	75	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{DW}	Data Valid to End of Write	30	—	40	—	40	—	40	—	50	—	ns
t_{DH}	Data Hold Time	10	—	10	—	10	—	10	—	10	—	ns
t_{OHZ}	Output Enable to Output in High Z	—	35	—	40	—	40	—	40	—	40	ns
t_{WZ}	Write Enabled to Output in High Z	—	35	—	40	—	40	—	50	—	60	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	ns
BUSY TIMING												
t_{RC}	Read Cycle Time	70	—	90	—	100	—	120	—	140	—	
t_{WC}	Write Cycle Time	70	—	90	—	100	—	120	—	140	—	
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	45	—	45	—	50	—	60	—	70	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	45	—	45	—	50	—	60	—	70	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Enable	—	40	—	40	—	50	—	60	—	70	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Enable	—	35	—	35	—	50	—	60	—	70	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data	—	50	—	50	—	60	—	80	—	90	ns
t_{WDD}	Write Pulse to Data Delay	—	90	—	100	—	120	—	140	—	160	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	70	—	80	—	100	—	120	—	140	ns
t_{APS}	Arbitration Priority Set Up Time	10	—	10	—	10	—	10	—	10	—	ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1, 2, and 3

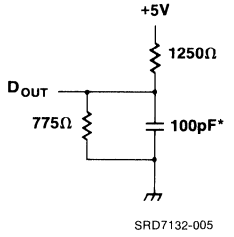


Figure 1.
Output Load

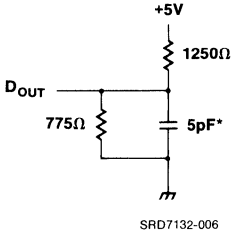


Figure 2.
Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

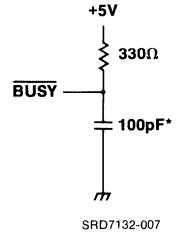


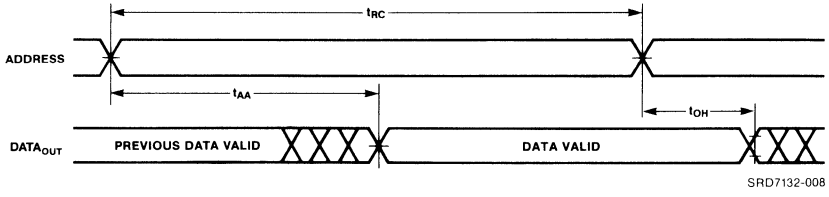
Figure 3.
$\overline{BUSY}$ Output Load

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	7M134S	7M135S	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	150	180	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	70	pF

NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 EITHER SIDE(1,2,6)



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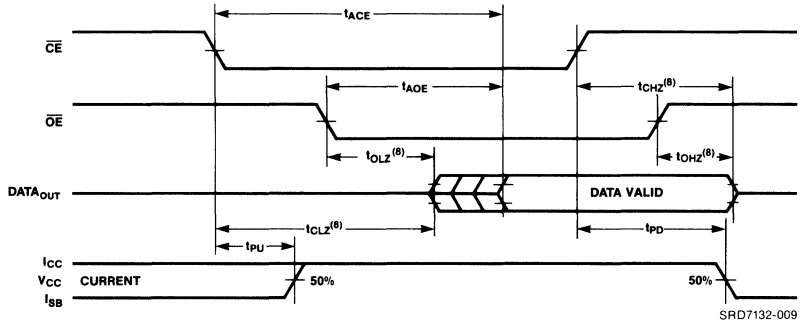
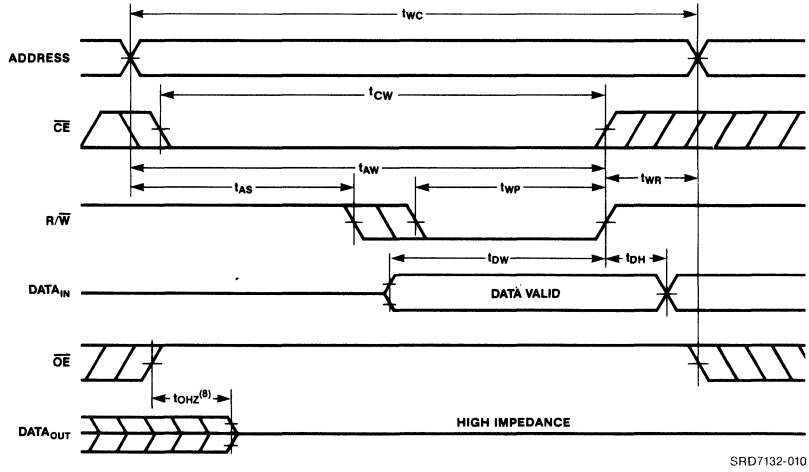
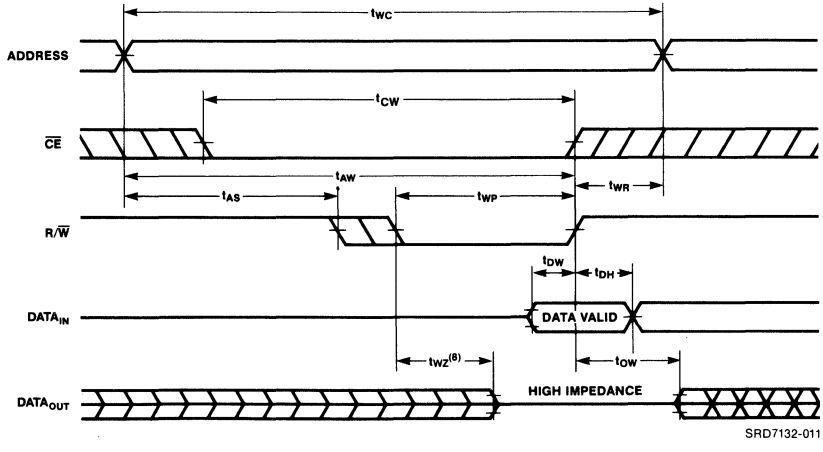
TIMING WAVEFORM OF READ CYCLE NO. 2 EITHER SIDE[1,3]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 EITHER SIDE[4,7]

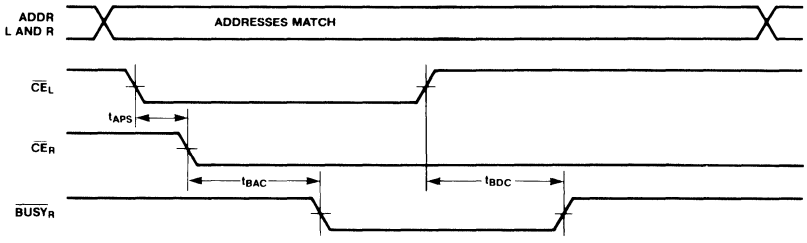


TIMING WAVEFORM OF WRITE CYCLE NO. 1 EITHER SIDE[4,7]



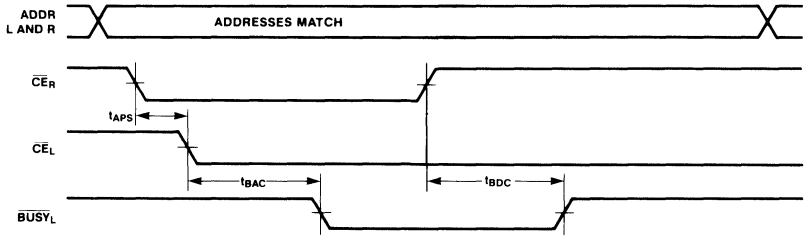
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1 $\overline{CE}$ ARBITRATION

$\overline{CE}_L$ VALID FIRST:



SRD7132-012

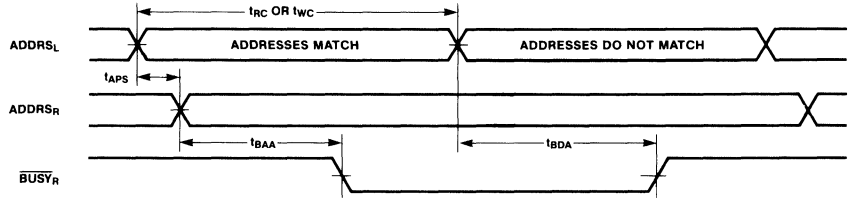
$\overline{CE}_R$ VALID FIRST:



SRD7132-013

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2 ADDRESS VALID ARBITRATION(5)

LEFT ADDRESS VALID FIRST



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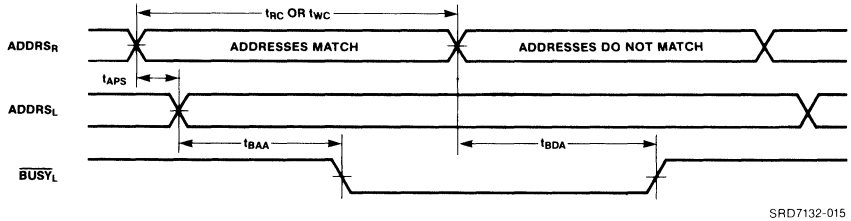
RIGHT ADDRESS VALID FIRST



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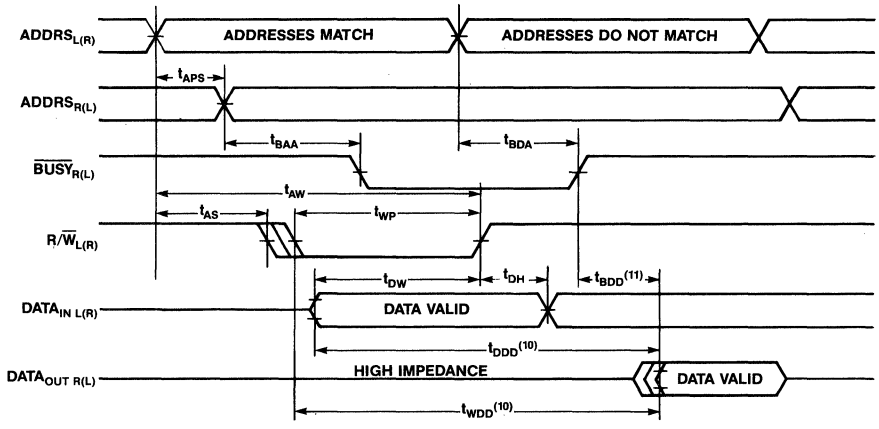
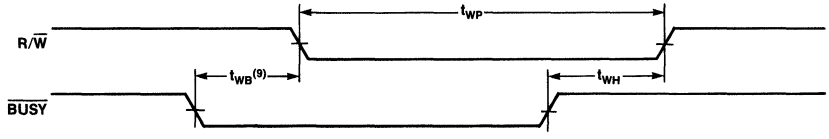
TIMING WAVEFORM OF READ WITH BUSY(5)



SRD7134-001

TIMING WAVEFORM OF WRITE WITH BUSY(5)



SRD7134-002

NOTES:

1. R/$\overline{W}$ is high for Read Cycles.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition low.
4. If $\overline{CE}$ goes high simultaneously with R/$\overline{W}$ high, the outputs remain in the high impedance state.
5. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}.
6. $\overline{OE}$ = V_{IL}.
7. R/$\overline{W}$ = V_{IH} during address transition.
8. Transition is measured at ±500mV from low or high impedance voltage with load (Figures 1, 2 & 3). This parameter is guaranteed by design, but not tested.
9. For slave port (IDT7M144/IDT7M145) only.
10. Port-to-port delay through RAM cells from writing port to reading port.
11. This parameter guaranteed by design, but not tested.

FUNCTIONAL DESCRIPTION:

The IDT7M134/IDT7M135 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7M134/IDT7M135 has an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION:

The arbitration logic will resolve an address match or a chip enable match down to 10ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and set the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) If the addresses match and are valid before $\overline{CE}$, on-chip control logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III, Address Arbitration). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION:

Expanding the data bus width to sixteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its L $\overline{BUSY}$ while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL, LEFT OR RIGHT PORT[1]

$R/\overline{W}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	FUNCTION
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = H$, Power Down Mode, I_{SB} or I_{SB2}
L	L	X	$DATA_{IN}$	Data on Port Written into Memory[2]
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES:

1. $A_{0L} - A_{13L} \neq A_{0R} - A_{13R}$
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.

H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

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TABLE II — ARBITRATION

LEFT PORT		RIGHT PORT		FLAGS		FUNCTION
$\overline{CE}_L$	A_{0L}-A_{13L}	$\overline{CE}_R$	A_{0R}-A_{13R}	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R}$-A_{13R}	L	$\neq A_{0L}$-A_{13L}	H	H	No Contention
ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH						
L	LV10R	L	LV10R	H	L	Left-Port Wins
L	RV10L	L	LV10R	L	H	Right-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CE}$						
LL10R	= A_{0R} - A_{13R}	LL10R	= A_{0L} - A_{13L}	H	L	Left-Port Wins
RL10L	= A_{0R} - A_{13R}	RL10R	= A_{0L} - A_{13L}	L	H	Right-Port Wins
LW10R	= A_{0R} - A_{13R}	LW10R	= A_{0L} - A_{13L}	H	L	Arbitration Resolved
LW10R	= A_{0R} - A_{13R}	LW10R	= A_{0L} - A_{13L}	L	H	Arbitration Resolved

NOTE:

X = DON'T CARE, L = LOW, H = HIGH, Same = Left and Right Addresses match within 10ns of each other.

LV10R = Left Address Valid ≥ 10ns before Right Address.

RV10L = Right Address Valid ≥ 10ns before Left Address.

LL10R = Left $\overline{CE}$ = LOW ≥ 10ns before Right $\overline{CE}$.

RL10L = Right $\overline{CE}$ = LOW ≥ 10ns before Left $\overline{CE}$.

LW10R = Left and Right $\overline{CE}$ = LOW within 10ns of each other.