CMOS SLAVE DUAL-PORT RAM MODULE 64K (8K x 8-BIT) & 128K (16K x 8-BIT)

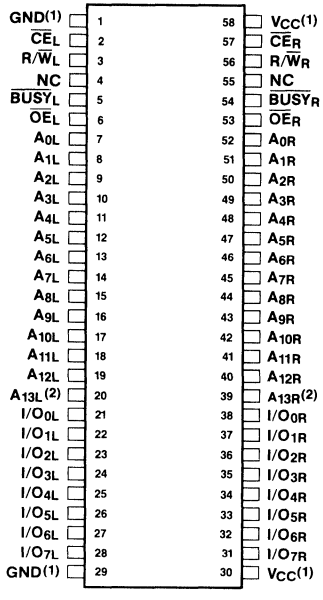
PRELIMINARY
IDT7M144S
IDT7M145S

Integrated Device Technology, Inc.

FEATURES:

- High-density 64K/128K-bit CMOS slave dual-port RAM module
- Easily expands data bus width to 16-or-more-bits when used with master IDT7M134 or IDT7M135
- 16K x 8 organization (IDT7M145) or 8K x 8 option (IDT7M144)
- High-speed access
  - —Military: 90/100/120/140ns (max.)
  - —Commercial: 70/90/100/120ns (max.)
- Low-power operation
  - —Active: 950mW (typ.) (IDT7M144)
  - —Standby: 20mW (typ.) (IDT7M144)
- $\overline{BUSY}$ input flags
- Fully asynchronous operation from either port
- Fully static operation
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Single 5V (±10%) power supply
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B

PIN CONFIGURATION



DIP
TOP VIEW

DESCRIPTION:

The IDT7M144/145 are 64K/128K-bit high-speed CEMOS™ SLAVE dual-port static RAM modules constructed on a multi-layered, co-fired, ceramic substrate using four IDT7142 2K x 8 slave dual-port RAMs (IDT7M144) or eight IDT7142 slave dual-port RAMs (IDT7M145) in leadless chip carriers. Dual-port function is achieved by utilization of the two on-board IDT54/74FCT138 decoder circuits that interpret the higher order addresses A_{L11-13} and A_{R11-13} to select one of the eight 2K x 8 dual-port RAMs. (On IDT7M144 8K x 8 option, the A_{L13} and A_{R13} need to be externally grounded and the selection becomes one of the four 2K x 8 dual-port RAMs.)

The IDT7M144/145 are designed as "SLAVE" dual-port RAM modules to be used together with the IDT7M134/135 "MASTER" dual-port RAM modules in 16-or-more-bit systems; whereas, the IDT7M134/135 are designed to be used as stand-alone 8-bit dual-port RAM modules. Using the IDT MASTER/SLAVE dual-port RAM module approach in 16-or-more-bit memory system applications results in full speed operation without the need for additional discrete logic.

Both SLAVE IDT7M144/145 and MASTER IDT7M134/135 modules provide two ports with separate control, address and I/O pins that permit independent asynchronous access for reads or writes to any location in the memory. The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. The delayed port will have access when $\overline{BUSY}$ goes high (inactive). The $\overline{BUSY}$ pins are outputs on the MASTER and inputs on the SLAVE.

PIN NAMES

LEFT PORT	RIGHT PORT	NAMES
$\overline{CE}_L$	$\overline{CE}_R$	CHIP ENABLE
R/$\overline{W}_L$	R/$\overline{W}_R$	READ/WRITE ENABLE
$\overline{OE}_L$	$\overline{OE}_R$	OUTPUT ENABLE
$\overline{BUSY}_L$	$\overline{BUSY}_R$	BUSY FLAG
A_{0L}-A_{13L}	A_{0R}-A_{13R}	ADDRESS
I/O_{0L}-I/O_{7L}	I/O_{0R}-I/O_{7R}	DATA INPUT/OUTPUT
V_{CC}		POWER
GND		GROUND

NOTES:
1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On 8K x 8 IDT7M134 option, A_{13L} and A_{13R} need to be externally connected to ground for proper operation.
3. IDT7M134/135 (MASTER): $\overline{BUSY}$ is open drain output and requires pull up resistor. IDT7M144/145 (SLAVE): $\overline{BUSY}$ is input.

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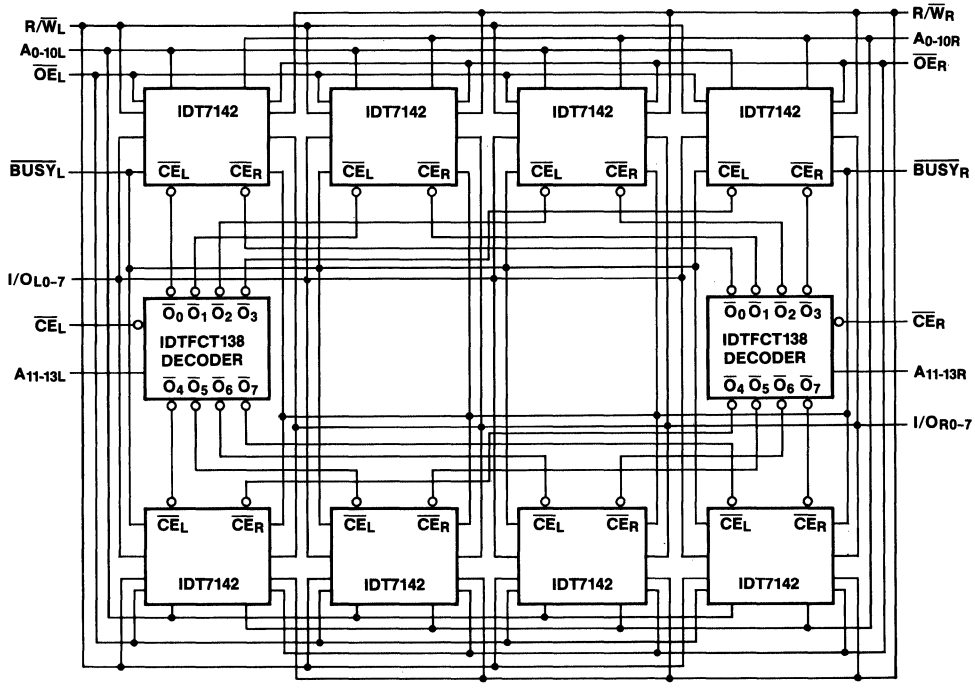
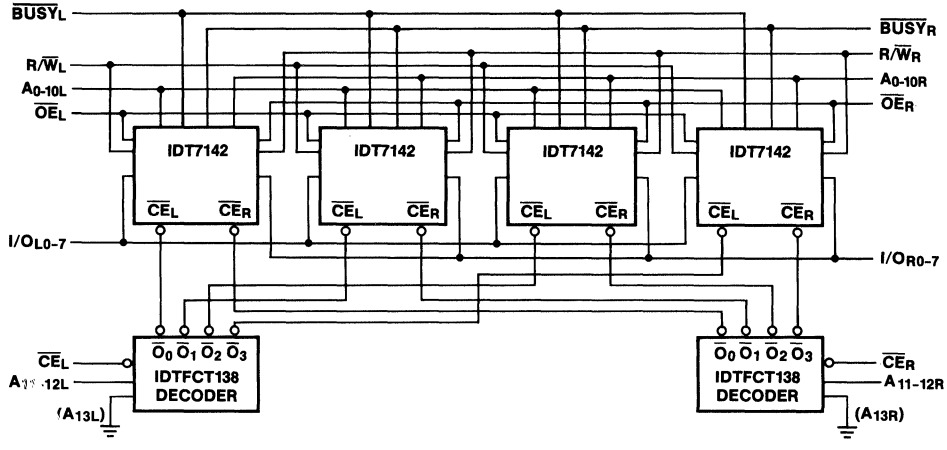
FUNCTIONAL BLOCK DIAGRAMS

(A) IDT7M145 (16K x 8-BIT)



(B) IDT7M144 (8K x 8-BIT)



(GROUND A_{13L} AND A_{13R} EXTERNALLY)

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

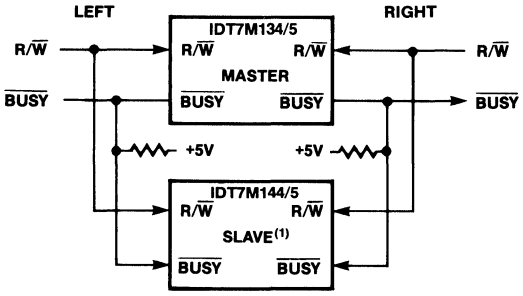
(DC electricals for the IDT7M144/IDT7M145 SLAVE Dual-Port are identical to the IDT7M134/IDT7M135 MASTER Dual-Port. Reference the IDT7M134/IDT7M135 CMOS Dual-Port RAM data sheet.)

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE

(AC electricals for the IDT7M144/IDT7M145 SLAVE Dual-Port are identical to the IDT7M134/IDT7M135 MASTER Dual-Port *except* where noted below.)

SYMBOL	PARAMETER	IDT7M144S70 IDT7M145S70 COM'L. ONLY		IDT7M144S90 IDT7M145S90		IDT7M144S100 IDT7M145S100		IDT7M144S120 IDT7M145S120		IDT7M144S140 IDT7M145S140 MIL. ONLY		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WP}	Write Pulse Width	40	—	50	—	60	—	70	—	80	—	ns
t_{WB}	Write to $\overline{BUSY}$	-10	—	-10	—	-10	—	-10	—	-10	—	ns
t_{WH}	Write Hold after $\overline{BUSY}$	20	—	20	—	20	—	20	—	20	—	ns

16-BIT MASTER/SLAVE DUAL PORT MEMORY SYSTEM



NOTE:

1. No arbitration in IDT7M144/IDT7M145 (SLAVE): $\overline{BUSY}$ IN inhibits write in IDT7M144/IDT7M145.

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