CMOS PARALLEL IN-OUT FIFO MODULE 2K x 9-BIT & 4K x 9-BIT

IDT7M203S
IDT7M204S

Integrated Device Technology, Inc.

FEATURES:

- First-In, First-Out memory module
- 2K x 9 organization (IDT7M203S)
- 4K x 9 organization (IDT7M204S)
- Low-power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Single 5V (±10%) power supply
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- High-performance CEMOS™ technology
- Pin compatible with IDT7201 and Mostek MK4501, but with four times word depth (IDT7M203S) or eight times (IDT7M204S)
- Module available with semiconductor components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M203/204 are FIFO memory modules that utilize a special First-In, First-Out algorithm that loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

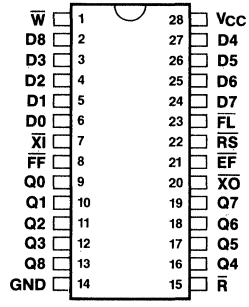
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The device has a read/write cycle time of 65ns (15MHz) for commercial and 70ns (14MHz) for military temperature ranges.

The device utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

The IDT7M203/204 are constructed on a multi-layered ceramic substrate using four IDT7201 (512x9) or four IDT7202 (1Kx9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7201s and IDT7202s fabricated in IDT's high-performance CEMOS technology.

IDT's military FIFO modules have semiconductor components 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



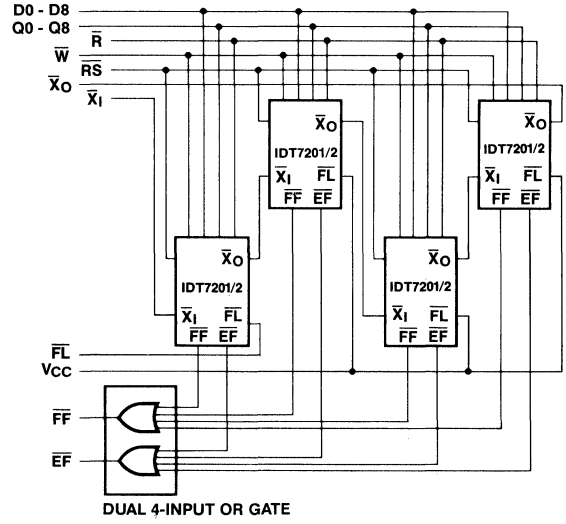
DIP
TOP VIEW

SSD7M203-001

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATA IN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATA OUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85°	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M203S IDT7M204S COMMERCIAL			IDT7M203S IDT7M204S MILITARY			UNIT	NOTES
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_{IL}	Input Leakage Current (Any Input)	-5	—	5	-10	—	10	μA	1
I_{OL}	Output Leakage Current	-10	—	10	-10	—	10	μA	2
V_{OH}	Output Logic "1" Voltage I_H = -2mA	2.4	—	—	2.4	—	—	V	—
V_{OL}	Output Logic "0" Voltage I_L = 8mA	—	—	0.4	—	—	0.4	V	—
I_{CC1}	Average V_{CC} Power Supply Current	—	110	176	—	155	230	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ = V_{IH})	—	20	33	—	30	60	mA	3
I_{CC3}	Power Down Current (All Input = V_{CC} -0.2V)	—	—	20	—	—	36	mA	3

NOTES:
1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. I_{CC} measurements are made with outputs open.

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	40	pF

NOTE:
1. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS[1]

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

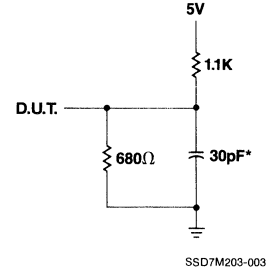
SYMBOL	PARAMETER	7M203/4S40 COM'L. ONLY		7M203/4S50		7M203/4S55		7M203/4S65		7M203/4S100		7M203/4S140		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_A	Access Time	—	40	—	50	—	55	—	65	—	100	—	140	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{RPW}	Read Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3,4]	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	25	—	30	—	30	—	35	—	40	—	50	ns
t_{WC}	Write Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_{WPW}	Write Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{DS}	Data Setup Time	20	—	25	—	30	—	40	—	50	—	50	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	70	—	85	—	125	—	165	—	ns
t_{RS}	Reset Pulse Width[2]	40	—	50	—	55	—	65	—	100	—	140	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	25	—	25	—	ns
t_{EFL}	Reset to Empty Flag Low	—	45	—	65	—	70	—	85	—	125	—	165	ns
t_{REF}	Read Low to Empty Flag Low	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{RFF}	Read High to Full Flag High	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{WEF}	Write High to Empty Flag High	—	45	—	50	—	55	—	60	—	95	—	135	ns
t_{WFF}	Write Low to Full Flag Low	—	45	—	50	—	55	—	60	—	95	—	135	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

NOTE:
Generating $\overline{R}/\overline{W}$ Signals — When using these high-speed FIFO devices, it is necessary to have clean inputs on the $\overline{R}$ and $\overline{W}$ signals. It is important to not have glitches, spikes or ringing on the $\overline{R}$, $\overline{W}$ lines (violates the V_{IH}, V_{IL} requirements); although the minimum pulse width low for the $\overline{R}$ and $\overline{W}$ are specified in tens of nanosecond, a glitch of 5ns can affect the read or write pointer and cause it to increment.



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*Includes jig and scope capacitances.

Figure 1. Output Load.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D0-D8)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2: i.e., t_{RPW} or t_{WPW} before the rising edge of $\overline{RS}$, and $\overline{W}$ should not change until t_{RSR} after the rising edge of $\overline{RS}$.

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a First-In, First-Out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the data outputs (Q0 through Q8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF}, and a valid READ can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$; so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD ($\overline{FL}$)

This pin is grounded to indicate that it is the first device. In the multiple mode (depth expansion mode) application, this pin on the rest of the devices should connect to V_{CC} for proper operation.

EXPANSION IN ($\overline{XI}$)

EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper application.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

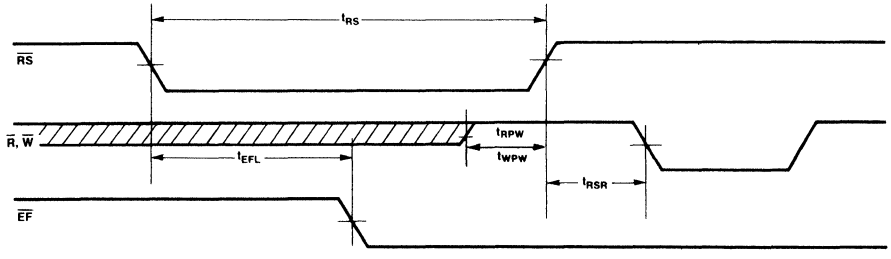
The FULL FLAT ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indiciating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 2048 writes for the IDT7M203 and 4096 writes for the IDT7M204.

EXPANSION OUT ($\overline{XO}$)

EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expanion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q0-Q8)

Data outputs for 9-bit wide data. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.



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NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

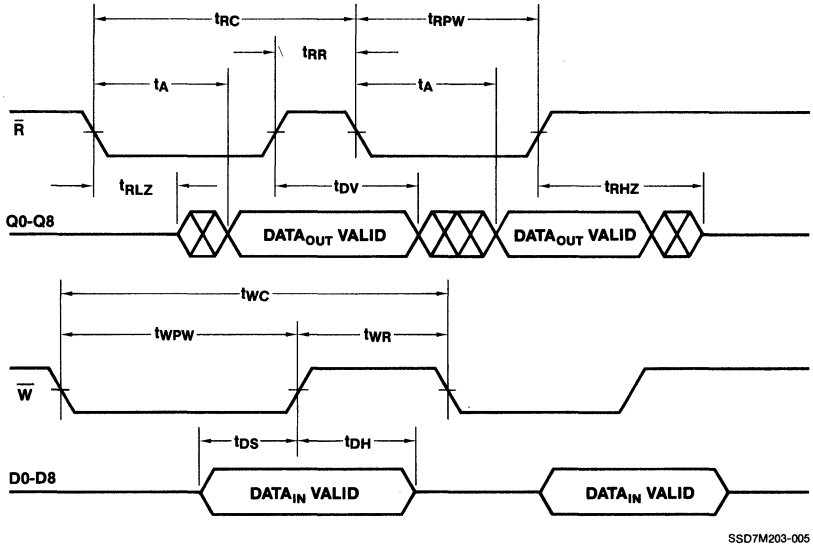


Figure 3. Asynchronous Write and Read Operation

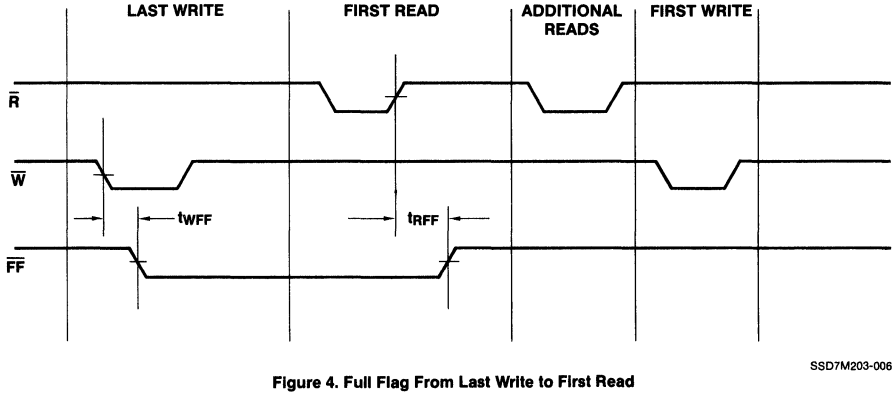


Figure 4. Full Flag From Last Write to First Read

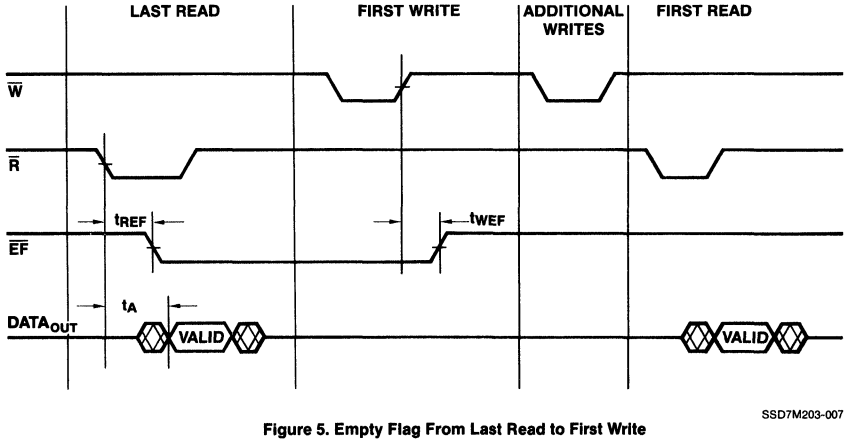
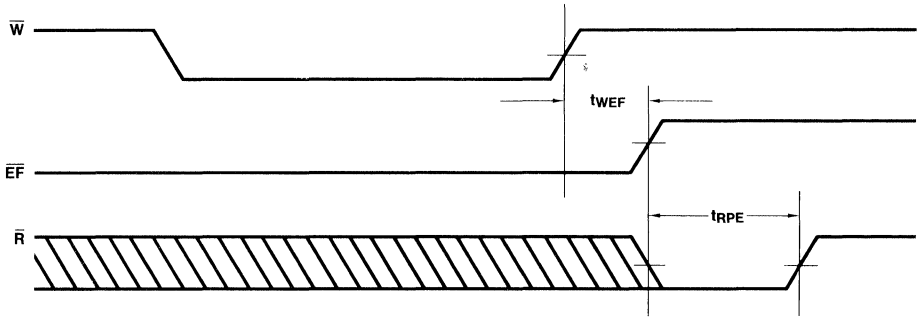


Figure 5. Empty Flag From Last Read to First Write

t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH



NOTE:
1. ($t_{RPE} = t_{RPW}$)

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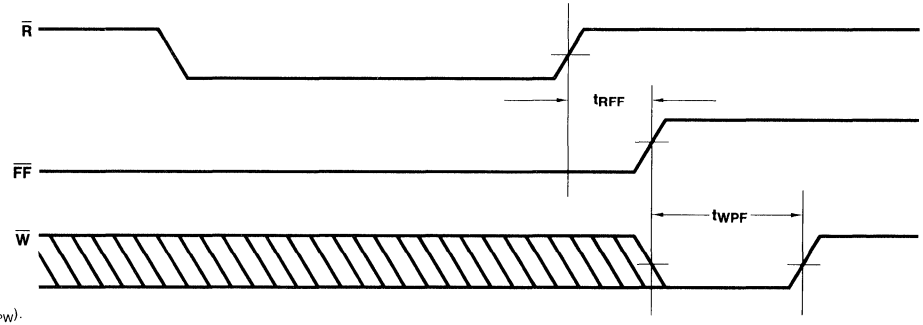
Figure 6. Empty Flag Timing

t_{WPF}: EFFECTIVE WRITE PULSE WIDTH AFTER FULL FLAG HIGH



NOTE:
1. ($t_{WPF} = t_{WPW}$).

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Figure 7. Full Flag Timing

OPERATING MODES:
SINGLE DEVICE MODE

A single IDT7M203/IDT7M204 may be used when the application requirements are for 2048/4096 words or less. The IDT7M203/IDT7M204 is a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7M203/ IDT7M204s. Any word width can be attained by adding additional IDT7M203/IDT7M204s.

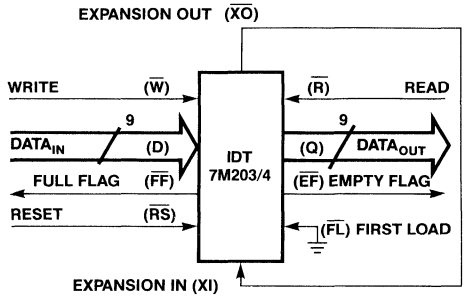

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Figure 8. Block Diagram of Single IDT7M203/IDT7M204 FIFO

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7M203/IDT7M204 can easily be adapted to applications when the requirements are for greater than 2048/4096 words. Figure 10 demonstrates Depth Expansion using three IDT7M203/IDT7M204s. Any depth can be attained by adding additional IDT7M203/IDT7M204s. The IDT7M203/IDT7M204 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. See Figure 10.
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 10.

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays. (See Figure 11.)

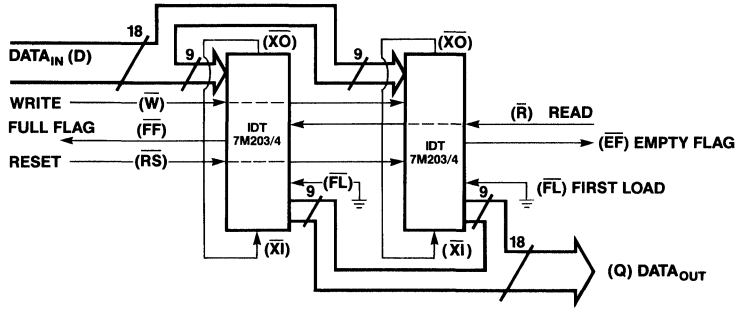
BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7M203/IDT7M204s as is shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7M203/IDT7M204: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ}ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge would deassert the empty flag); however, the same word (written on the first edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In a write flow-through mode (Figure 14), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted, but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, a new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and increment the write pointer.



NOTES:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 2048x18/4096x18 FIFO Memory Used in Width Expansion Mode

TABLE I — RESET — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUT	INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset	0	Location Zero	Location Zero	0	1
Read/Write	1	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II — RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 10.

$\overline{RS}$ = Reset Input, $\overline{FL}$ = First Load, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

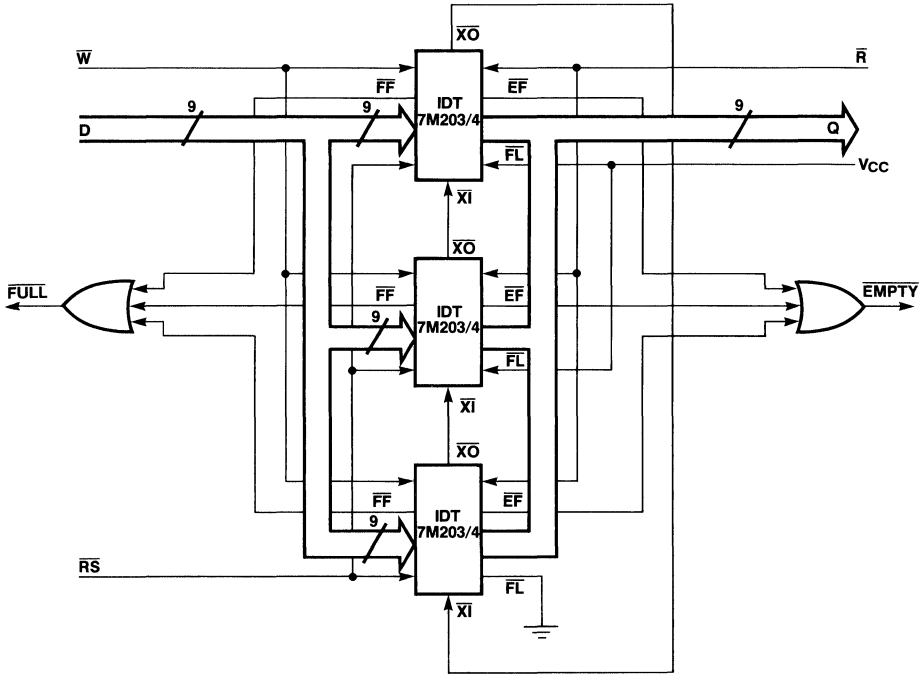


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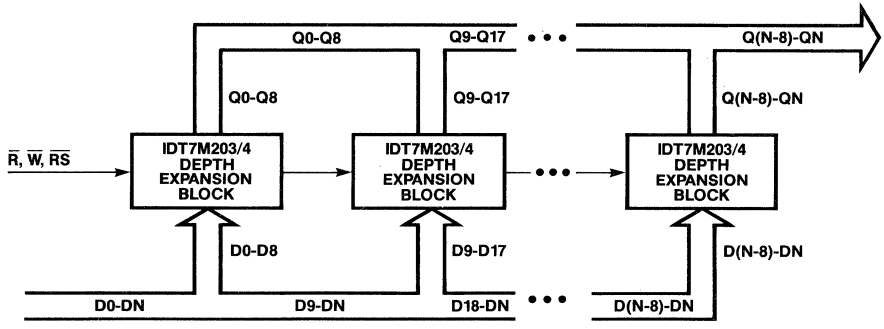
Figure 10. Block Diagram of 6144x9/12288x9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For flag detection see WIDTH expansion Section and Figure 9.

Figure 11. Compound FIFO Expansion

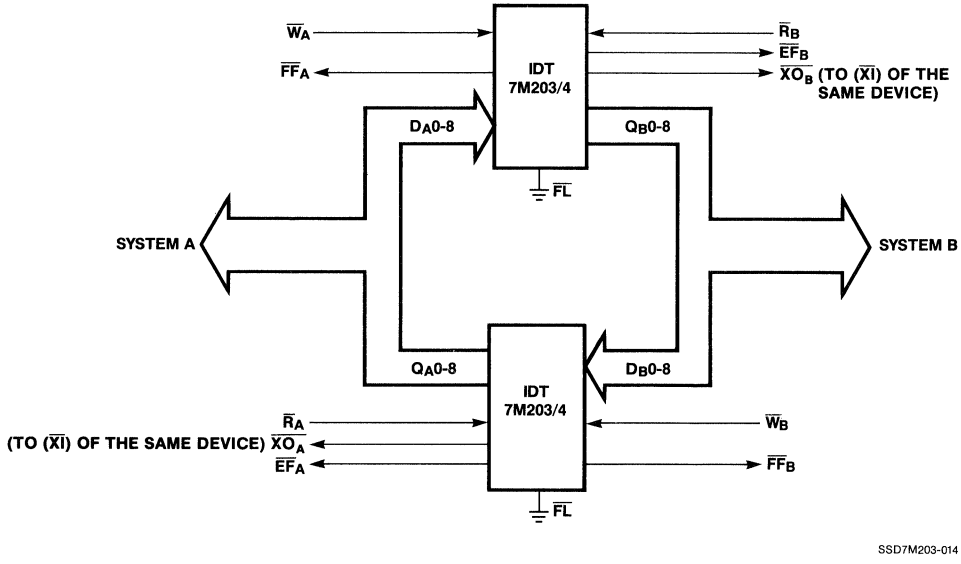
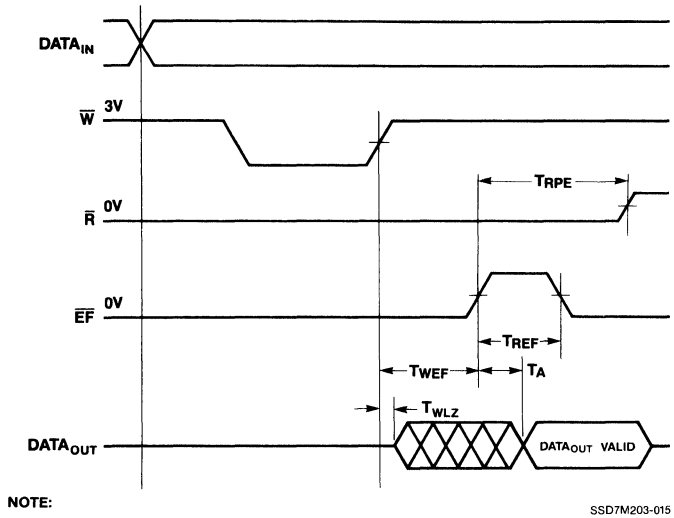
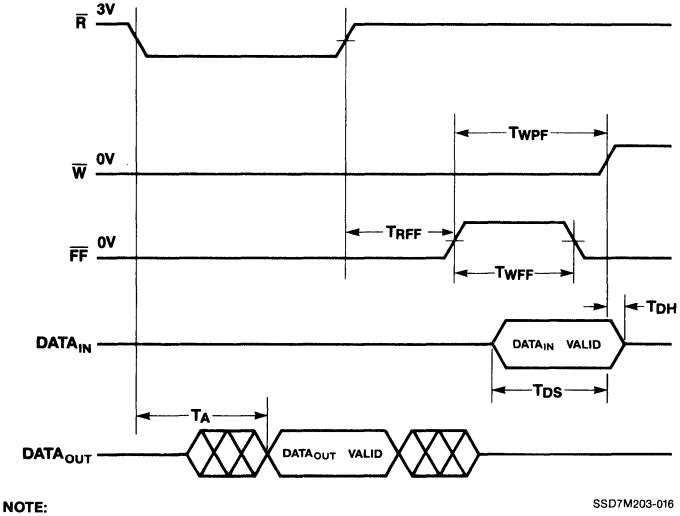


Figure 12. Bidirectional FIFO Mode



NOTE:
($T_{RPE} = T_{RPW}$)

Figure 13. Read Data Flow-Through Mode



NOTE:
($T_{WPF} = T_{WPW}$)

Figure 14. Write Data Flow-Through Mode

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