Integrated Device Technology, Inc.

1 MEGABIT CMOS STATIC RAM MODULE

IDT7M624S

FEATURES:

- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  - —Military: 45ns (max.)
  - —Commercial: 30ns (max.)
- Low power consumption
  - — Active 4.8W (typ. in 64K x 16 organization)
  - — Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Pin compatible with IDT7M656 (256K RAM module)
- Single 5V (±10%) power supply
- Dual GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M624 is a 1024K-bit high-speed CMOS static RAM constructed on a multi-layered ceramic substrate using 16 IDT7187 (64K x 1) static RAMs in leadless chip carriers. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

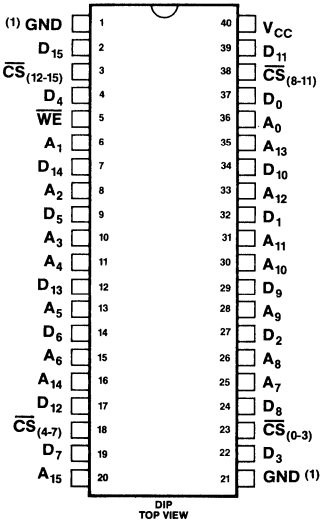
The IDT7M624 is available with access times as fast as 30ns commercial and 45ns military temperature range, with maximum operating power consumption of only 10.7W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.5W (max.) and a full standby mode of 1.7W (max.).

The IDT7M624 is offered in a 40-pin, 900 mil center sidebraze DIP to take advantage of the compact IDT7187s in leadless chip carriers.

All inputs and outputs of the IDT7M624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



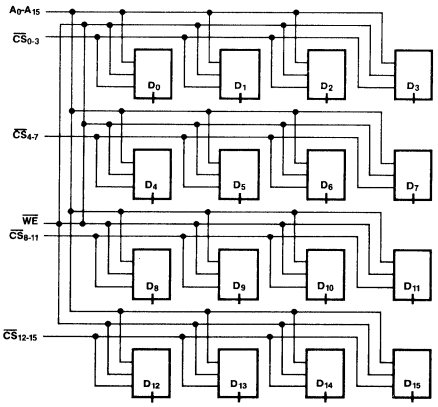
DIP
TOP VIEW

PIN NAMES

A_{0-16}	Addresses
I/O_{1-8}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

NOTE:
1. Both GND pins need to be grounded for proper operation.

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	8	8	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M624S			UNIT
			MIN.	TYP.(1)	MAX.	
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	20	µA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}_{XX}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = fMax.	—	960	1950	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	720	1380	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, Min. Duty Cycle = 100%	—	600	1100	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX} \geq V_{IH}$, (TTL Level), V_{CC} = 5.5V, Output Open	—	480	820	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V (CMOS Level)	—	0.32	320(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V	—	—	0.5	V
		I_{OL} = 8mA, V_{CC} = 4.5V	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = 4.5V	2.4	—	—	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. I_{SB1} max. at commercial temperature = 240 mA.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

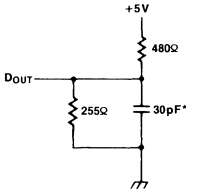


Figure 1. Output Load

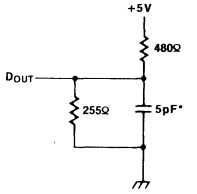


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M624S30 COM'L ONLY MIN.	MAX.	IDT7M624S45 MIN.	MAX.	IDT7M624S55 MIN.	MAX.	IDT7M624S65 MIN.	MAX.	IDT7M624S85 MIN.	MAX.	UNIT
READ CYCLE												
t_{RC}	Read Cycle Time	30	—	45	—	55	—	65	—	85	—	ns
t_{AA}	Address Access Time	—	30	—	45	—	55	—	65	—	85	ns
t_{ACS}	Chip Select Access Time	—	30	—	45	—	55	—	65	—	85	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High Z	—	25	—	30	—	30	—	30	—	4υ	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Selection to Power Down Time	—	30	—	35	—	35	—	35	—	40	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	30	—	45	—	55	—	65	—	85	—	ns
t_{CW}	Chip Selection to End of Write	25	—	40	—	50	—	55	—	65	—	ns
t_{AW}	Address Valid to End of Write	25	—	40	—	50	—	55	—	65	—	ns
t_{AS}	Address Setup Time	3	—	5	—	5	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	35	—	40	—	45	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	20	—	25	—	25	—	30	—	35	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	0	25	0	30	0	30	0	35	0	40	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

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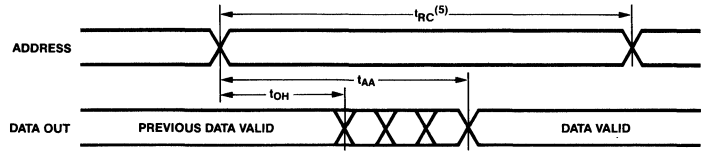
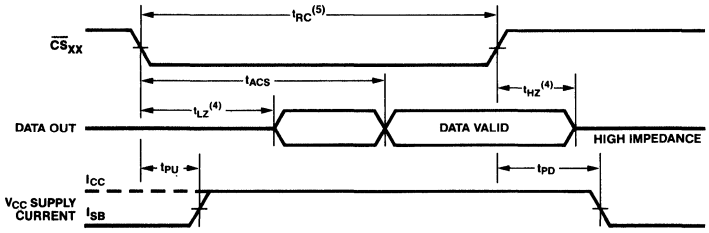
TIMING WAVEFORM OF READ CYCLE NO. 1(1,2)



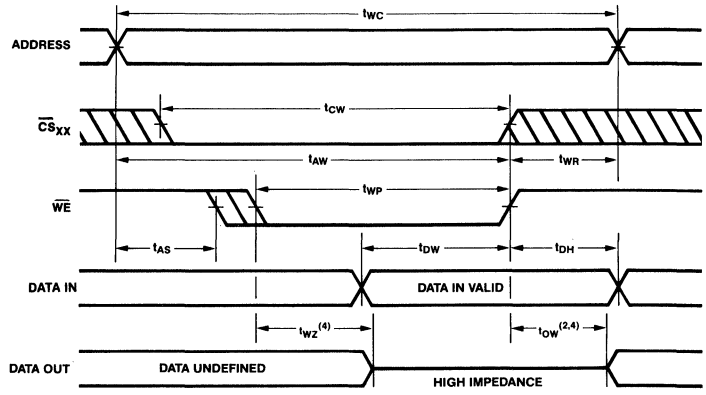
TIMING WAVEFORM OF READ CYCLE NO.2(1,3)



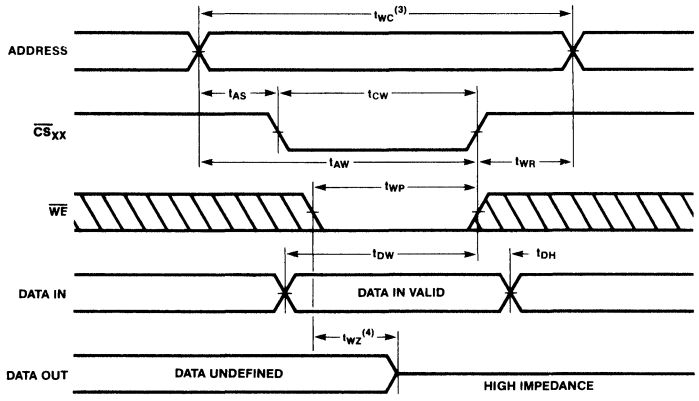
NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transititioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



NOTES:

1. $\overline{CS}_{XX}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}_{XX}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}_{XX}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	130	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE:

1. This parameter is sampled and not 100% tested.

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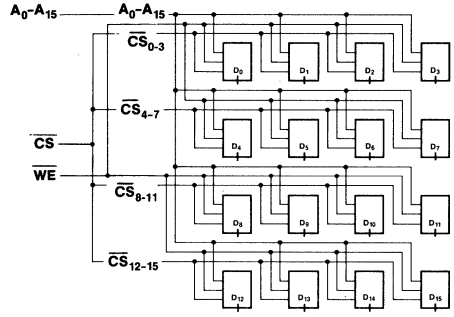
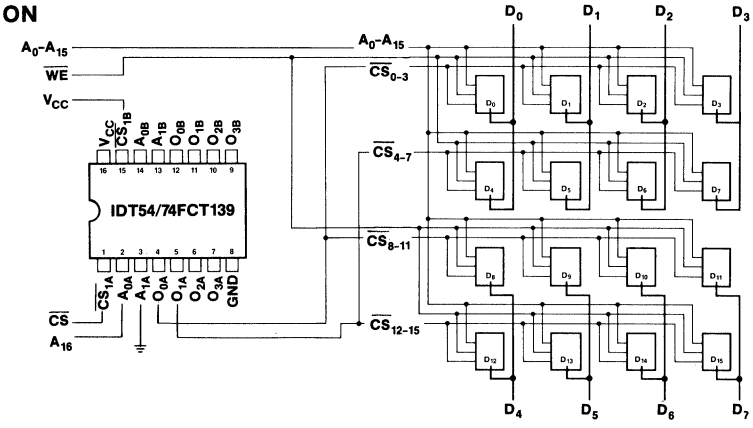
IDT7M624
64K x 16 CONFIGURATION



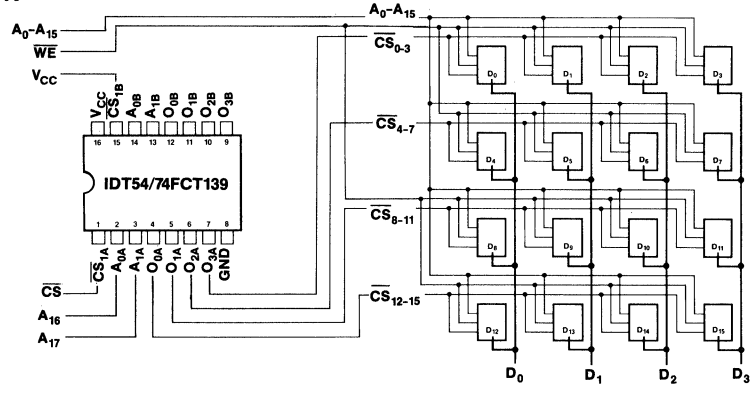
NOTE:
All chips selects tied together since, in a by 16 configuration, all chips are either on or off.

IDT7M624
128K x 8 CONFIGURATION



NOTE:
The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{16}) to determine which of the two banks of memory are enabled.

IDT7M624
256K x 4 CONFIGURATION



NOTE:
Each chip select is now controlled by the two higher order address pins A_{16} and A_{17}.