Integrated Device Technology, Inc.

256K CMOS STATIC RAM MODULE

IDT7M656L

FEATURES:

- High-density 256K-bit CMOS static RAM Module
- Customer-configured to 16Kx16, 32Kx8 or 64Kx4
- Fast access times
  - —Commercial — 25ns
  - —Military — 35ns
- Low-power consumption
  - —Active: 3.2W (typ.) (in 16K x 16 organization)
  - —Standby: 0.16mW (typ.)
- Utilizes 16 IDT6167s — high-performance 16K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in 40-pin, 900 mil center sidebraze DIP, achieving very high memory density
- Single 5V (±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Module available with components 100% screened to MIL-STD-883, Class B

DESCRIPTION:

The IDT7M656 is a 256K-bit high-speed CMOS static RAM constructed on a multilayered ceramic substrate using 16 IDT6167 (16Kx1) static RAMs in leadless chip carriers. Making 4 chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 16Kx16, 32Kx8 or 64Kx4 organization. In addition, extremely high speeds are achievable by the use of IDT6167s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides some of the fastest 16K static RAMs available.

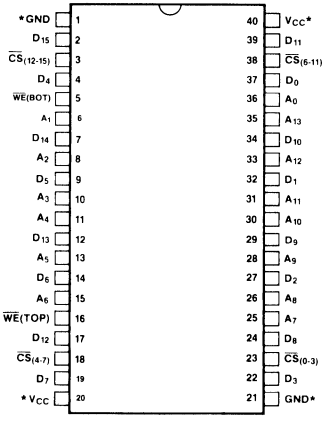
The IDT7M656 is available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 7.0W (significantly less if organized 32K x 8 or 64K x 4). The RAM Module also offers a maximum standby power mode of 2.2W and a maximum full standby mode of 82.5mW.

The IDT7M656 is offered in a high-density 40-pin, 900 mil center sidebraze DIP to take full advantage of the compact IDT6167s in leadless chip carriers.

All inputs and outputs of the IDT7M656 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Full asyncronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

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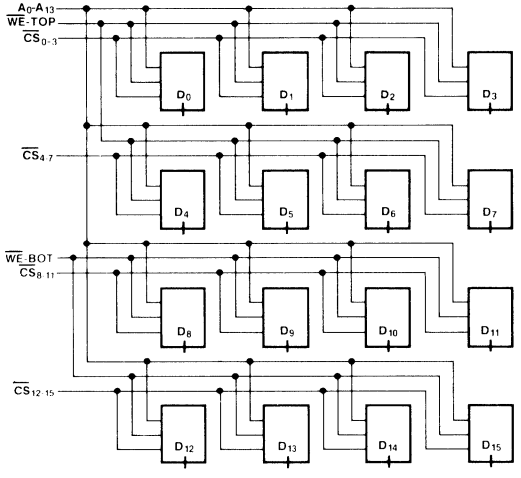
* Both V_{CC} pins need to be connected to the 5V Supply, and both GND pins need to be grounded for proper operation.

PIN NAMES

A_{XX}	ADDRESSES	D_{XX}	DATA IN/OUT
$\overline{CS}_{XX}$	CHIP SELECTS	V_{CC}	POWER
$\overline{WE}_{XX}$	WRITE ENABLES	GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	8.0	8.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} min = -1.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M656L MIN.	TYP.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	20	µA
I_{CCX16}	Operating Current in X16 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	640	1280	mA
I_{CCX8}	Operating Current in X8 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	420	840	mA
I_{CCX4}	Operating Current in X4 mode	$\overline{CS}_{XX}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	310	620	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	200	400	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}_{XX}$ ≥ V_{CC} - 0.2V (CMOS Level) V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.032	15(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	—	V

NOTES

1. V_{CC} = 5V, T_A = +25°C
2. I_{SB1} max. at commercial temperature = 5.0mA

TRUTH TABLE

MODE	$\overline{CS}_{XX}$	$\overline{WE}_{XX}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	200	pF
C_{OUT}(2)	Output Capacitance	V_{OUT} = 0V	60	pF

NOTES:

1. This parameter is sampled and not 100% tested.
2. For each output, 16K x 16 mode.

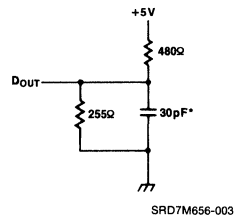


Figure 1. Output Load

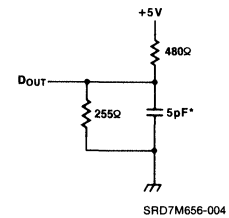


Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

***Including scope and jig.**

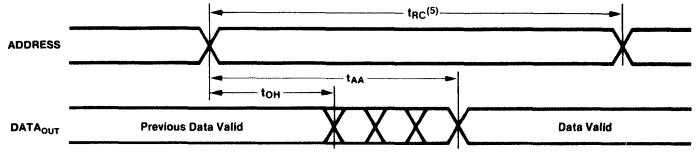
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V 10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7M656L25[1] COM'L. ONLY MIN.	MAX.	IDT7M656L35 MIN.	MAX.	IDT7M656L55 MIN.	MAX.	IDT7M656L65 MIN.	MAX.	IDT7M656L85 MIN.	MAX.	IDT7M656L100 MIL. ONLY MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	25	—	35	—	55	—	65	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	55	—	65	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	—	55	—	65	—	85	—	100	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{LZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselect to Output in High Z	—	15	—	20	—	40	—	40	—	50	—	50	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Select to Power Down Time	—	25	—	35	—	55	—	65	—	85	—	100	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	—	35	—	55	—	65	—	85	—	100	—	ns
t_{CW}	Chip Select to End of Write	20	—	30	—	45	—	55	—	65	—	80	—	ns
t_{AW}	Address Valid to End of Write	25	—	35	—	45	—	55	—	65	—	80	—	ns
t_{AS}	Address Setup Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	35	—	40	—	45	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	15	—	20	—	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold Time	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WZ}	Write Enable to Output in High Z	—	10	—	15	—	40	—	40	—	50	—	50	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

1. IDT7M656L25 will not have low V_{CC} data retention characteristics.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]



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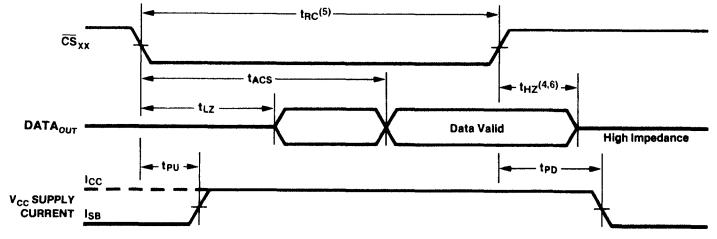
TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

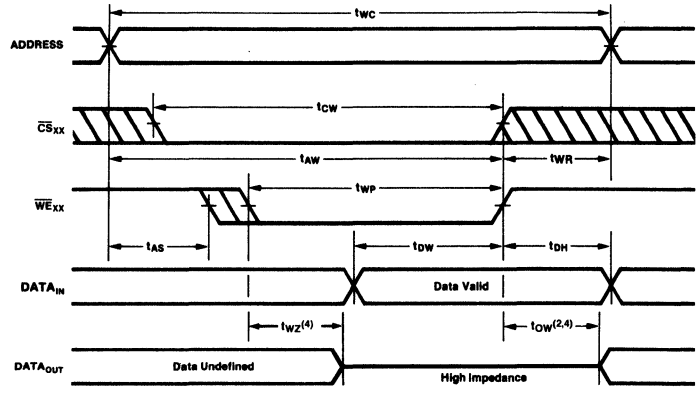


SRD7M656-006

NOTES:

1. $\overline{WE}_{XX}$ is high for READ cycle.
2. $\overline{CS}_{XX}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}_{XX}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.
6. For any given speed grade, operating voltage, and temperature, t_{HZ} will be less than or equal to t_{LZ}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



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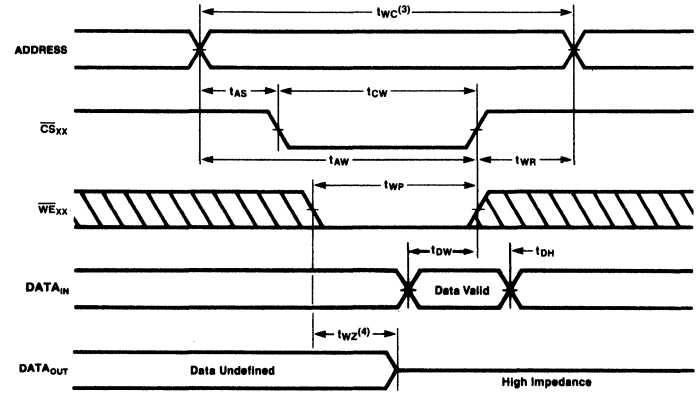
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



SRD7M656-008

NOTES:

1. $\overline{CS}_{XX}$ or $\overline{WE}_{XX}$ must be high during address transitions.
2. If $\overline{CS}_{XX}$ goes high simultaneously with $\overline{WE}_{XX}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.

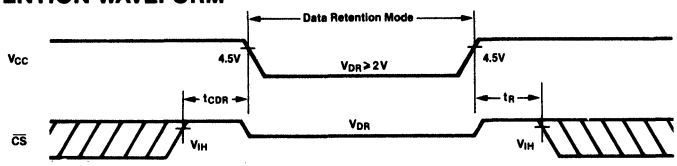
LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = -55°C to +125°C and 0°C to +70°C) (Except IDT7M656L25)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.(1)	MAX. COM'L.	MAX. MIL.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS}_{XX} \geq V_{CC} - 0.2V$	—	.01(2)	2.0(2)	6.0	mA
		$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	—	.02(3)	3.0(3)	9.0	
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	—	ns

NOTES:

1. T_A = +25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



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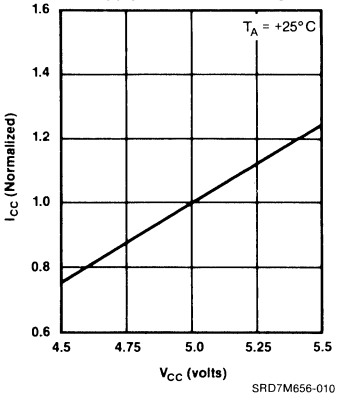
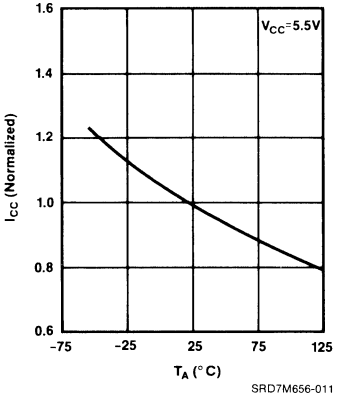
NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs. Voltage



SRD7M656-010

Supply Current vs. Ambient Temperature



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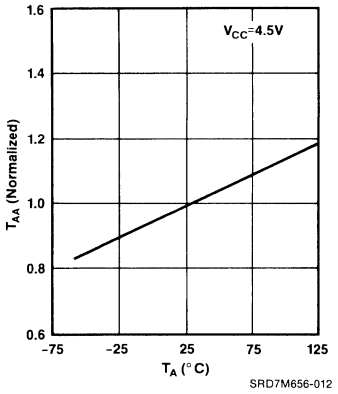
Address Access Time vs. Ambient Temperature



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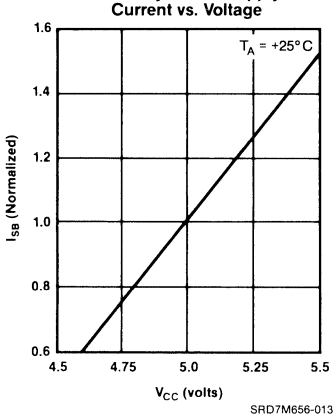
Stand-by Power Supply Current vs. Voltage



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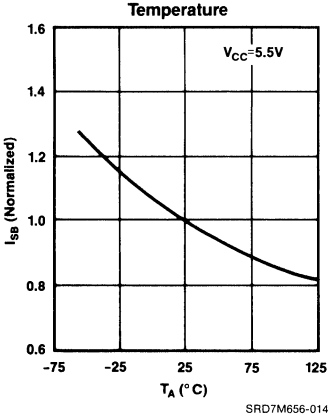
Stand-by-Power Supply Current vs. Ambient Temperature



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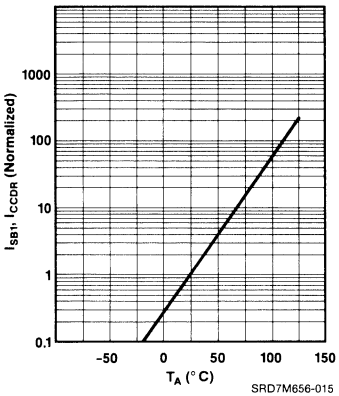
Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature



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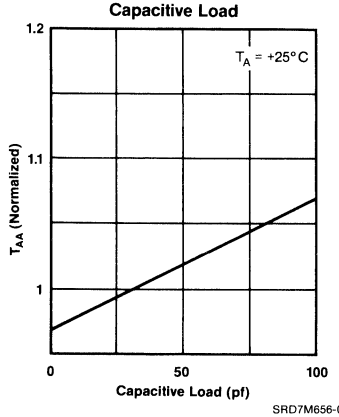
Address Access Time vs. Capacitive Load



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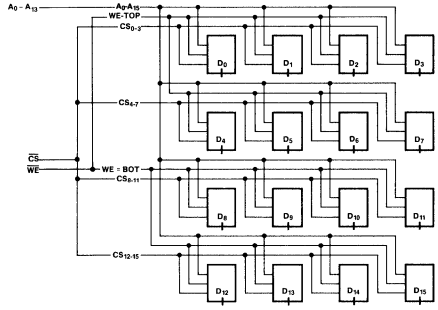
IDT7M656

16K x 16 CONFIGURATION



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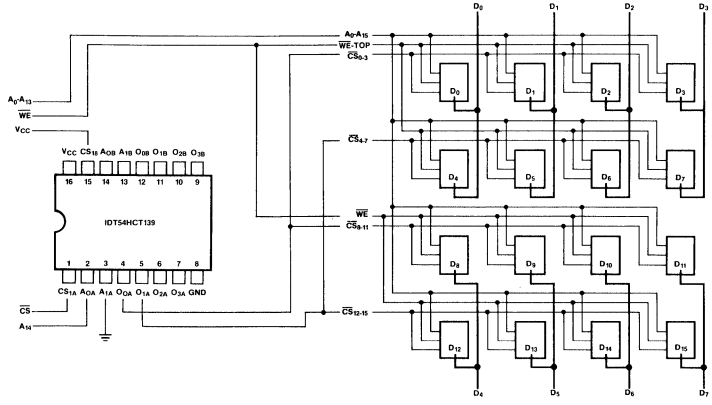
NOTES:

1. All chip selects tied together since, in a by 16 configuration, all chips are either on or off.
2. The two write enables are tied together allowing control of the write enable for entire memory at one time (necessary) in a by 16 organization since all chips are either writing or reading at any given time.

32K x 8 CONFIGURATION



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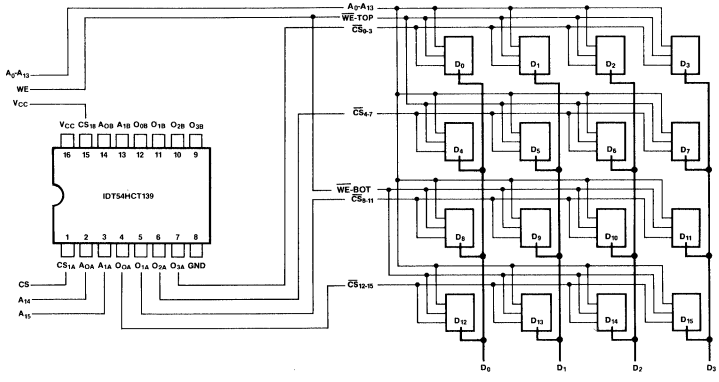
NOTES:

1. The chip selects are tied together in groups of two. The decoder uses the new higher order address pin (A_{14}) to determine which of the two banks of memory are enabled.
2. The two write enables are tied together for ease of layout. They could be controlled by the decoder similar to the chip selects but would save only a minimal amount of power and add complexity to the layout.

64K x 4 CONFIGURATION



SRD7M656-019

NOTES:

1. Each chip select is now controlled by the two higher order address pins A_{14} (necessary in 64K deep memory).
2. Again the two write enables are tied together for ease of layout (the megabit part will only have one write enable pin).