Integrated Device Technology, Inc.

512K (64K x 8-BIT or 64K x 9-BIT) CMOS STATIC RAM MODULE

IDT 7M812
IDT 7M912

FEATURES:

- High-density 512K-bit CMOS static RAM module
- 64K x 8 (IDT7M812) or 64K x 9 (IDT7M912) configuration
- Fast access times
  - Military: 35ns (max.)
  - Commercial: 25ns (max.)
- Low power consumption
  - Active: 2.4W (typ. in 64K x 8 organization)
  - Standby: 240µW (typ. in 64K x 8 organization)
- Utilizes 8 (IDT7M812) or 9 (IDT7M912) IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Available in 40-pin, 600 mil center sidebraze DIP, achieving very high memory density
- Single 5V(±10%) power supply
- Dual V_{CC} and GND pins for maximum noise immunity
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters

DESCRIPTION:

The IDT7M812/IDT7M912 are 512K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using 8 IDT7187 64K x 1 static RAMs (IDT7M812) or 9 IDT7187 static RAMs (IDT7M912) in leadless chip carriers. Extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

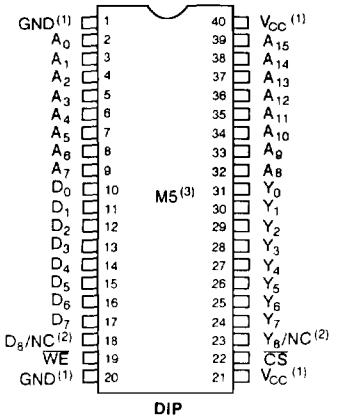
The IDT7M812/IDT7M912 are available with access times as fast as 25ns commercial and 35ns military temperature range, with maximum operating power consumption of only 6.9W (IDT7M912, 64K x 9 option). The module also offers a standby power mode of less than 3.2W (max.) and a full standby mode of 1.2W (max.).

The IDT7M812/IDT7M912 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7187s in leadless chip carriers. The IDT7M912 (64K x 9) option can provide more flexibility in system application for error detection, parity bit, etc.

All inputs and outputs of the IDT7M812/IDT7M912 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing access and cycles times for ease of use.

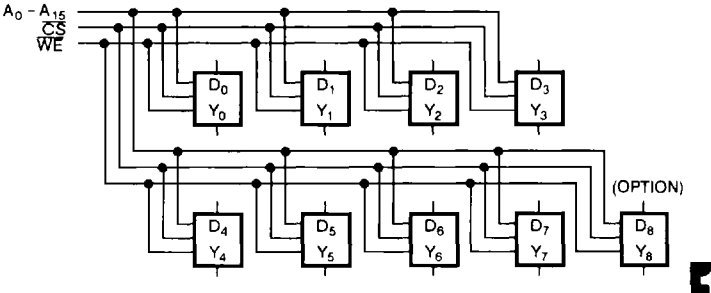
All IDT military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	Address
D_0-D_8	Data Input
Y_0-Y_8	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
GND	Ground

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.
2. Pin 18 is D_8 and pin 23 is Y_8 in 64K x 9 (IDT7M912) option and both 18 and 23 are NC in 64K x 8 (IDT7M812) option.
3. For module dimensions, please refer to module drawing M5 in the packaging section.

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ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7M912 MIN.	IDT7M912 TYP.	IDT7M912 MAX.[3]	IDT7M912 MAX.[4]	IDT7M812 MIN.	IDT7M812 TYP.	IDT7M812 MAX.[3]	IDT7M812 MAX.[4]	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	–	–	20	20	–	–	20	20	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	20	20	–	–	20	20	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open Min. Duty Cycle = 100%	–	540	1080	1260	–	480	960	1120	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100% Output Open	–	540	1080	1530	–	480	960	1360	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$ Min. Duty Cycle = 100%	–	270	450	585	–	240	400	520	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or ≤ 0.2V	–	0.2	180[2]	225	–	0.05	160[2]	200	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.	–	–	0.5	0.5	–	–	0.5	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	–	–	0.4	0.4	–	–	0.4	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	–	–	–	2.4	–	–	–	V

NOTES:

1. Typical limits are at V_{CC} = 5.0V, +25°C.
2. I_{SB1} (max.) of IDT7M812/912 at commercial temperature = 80mA/90mA.
3. t_{AA} = 30, 35, 45, 55ns
4. t_{AA} = 25ns

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

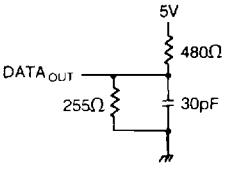

Figure 1. Output Load

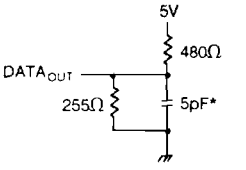

Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7M912S25 7M812S25 COM'L. ONLY		7M912S30 7M812S30 COM'L. ONLY		7M912S35 7M812S35		7M912S45 7M812S45		7M912S55 7M812S55		7M912S65 7M812S65		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{AA}	Address Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{ACS}	Chip Select Access Time	–	25	–	30	–	35	–	45	–	55	–	65	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{LZ}	Chip Selection to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{HZ}	Chip Deselection to Output in High Z	–	20	–	25	–	25	–	30	–	30	–	30	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Selection to Power Down Time	–	25	–	30	–	35	–	35	–	35	–	35	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	55	–	65	–	ns
t_{CW}	Chip Selection to End of Write	23	–	28	–	35	–	40	–	50	–	55	–	ns
t_{AW}	Address Valid to End of Write	23	–	28	–	35	–	40	–	50	–	55	–	ns
t_{AS}	Address Set-up Time	3	–	3	–	5	–	5	–	5	–	5	–	ns
t_{WP}	Write Pulse Width	20	–	25	–	30	–	30	–	35	–	40	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DW}	Data Valid to End of Write	15	–	20	–	20	–	25	–	25	–	30	–	ns
t_{DH}	Data Hold Time	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output in High Z	0	20	0	25	0	25	0	30	0	30	0	35	ns
t_{OW}	Output Active from End of Write	0	–	0	–	0	–	0	–	0	–	0	–	ns

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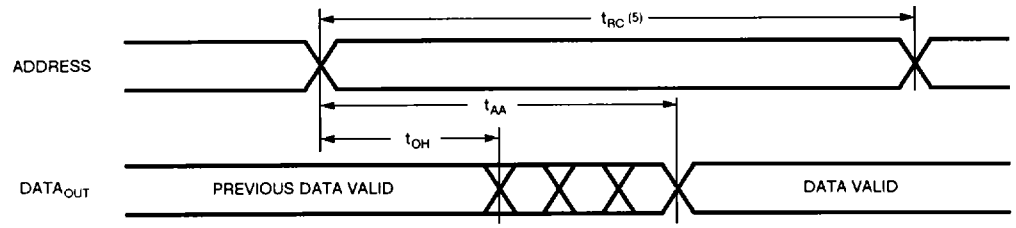
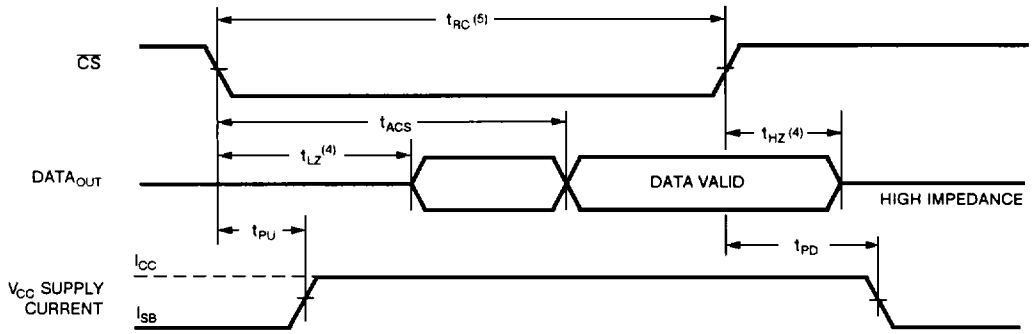
TIMING WAVEFORM OF READ CYCLE NO. 1 [1, 2]



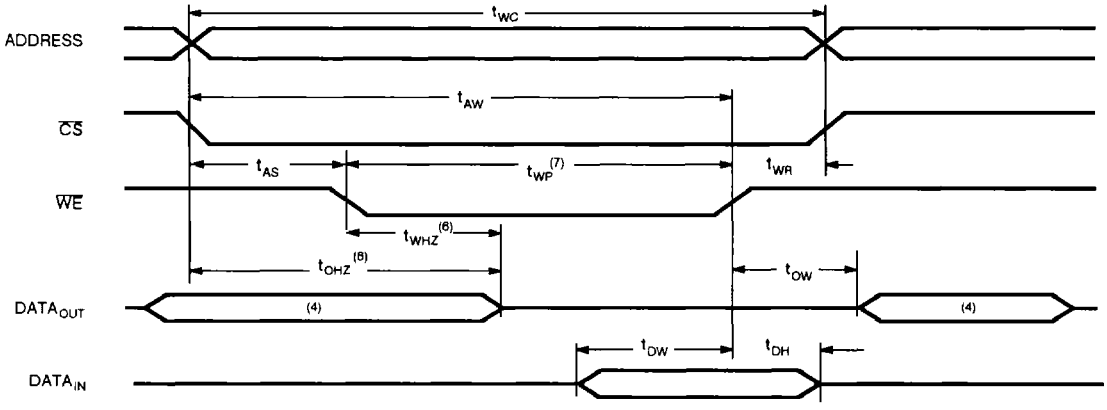
TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 3]



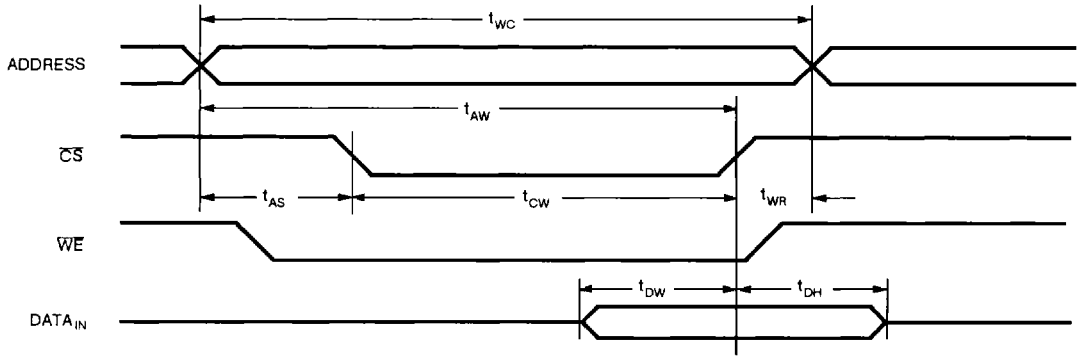
NOTES:

1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]



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NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	TEST	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	80	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION