Integrated Device Technology, Inc.

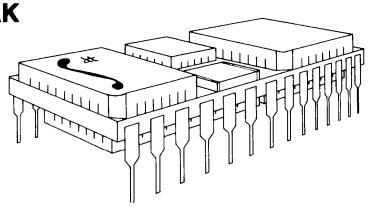
# 64K (8K x 8) CMOS STATIC RAMPAK

# IDT7M864 IDT8M864

## FEATURES:

- Equivalent to JEDEC standard 8K x 8 monolithic RAM
- 8,192 x 8 CMOS static RAM module complete with decoder and decoupling capacitor
- High-speed 65 (commercial only) 75/85/120/150/200ns (equal access and cycle times)
- Low power consumption, less than 1 watt maximum
- Two pinout options (64K EPROM & 64K static RAM)
- Utilizes IDT6116s — high performance 16K RAMs produced with advanced CEMOS™I technology
- CEMOS I process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Military modules available with semiconductor components 100% screened to MIL-STD-883 Class B

## 64K RAMPAK



The IDT7M864/IDT8M864 are available with access times as fast as 65ns for commercial and 75ns for military temperature ranges, with maximum power consumption of only 990mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ high and/or $CS_2$ (7M864) goes low, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In the standby mode, the module consumes less than 440mW. Substantially lower power levels can be achieved in the $I_{SB1}$ mode (less than 20mW max.) and 2V data retention mode (less than 3mW max.) - see "DC Characteristics" and "Data Retention Characteristics" for details.

Pinout of the IDT8M864 is equivalent to the 64K EPROMs (no connect on pin 26), ideal for applications requiring easy micro-code changes during prototyping. The IDT7M864's pinout is compatible with monolithic 64K static RAMs ($CS_2$ on pin 26).

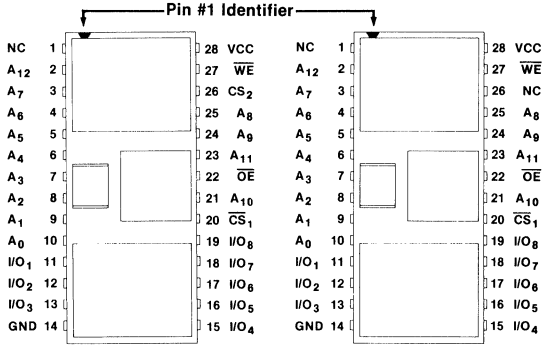
All inputs and outputs of the IDT7M864/IDT8M864 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Full asyncronous circuitry is used, requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT module semiconductor components are processed in compliance to the test methods of MIL-STD-883, as shown on back of data sheet, making them ideally, suited for applications demanding the highest level of performance and reliability.

## DESCRIPTION:

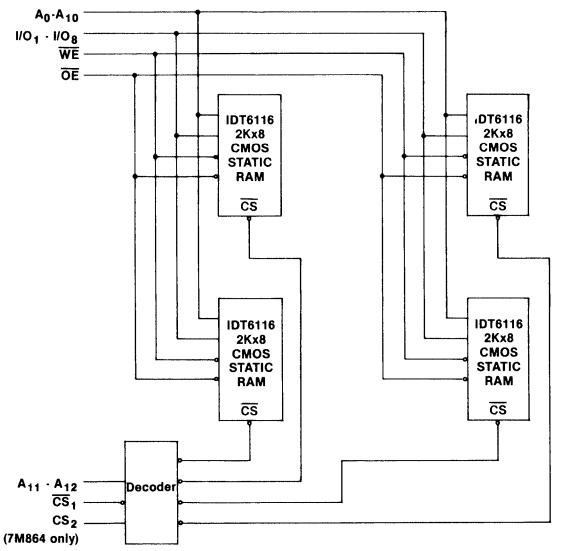
The IDT7M864/IDT8M864 are 64K (8,192 x 8 bit) high speed static RAMs constructed on a ceramic substrate using 4 IDT6116 (2,048 x 8) static RAMs in leadless chip carriers. Functional equivalence to a monolithic 64K static RAM is achieved by utilization of an on-board decoder circuit that interprets the higher order addresses $A_{11}$ and $A_{12}$ to select one of the four 2Kx8 RAMs. Extremely fast speeds can be achieved with this technique due to use of the IDT6116 fabricated in IDT's high performance, high-reliability technology — CEMOS™I. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 16K static RAMs available.

## PIN CONFIGURATIONS




7M864 8M864

## FUNCTIONAL BLOCK DIAGRAM




## PIN NAMES

| | | | |
|---|---|---|---|
| $A_0$-$A_{12}$ | ADDRESS | $\overline{WE}$ | WRITE ENABLE |
| $I/O_1$-$I/O_8$ | DATA INPUT/OUTPUT | $\overline{OE}$ | OUTPUT ENABLE |
| $\overline{CS}_1$, $CS_2$ | CHIP SELECT | GND | GROUND |
| $V_{CC}$ | POWER | | |

CEMOS is a trademark of Integrated Device Technology, Inc.

## TRUTH TABLE

| MODE | $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | $\overline{WE}$ | I/O OPERATION |
|---|---|---|---|---|---|
| Standby | H | X | X | X | High Z |
| Standby | X | L | X | X | High Z |
| Read | L | H | L | H | $D_{OUT}$ |
| Read | L | H | H | H | High Z |
| Write | L | H | X | L | $D_{IN}$ |

## RECOMMENDED DC OPERATING CONDITIONS

($T_A$ = −55°C to +125°C and 0°C to +70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | 3.5 | 6.0 | V |
| $V_{IL}$ | Input Low Voltage | −0.5 * | — | .65 | V |
| $C_L$ | Output Load | — | — | 100 | pF |
| TTL | Output Load | — | — | 1 | — |

*$V_{IL}$ min = −1.0V for pulse width less than 20ns.

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V ± 10%, $T_A$ = −55°C to +125°C and 0°C to +70°C)

| SYMBOL | PARAMETER | TEST CONDITIONS | IDT7M864/8M864 MIN. | TYP.(1) | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $\|I_{LI}\|$ | Input Leakage Current | $V_{CC}$ = 5.5V, $V_{IN}$ = 0V to $V_{CC}$ | — | — | 15 | µA |
| $\|I_{LO}\|$ | Output Leakage Current | $\overline{OE}$ or $\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$, $V_{OUT}$ = 0V to $V_{CC}$ | — | — | 15 | µA |
| $I_{CC}$ | Operating Power Supply Current | $\overline{CS_1} \leq V_{IL}$, $CS_2 \geq V_{IH}$, Output Open | — | 65 | 180 | mA |
| $I_{CC1}$ | Dynamic Operating Current | Min. Duty Cycle = 100% | — | 65 | 180 | mA |
| $I_{SB}$ | Standby Power Supply Current | $\overline{CS_1} \geq V_{IH}$, or $CS_2 \leq V_{IL}$ | — | 20 | 80 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current | $\overline{CS_1} \geq V_{CC}-0.2V$, and/or $CS_2 \leq 0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $\leq 0.2V$ | — | .016 | 3.6(2) | mA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4mA | — | — | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −1mA | 2.4 | — | — | V |

1. $V_{CC}$ = 5V, $T_A$ = 25°C
2. $I_{SB1}$ max at commercial temperature = 1.0 mA

## ABSOLUTE MAXIMUM RATINGS(1)

| SYMBOL | RATING | COMMERCIAL | MILITARY | UNIT |
|---|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | −0.5 to +7.0 | −0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | −55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | −10 to +85 | −65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | −55 to +125 | −65 to +150 | °C |
| $P_T$ | Power Dissipation | 4.0 | 4.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 10ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | 1 TTL Gate and $C_L$ = 100pF (including scope and jig) |

## CAPACITANCE ($T_A$ = 25°C, f = 1.0MHz)

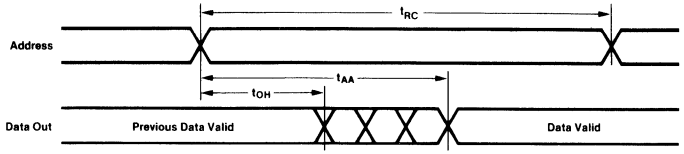
| SYMBOL | ITEM | CONDITIONS | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 28 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 33 | pF |

NOTE: This parameter is sampled and not 100% tested.

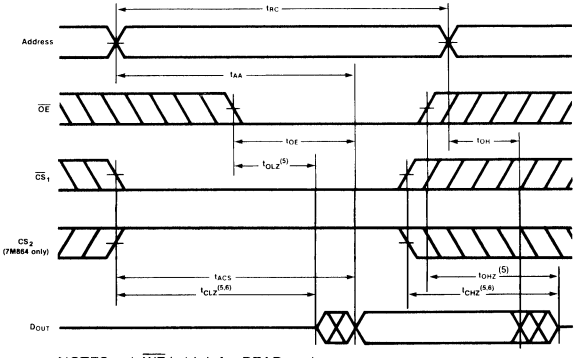
## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5V ± 10%, $T_A$ = −55°C to +125°C and 0°C to +70°C)

| SYMBOL | PARAMETER | IDT7M/8M864L65 COMMERCIAL ONLY | | IDT7M/8M864L75 | | IDT7M/8M864L85 | | IDT7M/8M864L120 | | IDT7M/8M864L150 | | IDT7M/8M864L200 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| **READ CYCLE** | | | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 65 | — | 75 | — | 85 | — | 120 | — | 150 | — | 200 | — | ns |
| $t_{AA}$ | Address Access Time | — | 65 | — | 75 | — | 85 | — | 120 | — | 150 | — | 200 | ns |
| $t_{ACS}$ | Chip Select Access Time | — | 65 | — | 75 | — | 85 | — | 120 | — | 150 | — | 200 | ns |
| $t_{CLZ}$ | Chip Selection to Output in Low Z | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| $t_{OE}$ | Output Enable to Output Valid | — | 50 | — | 55 | — | 65 | — | 65 | — | 80 | — | 100 | ns |
| $t_{OLZ}$ | Output Enable to Output in Low Z | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{CHZ}$ | Output Deselection to Output in High Z | — | 40 | — | 50 | — | 55 | — | 70 | — | 70 | — | 80 | ns |
| $t_{OHZ}$ | Chip Disable to Output in High Z | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | — | 50 | ns |
| $t_{OH}$ | Output Hold from Address Change | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| **WRITE CYCLE** | | | | | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 65 | — | 75 | — | 85 | — | 120 | — | 150 | — | 200 | — | ns |
| $t_{CW}$ | Chip Selection to End of Write | 55 | — | 65 | — | 65 | — | 80 | — | 100 | — | 120 | — | ns |
| $t_{AW}$ | Address Valid to End of Write | 60 | — | 70 | — | 70 | — | 85 | — | 100 | — | 120 | — | ns |
| $t_{AS}$ | Address Setup Time | 10 | — | 15 | — | 15 | — | 15 | — | 20 | — | 20 | — | ns |
| $t_{WP}$ | Write Pulse Width | 40 | — | 45 | — | 55 | — | 55 | — | 70 | — | 90 | — | ns |
| $t_{WR}$ | Write Recovery Time | 5 | — | 5 | — | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| $t_{OHZ}$ | Output Disable to Output in High Z | — | 30 | — | 35 | — | 40 | — | 40 | — | 40 | — | 50 | ns |
| $t_{WHZ}$ | Write to Output in High Z | 0 | 35 | 0 | 40 | 0 | 50 | 0 | 50 | 0 | 60 | 0 | 60 | ns |
| $t_{DW}$ | Data to Write Time Overlap | 25 | — | 30 | — | 30 | — | 30 | — | 35 | — | 40 | — | ns |
| $t_{DH}$ | Data Hold from Write Time | 5 | — | 10 | — | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| $t_{OW}$ | Output Active from End of Write | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 5 | — | ns |

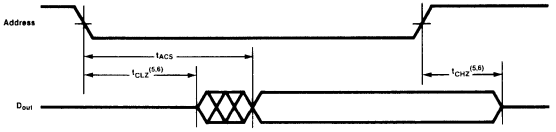
## TIMING WAVEFORM OF READ CYCLE NO. 1 (1,2,4)




## TIMING WAVEFORM OF READ CYCLE NO. 2 (1,3)

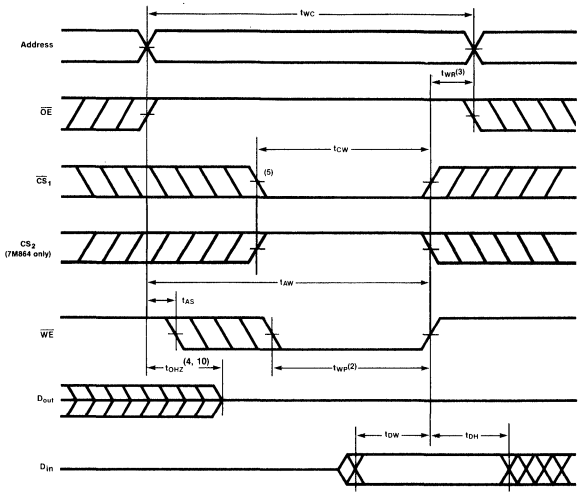



## TIMING WAVEFORM OF READ CYCLE NO. 3 (1,3,4)

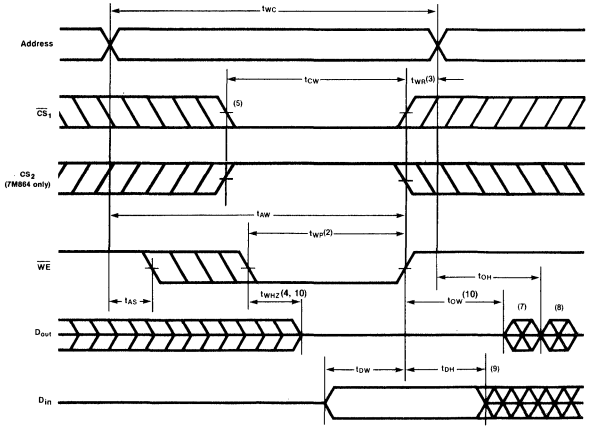



NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected, $\overline{CS}_1$ = $V_{IL}$, $CS_2$ = $V_{IH}$ (7M864 only).
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low, $CS_2$ transition high (7M864 only).
4. $\overline{OE}$ = $V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. For any given speed grade, operating voltage, and temperature, $t_{CHZ}$ will be less than or equal to $t_{CLZ}$.

## TIMING WAVEFORMS OF WRITE CYCLE 1[1]




## WRITE CYCLE 2[1,6]



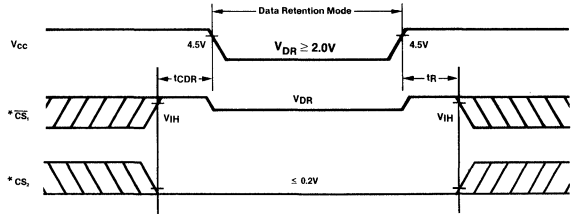

NOTES: 1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap ($t_{WP}$) of a low $\overline{CS_1}$, or high $CS_2$ (7M864 only) and a low $\overline{WE}$.
3. $t_{WR}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or $CS_2$ going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or $CS_2$ high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continously low ($\overline{OE}$ = $V_{IL}$).
7. $D_{OUT}$ is the same phase of write data of this write cycle.
8. $D_{OUT}$ is the read data of next address.
9. If $\overline{CS_1}$ is low or $CS_2$ is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

## LOW $V_{CC}$ DATA RETENTION CHARACTERISTICS ($T_A$ = −55°C to +125°C and 0°C to +70°C)

| SYMBOL | PARAMETER | TEST CONDITION | MIN. | TYP.[1] | MAX. COMM. | MAX. MIL. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2.0 | — | — | — | V |
| $I_{CCDR}$ | Data Retention Current | $\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \leq 0.2V$ | — | 2.0[2] | 350[2] | 1200[2] | µA |
| | | $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$ | — | 4.0[3] | 500[3] | 1800[3] | |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | — | — | — | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$[4] | — | — | — | ns |

NOTES: 1. $T_A$ = 25°C 3. at $V_{CC}$ = 3V
2. at $V_{CC}$ = 2.0V 4. $t_{RC}$ = Read Cycle Time

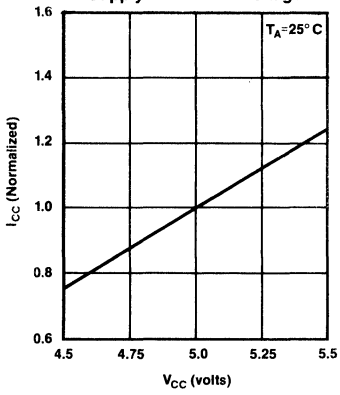
## LOW $V_{CC}$ DATA RETENTION WAVEFORM



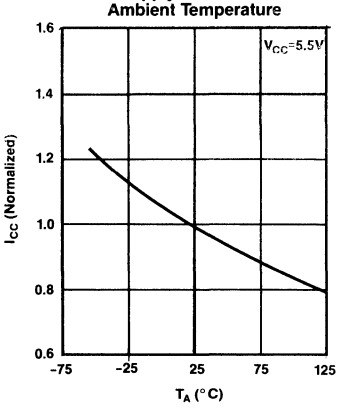

*Low $V_{CC}$ data retention achieved by the indicated $\overline{CS_1}$ waveform or $CS_2$ waveform.

## NORMALIZED TYPICAL PERFORMANCE CHARACTERISTICS

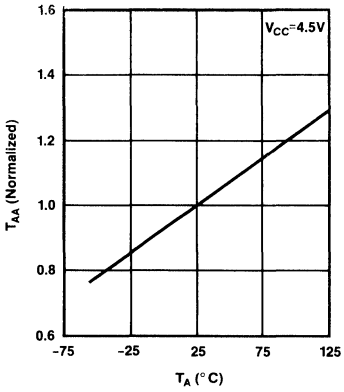
Supply Current vs. Voltage



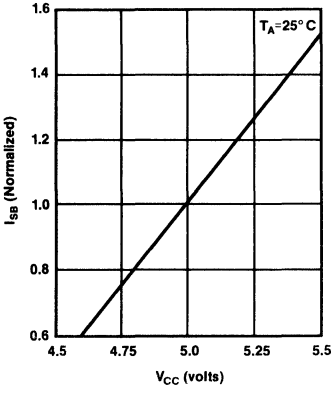

Supply Current vs. Ambient Temperature



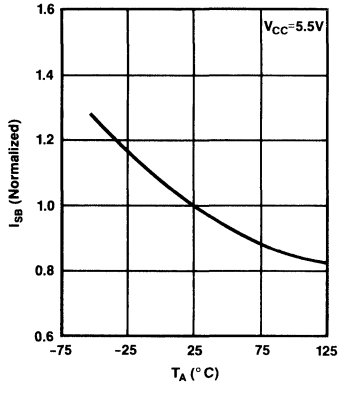

Address Access Time vs. Ambient Temperature



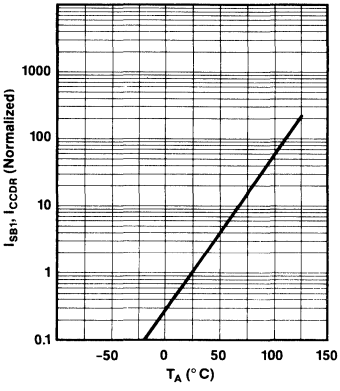

Stand-by Power Supply Current vs. Voltage



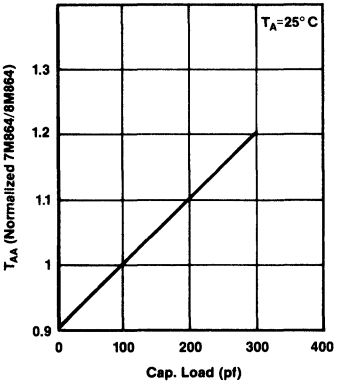

Stand-by Power Supply Current vs. Ambient Temperature




Full Stand-by Power Supply Current. Data Retention Current vs. Ambient Temperature




Address Access Time vs. Capacitive Load

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