1 MEGABIT CMOS STATIC RAM PLASTIC MODULE

ADVANCE INFORMATION IDT7MP624S

FEATURES:
- High-density 1024K-bit CMOS static RAM module
- Customer-configured to 64K x 16, 128K x 8 or 256K x 4
- Fast access times
  —30ns (max.) over commercial temperature range
- Low-power consumption
  —Active: 4.8W (typ. in 64K x 16 organization)
  —Standby: 1.6mW (typ.)
- Utilizes 16 IDT7187 high-performance 64K x 1 CMOS static RAMs produced with IDT's advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Offered in 40-pin, 900 mil center plastic DIP, achieving very high memory density
- Cost-effective plastic surface mounted RAM packages on an epoxy laminate (FR4) substrate

DESCRIPTION:
The IDT7MP624 is a 1024K-bit high-speed CMOS static RAM constructed on an epoxy laminate substrate using 16 IDT7187 (64K x 1) static RAMs in plastic surface mount packages. Making four chip select lines available (one for each group of 4 RAMs) allows the user to configure the memory into a 64K x 16, 128K x 8 or 256K x 4 organization. In addition, extremely high speeds are achievable by the use of IDT7187s fabricated in IDT's high-performance, high-reliability technology, CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 64K static RAMs available.

The IDT7MP624 is available with access times as fast as 30ns commercial temperature range, with maximum operating power consumption of only 10.5W (significantly less if organized 128K x 8 or 256K x 4). The module also offers a standby power mode of 4.4W (max.) and a full standby mode of 1.7W (max.).

The IDT7MP624 is offered in a high-density 40-pin, 900 mil center plastic DIP to take full advantage of the compact IDT7187s in plastic surface mount packages.

All inputs and outputs of the IDT7MP624 are TTL-compatible and operate from a single 5V supply. (NOTE: Both GND pins need to be grounded for proper operation.) Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access times for ease of use.
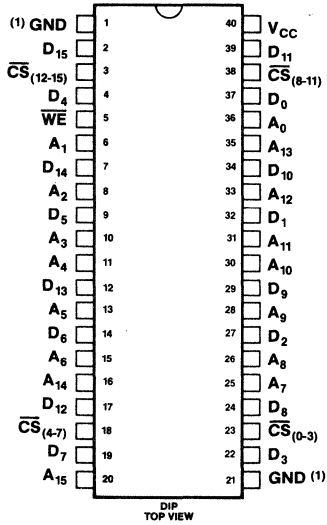
FUNCTIONAL BLOCK DIAGRAM
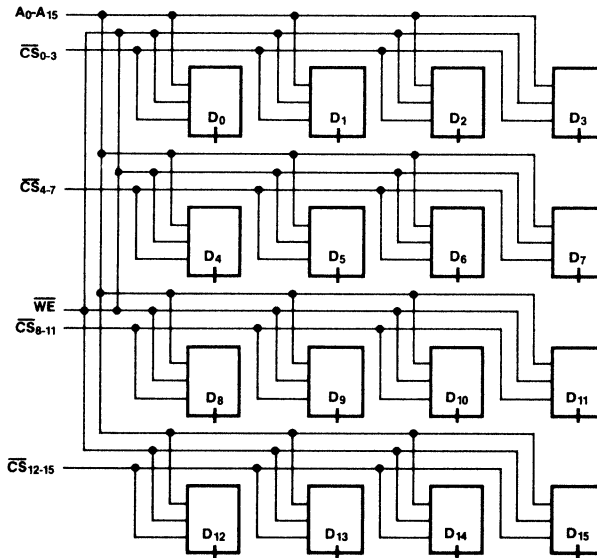
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COMMERCIAL TEMPERATURE RANGE   **JULY 1986**

PIN CONFIGURATION

(1) GND	1	40	V_{CC}
D_{15}	2	39	D_{11}
$\overline{CS}_{(12-15)}$	3	38	$\overline{CS}_{(8-11)}$
D_4	4	37	D_0
$\overline{WE}$	5	36	A_0
A_1	6	35	A_{13}
D_{14}	7	34	D_{10}
A_2	8	33	A_{12}
D_5	9	32	D_1
A_3	10	31	A_{11}
A_4	11	30	A_{10}
D_{13}	12	29	D_9
A_5	13	28	A_9
D_6	14	27	D_2
A_6	15	26	A_8
A_{14}	16	25	A_7
D_{12}	17	24	D_8
$\overline{CS}_{(4-7)}$	18	23	$\overline{CS}_{(0-3)}$
D_7	19	22	D_3
A_{15}	20	21	GND (1)

DIP
TOP VIEW

PIN NAMES

A_0 - A_{15}	ADDRESSES
D_0 - D_{15}	DATA INPUT/OUTPUT
$\overline{CS}_{XX}$	CHIP SELECTS
$\overline{WE}$	WRITE ENABLE
V_{CC}	POWER
GND	GROUND

NOTE:
1. Both GND pins need to be grounded for proper operation.