Integrated Device Technology, Inc.

CMOS STATIC RAM MODULE 256K (16K x 16-BIT) & 128K (8K x 16-BIT)

PRELIMINARY
IDT8M656S
IDT8M628S

FEATURES:

- High-density 256K/128K-bit CMOS static RAM modules
- 16K x 16 organization (IDT8M656) with 8K x 16 option (IDT8M628)
- Upper byte (I/O_{9-16}) and lower byte (I/O_{1-8}) separated control
  — Flexibility in application
- Equivalent to JEDEC standard for future monolithic 16K x 16/8K x 16 static RAMs
- High-speed
  — Military — 60ns (max.)
  — Commercial — 50ns (max.)
- Low-power consumption: typically less than 1W operating (IDT8M656), less than 1mW in standby
- Utilizes IDT7164s — high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Offered in the JEDEC standard 40-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT8M656/IDT8M628 are 265K/128K-bit high-speed CMOS static RAMs constructed on a multi-layered ceramic substrate using four IDT7164 8K x 8 static RAMs (IDT8M656) or two IDT7164 static RAMs (IDT8M628) in leadless chip carriers.

Functional equivalence to proposed monolithic static RAMs is achieved by utilization of an on-board decoder that interprets the higher order address A_{13} to select one of the two 8K x 16 RAMs as the by-16 output and using $\overline{LB}$ and $\overline{UB}$ as two extra chip select functions for lower byte (I/O_{1-8}) and upper byte (I/O_{9-16}) control, respectively. (On IDT8M628 8K x 16 option, A_{13} needs to be externally grounded for proper operation.) Extremely high speeds are achievable by the use of IDT7164s fabricated in IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest 256K/128K static RAMs available.

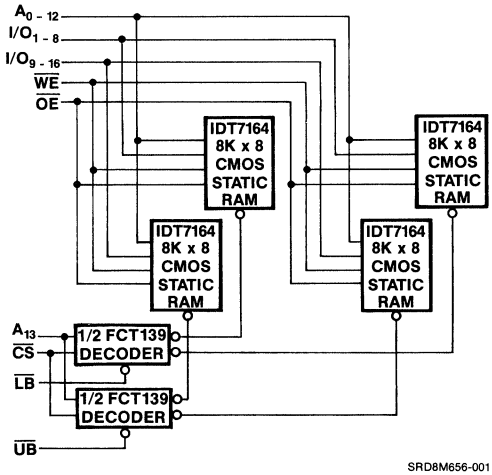
The IDT8M656/IDT8M628 are available with access times as fast as 50ns commercial and 60ns military temperature range, with maximum operating power consumption of only 1.8W (IDT8M656, 16K x 16 option). The module also offers a full standby mode of 440mW (max.).

The IDT8M656/IDT8M628 are offered in a high-density 40-pin, 600 mil center sidebraze DIP to take full advantage of the compact IDT7164s in leadless chip carriers.

All inputs and outputs of the IDT8M656/IDT8M628 are TTL-compatible and operate from a single 5V supply. (NOTE: Both V_{CC} pins need to be connected to the 5V supply and both GND pins need to be grounded for proper operation.) Fully asynchronous ciruitry is used requiring no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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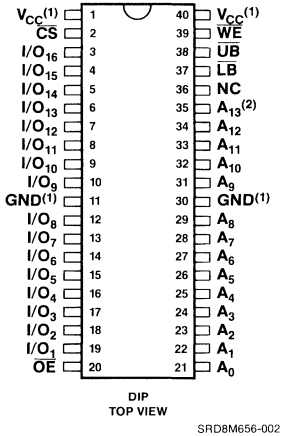
PIN CONFIGURATION



DIP
TOP VIEW

SRD8M656-002

PIN NAMES

A_{0-13}	Addresses
I/O_{1-16}	Data Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Power
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
$\overline{UB}$	Upper Byte Control
$\overline{LB}$	Lower Byte Control

NOTES:

1. Both V_{CC} pins need to be connected to the 5V supply, and both GND pins need to be grounded for proper operation.
2. On IDT8M628, 128K (8K x 16-Bit) option, A_{13} (Pin 35) is required external grounding for proper operation.

ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +155	°C
P_T	Power Dissipation	4.0	W
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:

1. V_{IL} (min) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%, V_{CC} (Min.) = 4.5V, V_{CC} (Max.) = 5.5V, V_{LC} = 0.2V, V_{HC} = V_{CC} = -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS	IDT8M656S			IDT8M628S			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	—	15	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	—	15	—	—	15	µA
I_{CCX16}	Operating Current in X16 Mode	$\overline{CS}$, $\overline{UB}$ & $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f Max.	—	165	330	—	150	300	mA
I_{CCX8}	Operating Current in X8 Mode	$\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL} V_{CC} = Max., Output Open f = f Max.	—	100	200	—	80	170	mA
I_{SB} & I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} or $\overline{UB}$ ≥ V_{IH} and $\overline{LB}$ ≥ V_{IH} V_{CC} = Max. Output Open	—	4	80(2)	—	2	40(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.	2.4	—	—	2.4	—	—	V

NOTE:

1. V_{CC} = 5V, T_A = +25°C
2. I_{SB} and I_{SB1} of IDT8M656/IDT8M628 at commercial temperature = 60mA/30mA.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figs. 1 & 2

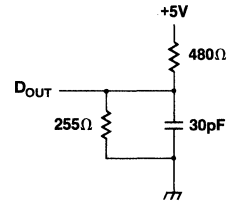


Figure 1. Output Load

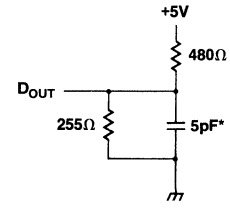


Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Including scope and jig

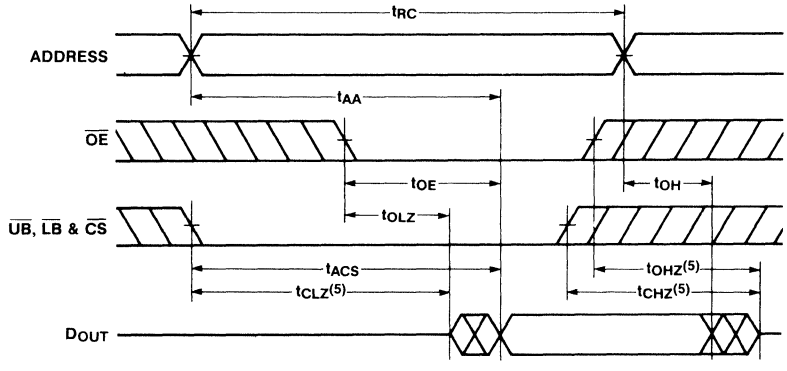
SRD8M656-003

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT8M656S50 IDT8M729S50 COM'L. ONLY		IDT8M656S60 IDT8M628S60		IDT8M656S70 IDT8M628S70		IDT8M656S85 IDT8M628S85		IDT8M656S100 IDT8M628S100 MIL. ONLY		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	50	—	60	—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time	—	50	—	60	—	70	—	85	—	100	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	50	—	60	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}(1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power Down Time	—	50	—	60	—	70	—	85	—	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	50	—	60	—	70	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AW}	Address Valid to End of Write	45	—	55	—	65	—	75	—	90	—	ns
t_{AS}	Address Setup Time	5	—	10	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	55	—	65	—	80	—	ns
t_{WR}	Write Recovery Time	5	—	5	—	5	—	10	—	10	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	25	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



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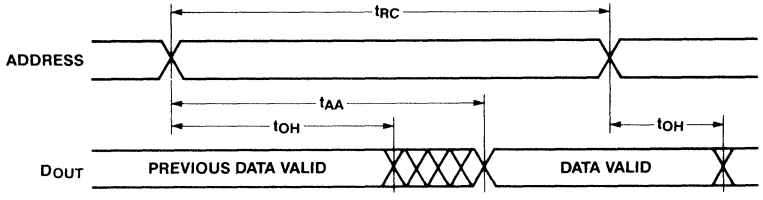
TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



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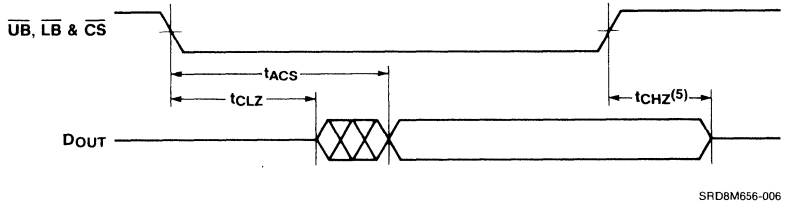
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



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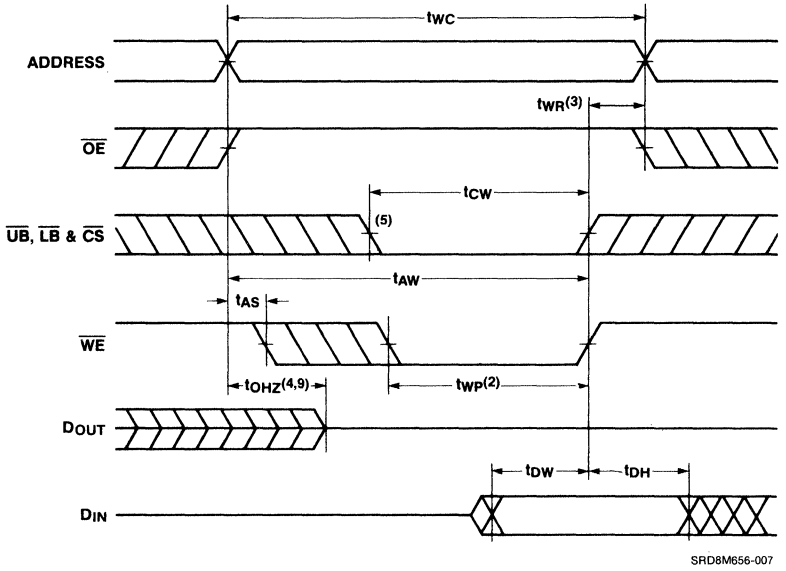
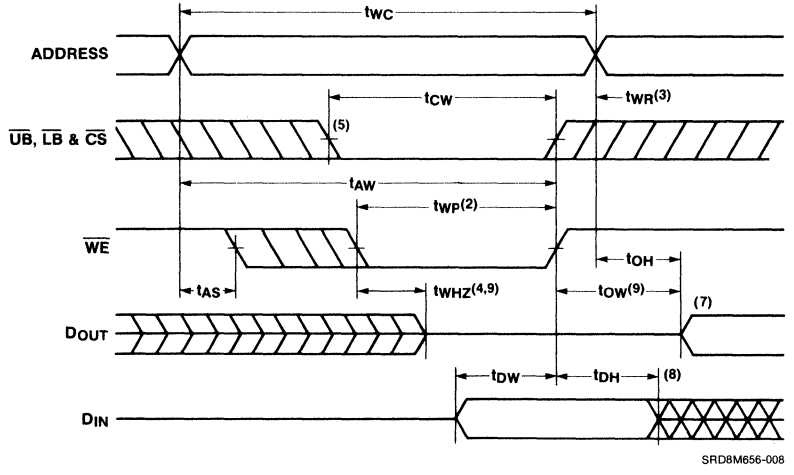
NOTES:

1. WE is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{UB}$, $\overline{LB}$ = V_{IL} for 16 output active.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2(1,6)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ or $\overline{UB}$ and $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	X	X	High Z	Standby
Standby	L	H	H	X	X	High Z	Standby
Read	L	L	L	L	H	$D_{OUT\ 1-16}$	Active
Lower Byte Read	L	H	L	L	H	$D_{OUT\ 1-8}$	Active (X8)
Upper Byte Read	L	L	H	L	H	$D_{OUT\ 9-16}$	Active (X8)
Read	L	L	L	H	H	High Z	Active
Lower Byte Read	L	H	L	H	H	High Z	Active (X8)
Upper Byte Read	L	L	H	H	H	High Z	Active (X8)
Write	L	L	L	X	L	$D_{IN\ 1-16}$	Active
Lower Byte Write	L	H	L	X	L	$D_{IN\ 1-8}$	Active (X8)
Upper Byte Write	L	L	H	X	L	$D_{IN\ 9-16}$	Active (X8)

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	TBD	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	TBD	pF

NOTE:
1. This parameter is sampled and not 100% tested.