

FEATURES:

- Compliant with Intel CK505 Gen II spec
- One high precision PLL for CPU, SSC and N programming
- One high precision PLL for SRC, SSC and N programming
- One high precision PLL for SATA/PCI, and SSC
- One high precision PLL for 96MHz/48MHz
- Push-pull IOs for differential outputs
- Support spread spectrum modulation, -0.5 down spread and others
- Support SMBus block read/write, byte read/write
- Available in TSSOP package

OUTPUTS:

- 2 - 0.7V differential CPU CLK pair
- 10 - 0.7V differential SRC CLK pair
- 1 - CPU_ITP/SRC differential clock pair
- 1 - SRC0/DOT96 differential clock pair
- 6 - PCI, 33.3MHz
- 1 - 48MHz
- 1 - REF
- 1 - SATA

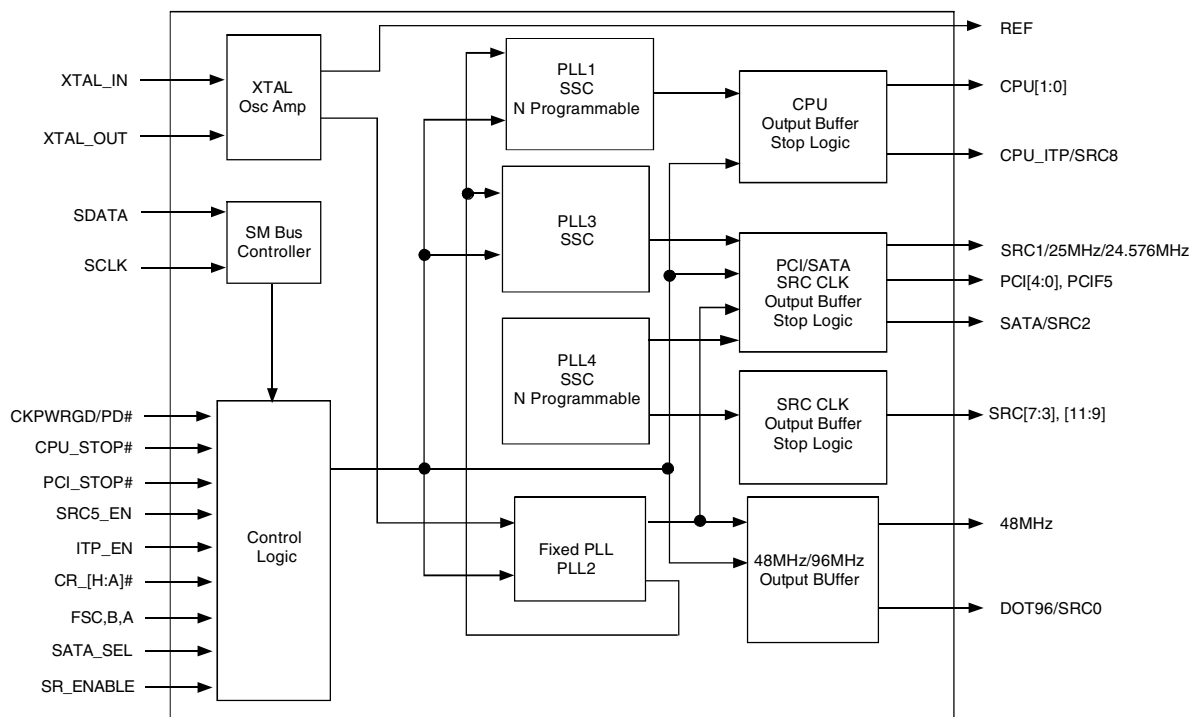
KEY FEATURES

- Direct CPU and SRC clock frequency programming—write the Hex number into Byte [16:18], 1MHz stepping.
- Linear and smooth transition for the CPU and SRC frequency programming.
- SATA PLL source hardware select latch pin, PLL2 or PLL4.
- Internal serial resistor hardware enable latch pin.
- WOL 25MHz support.

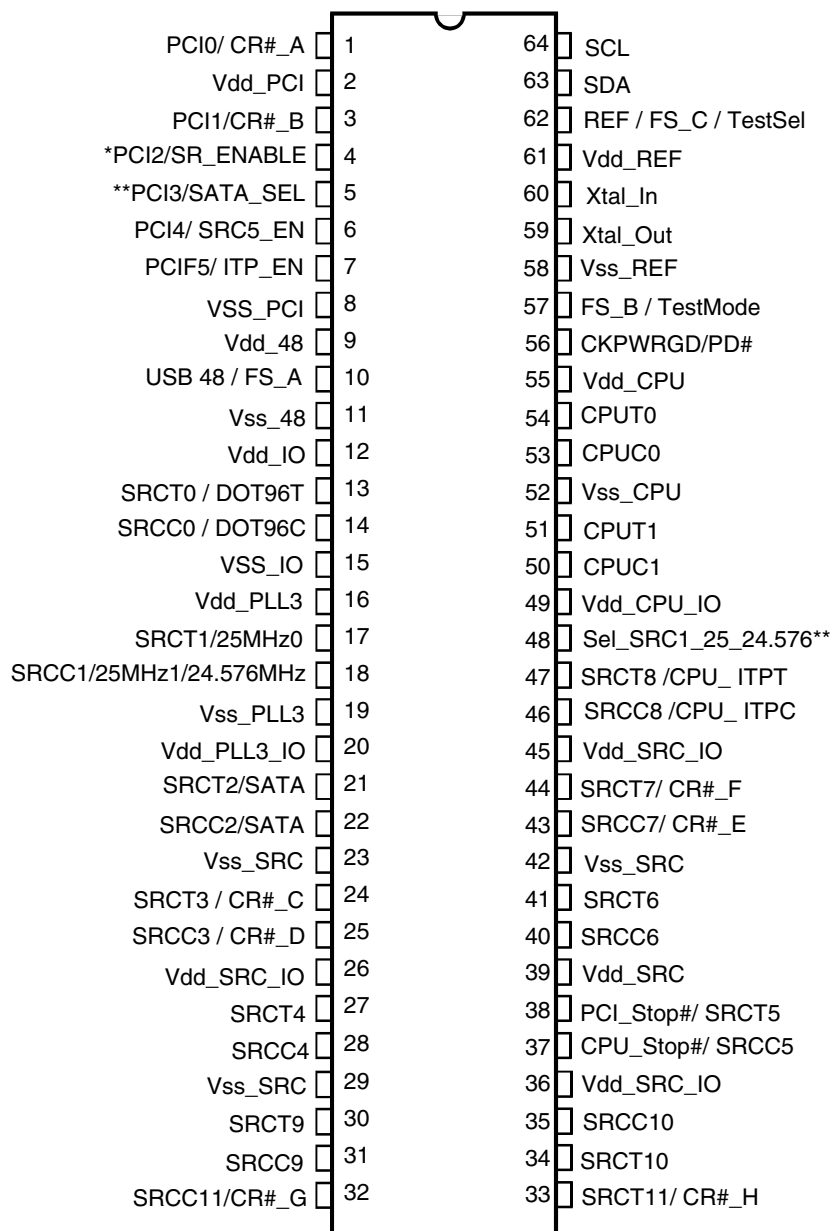
KEY SPECIFICATIONS:

- CPU/SRC CLK cycle to cycle jitter < 85ps
- PCI CLK cycle to cycle jitter < 500ps
- All SRC, SRC[0:11] phase noise < 3.10s RMS, PCIE Gen II phase noise requirement.
- SRC3, 4, 6, 7, designated PCIE Gen II outputs, nominal interpair skew = 0 ps

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



* Internal 100k pull high

** Internal 100k pull low

TSSOP
TOP VIEW

PIN DESCRIPTION

Pin #	Name	Type	Description
1	PCI0/CR#_A	I/O	33.33MHz. SRC0, 2 Differential clock output enable, control SRC0 and SRC2, 0 = enable. Mode is selected by SMBus control register. Default is PCI clock mode.
2	VDD_PCI	PWR	3.3V
3	PCI1/CR#_B	I/O	33.33MHz. SRC1, 4 Differential clock output enable, control SRC1 and SRC4, 0 = enable. Mode is selected by SMBus control register. Default is PCI clock mode.
4	PCI2/SRC_ENABLE	I/O	Power on latch, high, internal 33 ohm resistor enabled. Low, disabled. Afterward 33.33MH
5	PCI3/SATA_SEL	OUT	Power on Latch, high, SATA from PLL2. Low, SATA from PLL4 (as SRC clock). Afterward, 33.33MHz
6	PCI4/SRC5_EN	I/O	33.33MHz. Pin 37, 38 mode selection. Power on latch, HIGH = SRC5, LOW = CPU and PCI Stop#.
7	PCIF5/ITP_EN	I/O	33.33MHz. Pin 46, 47 mode selection. Power on latch, HIGH = CPU_ITP, LOW = SRC8.
8	Vss_PCI	GND	GND
9	VDD_48	PWR	3.3V
10	USB_48/FS_A	I/O	48MHz, frequency select, power on latch
11	Vss_48	GND	GND
12	VDD_IO	PWR	1.05 ~ 3.3V
13	SRCT0/DOT96T	OUT	Differential output clock. SRC or DOT96. Mode selected by SMBus control register, default is SRC0.
14	SRCC0/DOT96C	OUT	Differential output clock. SRC or DOT96. Mode selected by SMBus control register, default is SRC0.
15	Vss_IO	GND	GND
16	VDD_PLL3	PWR	3.3V
17	SRCT1/25MHz	OUT	SRC or 25MHz, mode selected by pin 48, Sel_SRC1_25_24.576
18	SRCC1/25MHz1/24.576MHz	OUT	SRC or 25MHz or 24.576MHz, mode selected by pin 48, Sel_SRC1_25_24.576
19	Vss_PLL3	GND	GND
20	VDD_PLL3_IO	PWR	1.05 ~ 3.3V
21	SATAT/SRCT2	OUT	Differential output clock
22	SATAC/SRCC2	OUT	Differential output clock
23	Vss_SRC	GND	GND
24	SRCT3/CR#_C	I/O	SRC clock. SRC differential clock output enable, control SRC0 and SRC2, 0 = enable. Mode selected by SMBus control register. Default is SRC3.
25	SRCC3/CR#_D	I/O	SRC clock. SRC differential clock output enable, control SRC1 and SRC4, 0 = enable. Mode selected by SMBus control register. Default is SRC3.
26	VDD_SRC_IO	PWR	1.05 ~ 3.3V
27	SRCT4	OUT	Differential output clock
28	SRCC4	OUT	Differential output clock
29	Vss_SRC	GND	GND
30	SRCT9	OUT	Differential output clock
31	SRCC9	OUT	Differential output clock
32	SRCC11/CR#_G	I/O	SRC clock. SRC differential clock output enable, control SRC9, 0 = enable. Mode selected by SMBus control register. Default is SRC11.
33	SRCT11/CR#_H	I/O	SRC clock. SRC differential clock output enable, control SRC10, 0 = enable. Mode selected by SMBus control register. Default is SRC11.
34	SRCT10	OUT	Differential output clock
35	SRCC10	OUT	Differential output clock
36	VDD_SRC_IO	PWR	1.05 ~ 3.3V
37	CPU_Stop#/SRCC5	I/O	CPU stop, LOW = stop. SRC clock. Mode selected by pin6, SRC5_EN.
38	PCI_Stop#/SRCT5	I/O	PCI stop, LOW = stop. SRC clock. Mode selected by pin6, SRC5_EN.
39	VDD_SRC	PWR	3.3V
40	SRCC6	OUT	Differential output clock
41	SRCT6	OUT	Differential output clock
42	Vss_SRC	GND	GND

PIN DESCRIPTION, CONTINUED

Pin #	Name	Type	Description
43	SRCC7/CR#_E	I/O	SRC clock. SRC differential clock output enable, control SRC6, 0 = enable. Mode selected by SMBus control register. Default is SRC7.
44	SRCT7/CR#_F	I/O	SRC clock. SRC differential clock output enable, control SRC8, 0 = enable. Mode selected by SMBus control register. Default is SRC7.
45	VDD_SRC_IO	PWR	1.05 ~ 3.3V
46	SRCC8/CPU_ ITPC	OUT	SRC clock. CPU clock. Mode selected by pin7.
47	SRCT8/CPU_ IPTPT	OUT	SRC clock. CPU clock. Mode selected by pin7.
48	Sel_SRC1_25_24.576	OUT	Power on latch, Select pin 17, 18 Mode, see pin 48 Function Table.
49	VDD_CPU_IO	PWR	1.05 ~ 3.3V
50	CPUC1	OUT	Differential output clock
51	CPUT1	OUT	Differential output clock
52	VSS_CPU	GND	GND
53	CPUC0	OUT	Differential output clock
54	CPUT0	OUT	Differential output clock
55	VDD_CPU	PWR	3.3V
56	CKPWRGD/PD#	IN	CKPWRGD power good, active LOW, used to latch FSA,B,C, ITP_EN, TME, and SRC5_EN, active HIGH. After, becomes power down, LOW active.
57	FS_B/TestMode	IN	Frequency Select at CKPWRGD assertion. Test Mode selection, see TEST_MODE selection table.q
58	VSS_REF	GND	GND
59	XTAL_OUT	OUT	XTAL out
60	XTAL_IN	IN	XTAL in
61	VDD_REF	PWR	3.3V
62	REF/FS_C/TestSel	I/O	14.318MHz. Frequency Select at CKPWRGD assertion. Selects test mode if pulled above 2V at CKPWRGD assertion.
63	SDA	I/O	SMBus data
64	SCL	IN	SMBus clock

TEST MODE SELECTION⁽¹⁾

If TEST_SEL sampled above 2V at CKPWRGD active LOW

Test_Mode	CPU	SRC	PCI/F	REF	DOT_96/DOT_SSC	USB
1	REF/N	REF/N	REF/N	REF	REF/N	REF/N
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

NOTE:

1. Once test clock operation has been invoked, TEST_MODE pin will select between the Hi-Z and REF/N, with V_{IH_FS} and V_{IL_FS} thresholds.

FREQUENCY SELECTION

FSC, B, A	CPU	SRC[7:0]	PCI	USB	DOT	REF
101	100	100	33.3	48	96	14.318
001	133	100	33.3	48	96	14.318
011	166	100	33.3	48	96	14.318
010	200	100	33.3	48	96	14.318
000	266	100	33.3	48	96	14.318
100	333	100	33.3	48	96	14.318
110	400	100	33.3	48	96	14.318
111	Reserve	100	33.3	48	96	14.318

SEL_SRC1_25_24.576 (PIN 48) VOLTAGE DECODING TABLE

state	Min	Typ	Max
Low	0V	0.55V	0.9V
Mid	1.3V	1.65V	2V
High	2.4V	2.75V	VDD

SR_ENABLE TABLE

SR_ENABLE	
0	Need external 33 ohm serial resistor, Byte19 bit7 = 0
1 (default)	Enable 33 ohm internal serial resistor, Byte19 bit7 = 1

SEL_SRC1_25_24.576 FUNCTION TABLE

Sel_SRC1_25_24.576 (pin48)	CPU	PCI	Pin 17	Pin 18	SRC	48/96
Low	PLL1	PLL4	25MHz, PLL3 (SS off)	25MHz PLL3 (SS off)	PLL4 down	PLL2, fixed
Mid	PLL1	PLL4	SRCT1	SRCC1	PLL4 down	PLL2, fixed
High	PLL1	PLL4	25MHz PLL2	24.576MHz PLL3 (SS off)	PLL4 down	PLL2, fixed

SATA_SEL TABLE

SATA_SEL	SRC2/SATA
0	PLL4 (SRC PLL, SSC)
1	PLL2 (48/96 PLL)

DEVICE ID TABLE

ID3,ID2,ID1,ID0		Comments
0000	CK505 56 pin TSSOP	CK505 YC
0001	CK505 64 pin TSSOP	CK505 YC
0010	48 pin QFN	CK505 YC
0011	56 pin QFN	CK505 YC
0100	64 pin QFN	CK505 YC
0101	72 pin QFN	CK505 YC
0110	48 pin SSOP	CK505 YC
0111	56 pin SSOP	CK505 YC
1000	Reserved	CK505 Derivative (non YC)
1001	Reserved	
1010	Reserved	
1011	Reserved	
1100	Reserved	
1101	Reserved	
1110	Reserved	
1111	Reserved	

IO_VOUT [2:0] TABLE

000	0.3V
001	0.4V
010	0.5V
011	0.6V
100	0.7V
101	0.8V
110	0.9V
111	1V

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDD	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	-65	+150	°C
TAMBIENT	Ambient Operating Temperature	0	+70	°C
TCASE	Case Temperature		+115	°C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

SM PROTOCOL

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit 30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	D3h
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes)
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

N-PROGRAMMING PROCEDURE

- Byte 16 bit 3 has to be "1". This bit will decode the power on latched value of pins 4, 5 (see CFG table 1).
- User writes the desired CPU frequency in HEX form into CPUN [8:0], Byte 16, 17.
- User writes the desired SRC frequency in HEX form into PN [7:0], Byte 18.

CONTROL REGISTERS

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	FSC	Latched FSC			R	Latched Value
6	FSB	Latched FSB			R	Latched Value
5	FSA	Latched FSA			R	Latched Value
4	iAMT_EN	iAMT Mode	Legacy Mode	Enabled	RW	HW M1 setting(1)
3	Reserved				RW	0
2	Reserved				RW	0
1	SRC2/SATA source		PLL4	PLL2	RW	SATA_SEL latch
0	PD_Restore	SMBUS control registers setting after the power down	Power on default, With some exceptions	Save register contents	RW	1

NOTES:

1. Sticky 1, can only be reset by power off.

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRC0_sel	Pin13/14 mode select	SRC0	DOT96	RW	0
6	PLL1_SSC_DC	SSC mode selection	Down spread	Center spread	RW	1
5	PLL4_SSC_DC	SSC mode selection	Down spread	Center spread	RW	0
4	Reserved				RW	0
3	Reserved				RW	0
2	25MHz_0	PD# free run control	Disabled	Free run	RW	1
1	25MHz_1	PD# free run control	Disabled	Free run	RW	1
0	PCI		PLL2	PLL4	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	REF	Output Enable	Tristate	Enable	RW	1
6	USB_48	Output Enable	Tristate	Enable	RW	1
5	PCIF5	Output Enable	Tristate	Enable	RW	1
4	PCI4	Output Enable	Tristate	Enable	RW	1
3	PCI3	Output Enable	Tristate	Enable	RW	1
2	PCI2	Output Enable	Tristate	Enable	RW	1
1	PCI1	Output Enable	Tristate	Enable	RW	1
0	PCI0	Output Enable	Tristate	Enable	RW	1

BYTE 3

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRC11	Output Enable	Tristate	Enabled	RW	1
6	SRC10	Output Enable	Tristate	Enabled	RW	1
5	SRC9	Output Enable	Tristate	Enabled	RW	1
4	SRC8/ITP	Output Enable	Tristate	Enabled	RW	1
3	SRC7	Output Enable	Tristate	Enabled	RW	1
2	SRC6	Output Enable	Tristate	Enabled	RW	1
1	SRC5	Output Enable	Tristate	Enabled	RW	1
0	SRC4	Output Enable	Tristate	Enabled	RW	1

BYTE 4

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRC3	Output Enable	Disabled	Enabled	RW	1
6	SATA/SRC2	Output Enable	Disabled	Enabled	RW	1
5	SRC1	Output Enable	Disabled	Enabled	RW	1
4	SRC0/DOT96	Output Enable	Disabled	Enabled	RW	1
3	CPU1	Output Enable	Disabled	Enabled	RW	1
2	CPU0	Output Enable	Disabled	Enabled	RW	1
1	PLL1_SSC_ON	SSC Enable	Disabled	Enabled	RW	1
0	PLL4_SSC_ON	SSC Enable	Disabled	Enabled	RW	1

BYTE 5

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CR#_A	Pin1 mode selection	PCI0 mode	CR#_A mode	RW	0
6	CR#_A control	CR#_A control selection	SRC0	SRC2	RW	0
5	CR#_B	Pin3 mode selection	PCI1 mode	CR#_B mode	RW	0
4	CR#_B control	CR#_B control selection	SRC1 ⁽¹⁾	SRC4	RW	0
3	CR#_C	Pin24 mode selection	SRCT3 mode	CR#_C mode	RW	0
2	CR#_C control	CR#_C control selection	SRC0	SRC2	RW	0
1	CR#_D	Pin25 mode selection	SRCC3 mode	CR#_D mode	RW	0
0	CR#_D control	CR#_D control selection	SRC1	SRC4	RW	0

NOTE:

1. Only when SRC1 is SRC Clock.

BYTE 6⁽¹⁾

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	CR#_E	Pin43 mode selection, control SRC6	SRCC7 mode	CR#_E mode, Control SRC 6	RW	0
6	CR#_F	Pin44 mode selection, control SRC8	SRCT7 mode	CR#_F mode, Control SRC 8	RW	0
5	CR#_G	Pin32 mode selection, control SRC9	SRCC11 mode	CR#_G mode, Control SRC 9	RW	0
4	CR#_H	Pin33 mode selection, control SRC10	SRCT11 mode	CR#_H mode, Control SRC 10	RW	0
3	Reserved				RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	SRC_STP_CRTL	If set, SRCs stop with PCI_STOP#	Free running	Stoppable	RW	0

NOTE:

1. STOP - CPUT and SRCT stay high, CPUC and SRCC stay low.

BYTE 7

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7		Revision ID				0
6		Revision ID				0
5		Revision ID				0
4		Revision ID				0
3		Vendor ID				0
2		Vendor ID				1
1		Vendor ID				0
0		Vendor ID				1

BYTE 8

Bit	Output(s) affected	Description/Function	0	1	Type	Power On
7	Device_ID3	See device ID table			R	
6	Device_ID2				R	
5	Device_ID1				R	
4	Device_ID0				R	
3					RW	0
2					RW	0
1	Pin 17_SE_OE	Output enable (Cannot be reset by PD Restore)	Disabled	Enabled	RW	1
0	Pin 18_SE_OE	Output enable (Can not be reset by PD Restore)	Disabled	Enabled	RW	1

BYTE 9

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PCIF5 with PCI_STOP#	Free running	Free running	stoppable	RW	0
6	Reserved					
5	REF Drive Strength	Strength control	1x	2x	RW	1
4		Only valid when Byte9 bit3 is 1	Hi-Z	REF/N mode	RW	0
3		Test Mode entry control	Normal operation	Test mode, controlled by byte9 bit 4	RW	0
2	IO_VOUT2				RW	1
1	IO_VOUT1	Programmable IO_Vout voltage			RW	0
0	IO_VOUT0				RW	1

BYTE 10

Bit	Output(s) affected	Description/ Function	0	1	Type	Power On
7		SRC5_EN_Strap			R	The latch of SRC5_EN
6	PLL3	PLL3 enable	PLL3 pwr dwn	Pwr up	RW	1
5	PLL2	PLL2 enable	PLL2 pwr dwn	Pwr up	RW	1
4	SRC_DIV	SRC divider disable	disable	enable	RW	1
3	PCI_DIV	PCI divider disable	disable	enable	RW	1
2	CPU_DIV	CPU divider disable	disable	enable	RW	1
1	CPU1 Free run	Controlled by CPU_STP#	Free run	Controllable	RW	1
0	CPU0 Free run	Controlled by CPU_STP#	Free run	Controllable	RW	1

BYTE 11 - RESERVED

Bit	Output(s) affected	Description/ Function	0	1	Type	Power On
7	Reserved				R	
6	Reserved				R	
5	Reserved				RW	0
4	Reserved				RW	1
3	CPU_ITP_AMT_EN	M1 mode CLK enable at M1 mode Only if ITP_EN = 1	disable	enable	RW	0
2	CPU1_AMT_EN	M1 mode CLK enable at M1 mode	disable	enable	RW	1
1	PCI GEN II	GEN II compliance	None GEN II	GEN II	R	1
0	CPU_ITP_STOP_EN	Free run control	Free run	Controlled	RW	1

BYTE 12 - BYTE COUNT - DEFAULT 0x13H

BYTE 13

Bit	Output(s) Affected	Description/ Function	0	1	Type	Power On
7	48M	Strength control	1x	2x	RW	1
6	REF	Strength control	1x	2x	RW	0
5	PCIF5	Strength control	1x	2x	RW	1
4	PCI4	Strength control	1x	2x	RW	1
3	PCI3	Strength control	1x	2x	RW	1
2	PCI2	Strength control	1x	2x	RW	1
1	PCI1	Strength control	1x	2x	RW	1
0	PCI0	Strength control	1x	2x	RW	1

BYTE 14 RESERVED

BYTE 15, WATCH DOG⁽¹⁾

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Watch Dog Enable	Watch Dog Alarm Enable	Disabled	Enabled	RW	0
6	Watch Dog Select	Watch Dog Hard/Soft Alarm Select	Hard Alarm Only	Hard and Soft Alarm	RW	0
5	Watch Dog Hard Alarm Status	Watch Dog Hard Alarm Status	Normal	Alarm	R	
4	Watch Dog Soft Alarm Status	Watch Dog Soft Alarm Status	Normal	Alarm	R	
3	Watch Dog control	Watch Dog Time Base Control	290ms base	1160ms base	RW	0
2	WD_1_Timer 2	WatchDog_1_Alarm Timer Default is 7*290ms			RW	1
1	WD_1_Timer 1				RW	1
0	WD_1_Timer 0				RW	1

NOTE:

1. Hard Alarm switch to HW FS frequency.

BYTE 16

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	WDEAPD	Set Byte15 bit7 = 1 after Power Down to enable the watch dog after the power down	Disabled	Enabled	RW	0
6	Reserved				RW	0
5	Reserved				RW	0
4	Test_scl	On chip test mode enable	normal	SCLK=1, clk outputs = 1 SCLK=0, clk outputs=0	RW	0
3	N programming Enable		Disabled	Enabled	RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	CPUN8				RW	FS latch

BYTE 17 (PLL1)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	CPUN7	CPU clock frequency = CPUN [8:0] (Hex)			RW	FS latch
6	CPUN6				RW	
5	CPUN5				RW	
4	CPUN4				RW	
3	CPUN3				RW	
2	CPUN2				RW	
1	CPUN1				RW	
0	CPUN0				RW	

BYTE 18 (PLL4)

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	PN 7	SRC clock frequency = PNC [7:0] (Hex)			RW	100MHz
6	PN 6				RW	
5	PN 5				RW	
4	PN 4				RW	
3	PN 3				RW	
2	PN 2				RW	
1	PN 1				RW	
0	PN 0				RW	

BYTE 19 CLOCK SOURCE SELECTION, WRITTEN AFTER STOP BIT

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Output serial resistor		0 ohm (External resistor needed)	33 ohm (No external resistor needed)	RW	SR_ENABLE latch
6	PLL1 SSC	spread % selection	0.5% (p-p)	0.45%(p-p)	RW	0
5	Reserved				RW	0
4	PLL4 SSC	spread % selection	0.5% (p-p)	0.45%(p-p)	RW	0
3	Reserved				RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	Reserved				RW	0

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage		4.6	V	1,7
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply		3.8	V	1,7
Maximum Input Voltage	V _{IH}	3.3V LVCMOS Inputs		4.6	V	1,7,8
Minimum Input Voltage	V _{IL}	Any Input	GND - 0.5		V	1,7
Storage Temperature	T _s	-	-65	150	°C	1,7
Input ESD protection	ESD prot	Human Body Model	2000		V	1,7

ELECTRICAL CHARACTERISTICS - INPUT/SUPPLY/COMMON OUTPUT PARAMETERS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	T _{ambient}	-	0	70	°C	1
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	1
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	1.05	3.3	V	1
Input High Voltage	V _{IHSE}	Single-ended inputs	2	V _{DD} + 0.3	V	1
Input Low Voltage	V _{ILSE}	Single-ended inputs	V _{SS} - 0.3	0.8	V	1
Input Leakage Current	I _{IN}	V _{IN} = V _{DD} , V _{IN} = GND	-5	5	uA	1
Input Leakage Current	I _{INRES}	Inputs with pull or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND	-200	200	uA	1
Output High Voltage	V _{OHSE}	Single-ended outputs, I _{OH} = -1mA	2.4		V	1
Output Low Voltage	V _{OLSE}	Single-ended outputs, I _{OL} = 1 mA		0.4	V	1
Output High Voltage	V _{OHDF}	Differential Outputs, I _{OH} = TBD mA	0.7	0.9	V	1
Output Low Voltage	V _{OLDIF}	Differential Outputs, I _{OL} = TBD mA		0.4	V	1
Low Threshold Input-High Voltage (Test Mode)	V _{IH_FS_TEST}	3.3 V +/-5%	2	V _{DD} + 0.3	V	1
Low Threshold Input-High Voltage	V _{IH_FS}	3.3 V +/-5%	0.7	1.5	V	1
Low Threshold Input-Low Voltage	V _{IL_FS}	3.3 V +/-5%	V _{SS} - 0.3	0.35	V	1
Operating Supply Current	I _{DDOP3.3}	Full active, C _L =full load, I _{DD} 3.3V		200	mA	1
	I _{DD_IO}	Full active, C _L =full load, I _{DD} 3.3		70	mA	1
Power Down Current	I _{DD_PD3.3}	3.3V supply, Power Down Mode		5	mA	1
	I _{DD_PDIO}	0.8V IO supply, Power Down Mode		0.1	mA	1
iAMT Mode Current	I _{DD_iAMT3.3}	3.3V supply, iAMT Mode		80	mA	1
	I _{DD_iAMT0.8}	0.8V IO supply, iAMT Mode		10	mA	1
Input Frequency	F _i	V _{DD} = 3.3 V		15	MHz	2
Pin Inductance	L _{pin}			7	nH	1
Input Capacitance	C _{IN}	Logic Inputs	1.5	5	pF	1
	C _{OUT}	Output pin capacitance		6	pF	1
	C _{INX}	X1 & X2 pins		TBD	pF	1
Spread Spectrum Modulation Frequency	f _{SSMOD}	Triangular Modulation	30	33	kHz	1

AC ELECTRICAL CHARACTERISTICS - INPUT/COMMON PARAMETERS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock		1.8	ms	1
Tdrive_SRC	T_{DRSRC}	SRC output enable after PCI_STOP# de-assertion		15	ns	1
Tdrive_PD#	T_{DRPD}	Differential output enable after PD# de-assertion		300	us	1
Tdrive_CPU	T_{DRSRC}	CPU output enable after CPU_STOP# de-assertion		10	ns	1
Tfall_PD#	T_{FALL}	Fall/rise time of PD#, PCI_STOP# and CPU_STOP# inputs		5	ns	1
Trise_PD#	T_{RISE}			5	ns	1

AC ELECTRICAL CHARACTERISTICS - LOW POWER DIFFERENTIAL OUTPUTS

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Differential Measurement	2.5	8	V/ns	1,2
Falling Edge Slew Rate	t_{FLR}	Differential Measurement	2.5	8	V/ns	1,2
Slew Rate Variation	t_{SLVAR}	Single-ended Measurement		20	%	1
Maximum Output Voltage	V_{HIGH}	Includes overshoot		1150	mV	1
Minimum Output Voltage	V_{LOW}	Includes undershoot	-300		mV	1
Differential Voltage Swing	V_{SWING}	Differential Measurement	300		mV	1
Crossing Point Voltage	V_{XABS}	Single-ended Measurement	300	550	mV	1,3,4
Crossing Point Variation	$V_{XABSVAR}$	Single-ended Measurement		140	mV	1,3,5
Duty Cycle	D_{CYC}	Differential Measurement	45	55	%	1
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		85	ps	1
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		125	ps	1
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		250	ps	1
CPU[1:0] Skew	CPU_{SKEW10}	Differential Measurement		100	ps	1
CPU[2_ITP:0] Skew	CPU_{SKEW20}	Differential Measurement		150	ps	1
SRC[10:0] Skew	SRC_{SKEW}	Differential Measurement		250	ps	1,10

ELECTRICAL CHARACTERISTICS - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-300	300	ppm	1,6
Clock period	T_{period}	33.33MHz output nominal	29.99100	30.00900	ns	6
		33.33MHz output spread		30.15980	ns	6
Absolute min/max period	T_{abs}	33.33MHz output nominal/spread	29.49100	30.65980	ns	6
Output High Voltage	V_{OH}	$I_{OH} = -1 \text{ mA}$	2.4		V	1
Output Low Voltage	V_{OL}	$I_{OL} = 1 \text{ mA}$		0.4	V	1
Output High Current	I_{OH}	$V_{OH} @ \text{MIN} = 1.0 \text{ V}$	-33		mA	1
		$V_{OH} @ \text{MAX} = 3.135 \text{ V}$		-33	mA	1
Output Low Current	I_{OL}	$V_{OL} @ \text{MIN} = 1.95 \text{ V}$	30		mA	1
		$V_{OL} @ \text{MAX} = 0.4 \text{ V}$		38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	d_{t1}	$V_T = 1.5 \text{ V}$	45	55	%	1
Skew	t_{skew}	$V_T = 1.5 \text{ V}$		250	ps	1
Intentional PCI-PCI delay	t_{delay}	$V_T = 1.5 \text{ V}$	200 nominal		ps	1,9
Jitter, Cycle to cycle	$t_{jcy-cyc}$	$V_T = 1.5 \text{ V}$		500	ps	1

ELECTRICAL CHARACTERISTICS - USB48MHZ

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see T _{period} min-max values	-100	100	ppm	1,2
Clock period	T _{period}	48.00MHz output nominal	20.83125	20.83542	ns	2
Absolute min/max period	T _{abs}	48.00MHz output nominal	20.48130	21.18540	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4		V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA		0.4	V	1
Output High Current	I _{OH}	V _{OH} @ MIN = 1.0 V	-29		mA	1
		V _{OH} @ MAX = 3.135 V		-23	mA	1
Output Low Current	I _{OL}	V _{OL} @ MIN = 1.95 V	29		mA	1
		V _{OL} @ MAX = 0.4 V		27	mA	1
Rising Edge Slew Rate	t _{SLR}	Measured from 0.8 to 2.0 V	1	2	V/ns	1
Falling Edge Slew Rate	t _{FLR}	Measured from 2.0 to 0.8 V	1	2	V/ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45	55	%	1
Jitter, Cycle to cycle	t _{jcy-cyc}	V _T = 1.5 V		350	ps	1

ELECTRICAL CHARACTERISTICS - SMBUS INTERFACE

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
SMBus Voltage	V _{DD}		2.7	5.5	V	1
Low-level Output Voltage	V _{OLSMB}	@ I _{PULLUP}		0.4	V	1
Current sinking at V _{OLSMB} = 0.4 V	I _{PULLUP}	SMB Data Pin	4		mA	1
SCLK/SDATA Clock/Data Rise Time	T _{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T _{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	1
Maximum SMBus Operating Frequency	F _{SMBUS}	Block Mode		100	kHz	1

ELECTRICAL CHARACTERISTICS - REF-14.318MHZ

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see T _{period} min-max values	-300	300	ppm	1,2
Clock period	T _{period}	14.318MHz output nominal	69.8203	69.8622	ns	2
Absolute min/max period	T _{abs}	14.318MHz output nominal	69.8203	70.86224	ns	2
Output High Voltage	V _{OH}	I _{OH} = -1 mA	2.4		V	1
Output Low Voltage	V _{OL}	I _{OL} = 1 mA		0.4	V	1
Output High Current	I _{OH}	V _{OH} @MIN = 1.0 V, V _{OH} @MAX = 3.135 V	-33	-33	mA	1
Output Low Current	I _{OL}	V _{OL} @MIN = 1.95 V, V _{OL} @MAX = 0.4 V	30	38	mA	1
Rising Edge Slew Rate	t _{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t _{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45	55	%	1
Jitter	t _{jyc-cyc}	V _T = 1.5 V		1000	ps	1

Notes on Electrical Characteristics:

¹Guaranteed by design and characterization, not 100% tested in production.

²Slew rate measured through V_{swing} centered around differential zero

³V_{xabs} is defined as the voltage where CLK = CLK#

⁴Only applies to the differential rising edge (CLK rising and CLK# falling)

⁵Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a +/-75mV window centered on the average cross point where CLK meets CLK#.

⁶All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

⁷Operation under these conditions is neither implied, nor guaranteed.

⁸Maximum input voltage is not to exceed maximum VDD

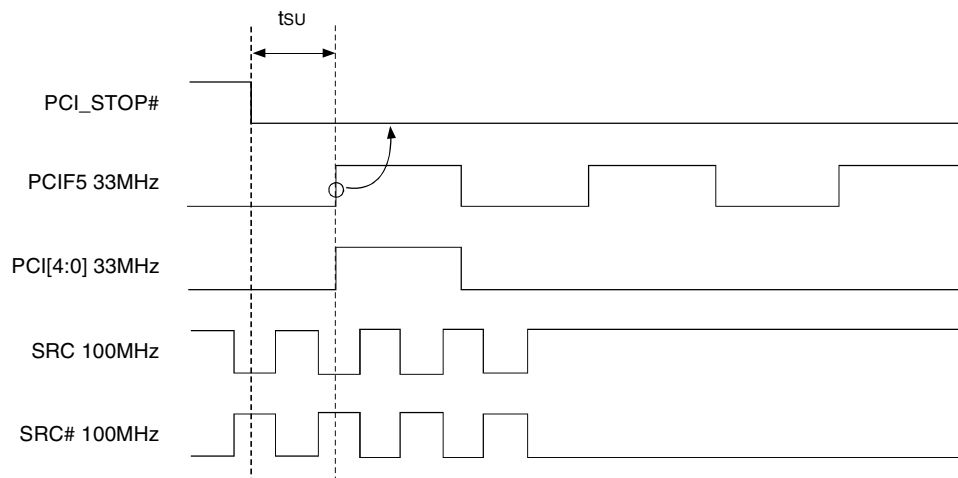
⁹See PCI Clock-to-Clock Delay Figure

¹⁰SRC 3,4,6,7, are 0 ps nominal interpair skew

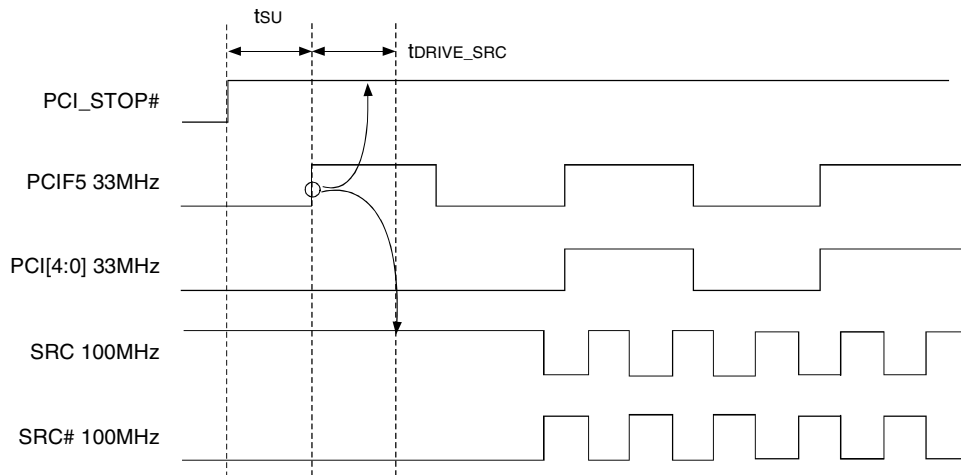
PCI STOP FUNCTIONALITY

PCI_STOP#	SRC	SRC#	PCI
1	Normal	Normal	33MHz
0	High	Low	Low

PCI_STOP# ASSERTION (TRANSITION FROM '1' TO '0')



PCI_STOP# - DE-ASSERTION (TRANSITION FROM '0' TO '1')



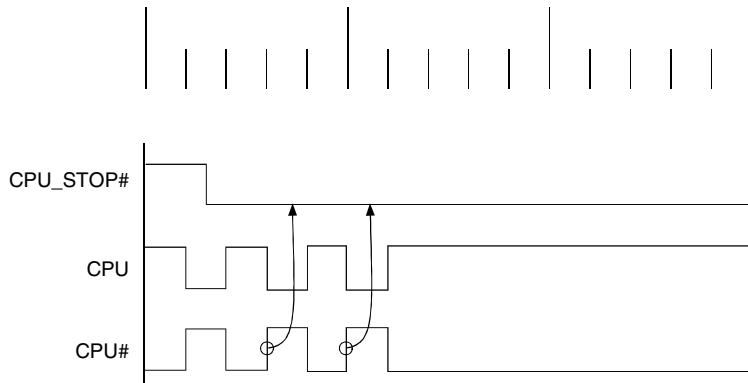
CPU STOP FUNCTIONALITY

The CPU_STOP# signal is an active low input controlling the CPU outputs. This signal can be asserted asynchronously.

CPU_STOP#	CPU	CPU#
1	Normal	Normal
0	High	Low

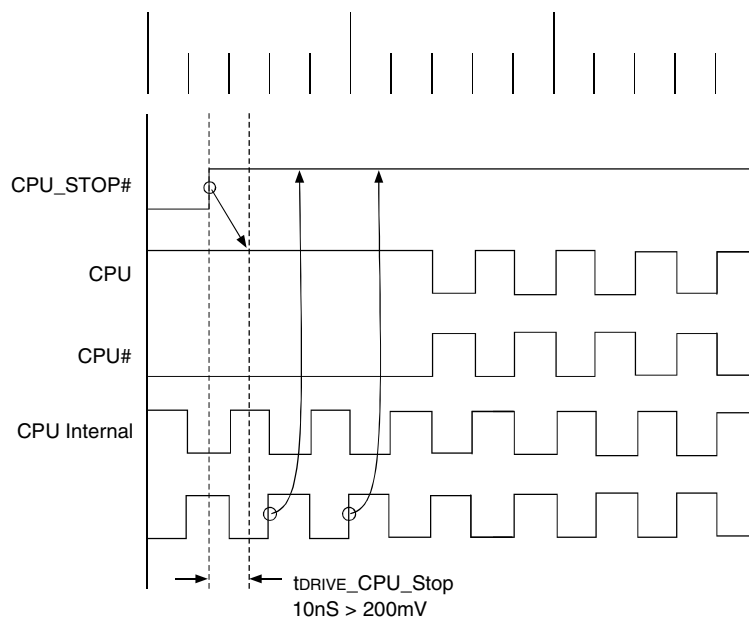
CPU_STOP# ASSERTION (TRANSITION FROM '1' TO '0')

Asserting CPU_STOP# pin stops all CPU outputs that are set to be stoppable after their next transition. When the SMBus CPU_STOP tri-state bit corresponding to the CPU output of interest is programmed to a '0', CPU output will stop CPU_True = High and CPU_Complement = Low. When the SMBus CPU_STOP# tri-state bit corresponding to the CPU output of interest is programmed to a '1', CPU outputs will be tri-stated.



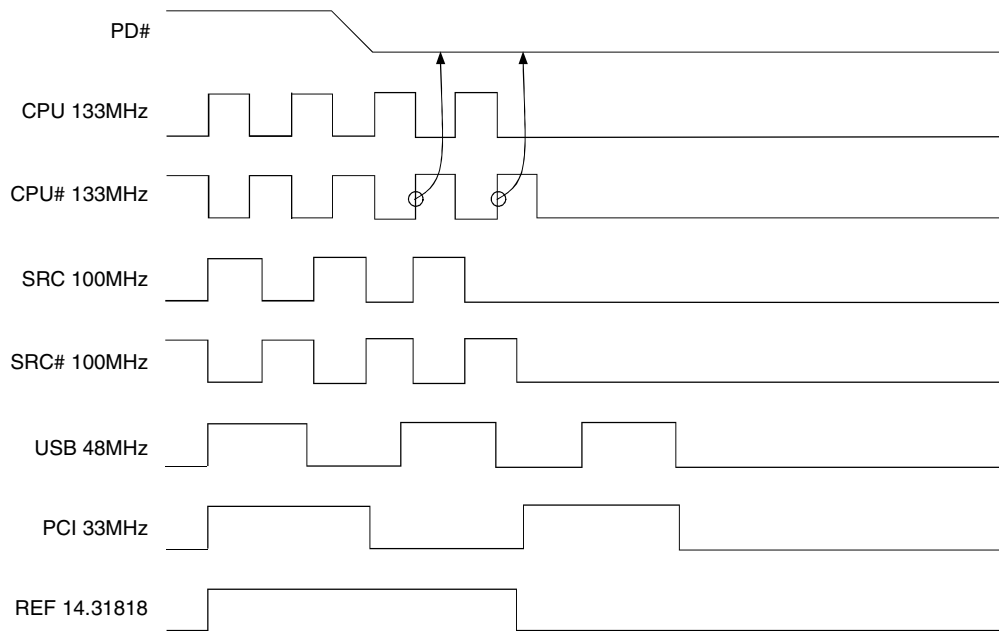
CPU_STOP# - DE-ASSERTION (TRANSITION FROM '0' TO '1')

With the de-assertion of CPU_STOP# all stopped CPU outputs will resume without a glitch. The maximum latency from the de-assertion to active outputs is two to six CPU clock periods. If the control register tristate bit corresponding to the output of interest is programmed to '1', then the stopped CPU outputs will be driven High within 10nS of CPU_STOP# de-assertion to a voltage greater than 200mV.

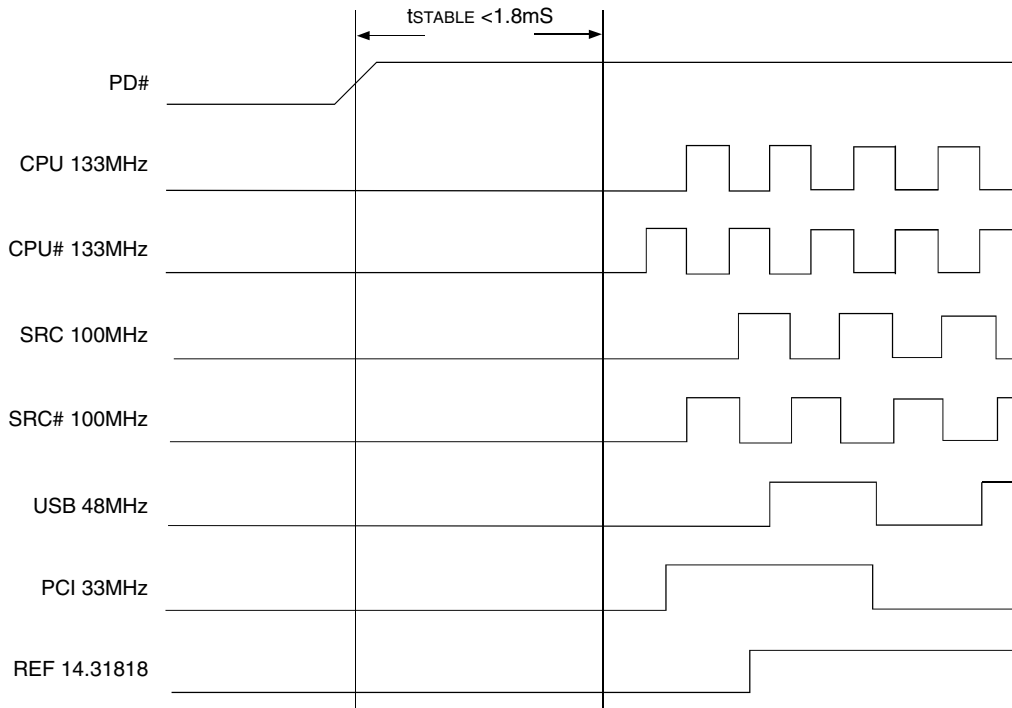


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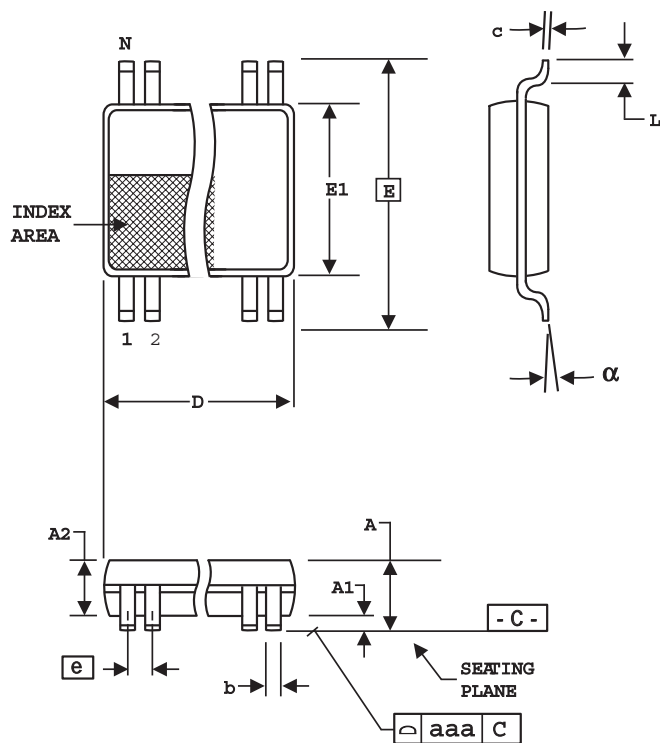
PD# ASSERTION



PD# DE-ASSERTION



TSSOP PACKAGE DIMENSIONS



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS	COMMON DIMENSIONS
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
alpha	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

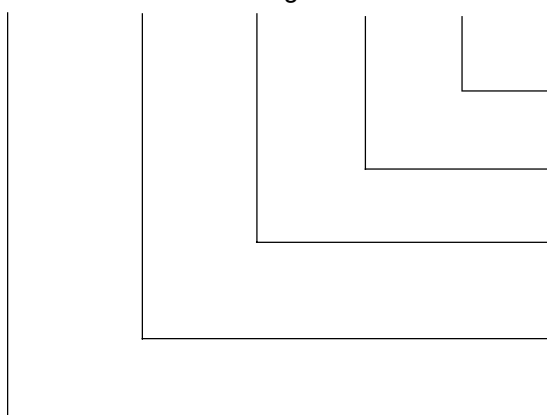
N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
64	16.90	17.10	.665	.673

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

ORDERING INFORMATION

IDTCV XXXX XXX XX X X
Device Type Revision Package T/R Grade



- Blank | Commercial Temperature Range (0°C to +70°C)
- 8 | Designation for tape and reel packaging
- PVG | Shrink Small Outline Package - Green
- PAG | Thin Shrink Small Outline Package - Green
- C | Revision Designator
- 193 | Programmable FlexPC Clock for P4 Processor

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REVISION HISTORY

August 15, 2007	Initial Release.
August 21, 2007	Updated Pinout/Pin Description (pages 2-4). Added Sata_Sel Table (page 5). Updated SMBus (pages 7-12).
December 07, 2007	Updated Byte 18 (pg. 12).
April 08, 2008	Updated VDDxxx_IO supply voltage (pg. 13).
April 24, 2008	Fixed Ordering Information (pg. 20).
June 24, 2008	Added tape and reel ordering information (page 20) Corrected typo on pins 55 and 56 pin description (page 4)
October 20, 2008	Updated Byte 1 (page 7).
April 8, 2009	Updated Input/Supply Common Output Parameters table.

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