WPC1.1-Compatible A5/A11 Wireless Power Transmitter

Product Preview

IDTP9038

Features

- Integrated 5V WPC 1.1-compliant Transmitter for A5 or A11-type coils
- Conforms with WPC Specification 1.1
- Operates from 5V supplies (4.5V to 6.9V)
- Easy to Use, with Reduced Parts Count
- 8W Power Transfer Solution
- Integrated Full-Bridge Inverter for Optimal Coil Drive Ensures Low EMI/RFI Emissions
- Demodulates and Decodes Communication Packets from WPC-compliant Receivers
- Implements Closed-Loop Power Transfer Control
- Optional Proprietary Back-Channel Communication
- Security and Encryption up to 64-bit
- USB Interface Supports High Current Charging with D+ / D- detection
- Master/Slave I^2C Interface

Safety Features

- Over-Current, Over-Voltage, and Over-Temperature Protection
- Fully Integrated Programmable WPC1.1-Compliant Multilayer Foreign Object Detection (FOD)
- Power Good and Fault Condition Detection with LED Indicator outputs

Applications

- Charging Mats or Pads
- Public Facilities – Shops, Libraries, Airports, Schools
- Office Furniture
- Personal Computer Docks
- Portable Instruments

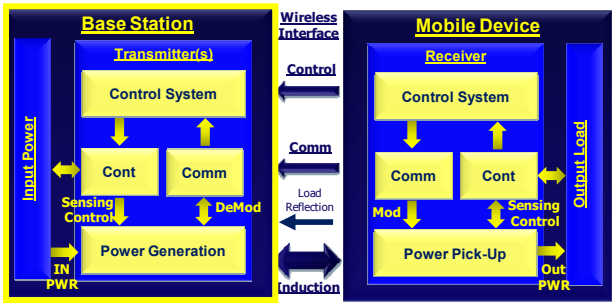
Package: 7x7-56 VFQFN (See page 22)
Ordering Information: (See page 24)

Description

The IDTP9038 is a WPC-compliant Wireless Power Transmitter for A5 and A11 designs operating from 5V supplies which conforms with WPC Specification 1.1. Operating in the WPC-compliant mode, the integrated full-bridge inverter supports 8W power transfer utilizing the IDTP902X Receiver family, and ensures efficient switching with EMI/RFI emissions that are better than the requirements of the WPC specification.

An embedded microcontroller provides extensive control & application flexibility. In addition to implementing the WPC-specified device identification and a closed-loop control protocol which constantly adjusts transmitted power, the IDTP9038 features a proprietary back-channel communication mode compatible with other IDT Wireless Power products, providing secure authentication with data encryption using a Secure Hash Algorithm (SHA) of up to 64 bits.

Featuring programmable multi-layer Foreign Object Detection and built-in Over-Current, Over-Voltage, and Over-Temperature Protection, the IDTP9038 is extremely easy to use and provides a complete WPC-compliant solution with minimum external parts count, requiring significantly less board space and lower total solution cost than competing products. It is available in a compact 7mm x 7mm VQFN package. A complete Evaluation kit is available with an easy-to-use GUI interface, which allows users to quickly verify system performance and implement WPC-compliant designs with minimal effort.



ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the IDTP9038 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods may affect long-term reliability.

Table 1. Absolute Maximum Ratings Summary. (All voltages are referred to ground.)

Pins	Rating	Units
VBUS_SNS	-0.3 to 27	V
$\overline{EN}$, IN, REG_IN, , SW1, SW2, ISNSN_IN, ISNSP_IN	-0.3 to 12.5	V
GPIO_6:0, SCL, SDA, RESET, DP, DM, NC, NC1, NC2, NC3, SHIELD2, LDO5V, LDO2P5V_IN, INV5V_IN, VFOD_SNS, ISNS, HPF, OVP_SEL, ISNS_V	-0.3 to 5.5	V
BST1, BST2	-0.3 to SW+6	V
GATE	-0.3 to REG_IN+6	V
GND, REFGND, PGND1, PGND2	±0.3	V
SHIELD1	-0.3 to 8	V
LDO2P5V	-0.3 to 2.75	V

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	TQFN RATING	UNITS
Θ_{JA}	Thermal Resistance Junction to Ambient	25.5	°C/W
Θ_{JC}	Thermal Resistance Junction to Case	8.6	°C/W
Θ_{JB}	Thermal Resistance Junction to Board	2.4	°C/W
T_J	Operating Junction Temperature	-40 to +125	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 3. ESD Information

TEST MODEL	PINS	RATINGS	UNITS
HBM	All pins.	+/- 2000	V
CDM	All pins.	+/- 500	V

SPECIFICATION TABLE

Table 4. Device Characteristics

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IBUS} = 1µF, C_{BYPASS} = 40µF, Coil = A5, C_{OUT_T1} = 400nF, T_A =-40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typ	Max	Units
Input Supplies & UVLO						
V_{BUS}	Input Operating range	VBUS_MIN to OVP_Max	4.5		6.9	V
I_{IN_REGIN} NOTE 2	Operating Input Current	After power-up sequence complete, No coil, 175kHz switching at SW1, SW2, LDO5V, LDO2P5V.		33	45	mA
	Standby Input Current (no ping)	After power-up sequence complete. No coil, no switching at SW1, SW2, LDO5V, LDO2P5V.		8	12	mA
	Standby Input Current (pinging)	After power-up sequence complete. Average including pinging		15		mA
	Sleep Mode Input Current	$\overline{EN}$ = REG_IN = 6.9V			600	uA
$I_{IN\_VBUS\_SNS}$	VBUS_SNS Input Current	VBUS_SNS = 6.9V			1	mA
V_{REGIN_UVLO}	REGIN Under-Voltage Protection Trip Points	Rising			4.1	V
		Falling	3.4			V
		Hysteresis	150			mV
Full Bridge PWM Generators						
F_{SW}	Switching frequency		110		205	kHz
F_{SW} LSB	Switching Frequency Step Size			12.5		ns
Duty	Duty cycle	V_{REG}=4.5V-6.9V	10	50	90	%
Full Bridge Inverter						
$I_{HS\_OCP\_RNG}$	Over-Current Protection Trip Point Range	V_{IN} = 5V, cycle-by-cycle protection., programmable Range	3		15	A
$I_{HS\_OCP\_ACC}$	Over-Current Protection Trip Point Accuracy	V_{IN}=5V, OCP Setting = 5A	-20		20	%
Input OVP, Inrush Control, and Current Limit						
V_{BUS_OVP}	VBUS Over-Voltage Protection Trip Point	V_{BUS} rising, OVP_SEL pin grounded	6.7	7.15		V
		V_{BUS} rising, OVP_SEL pin 220k 5% to GND	5.8	6.3		V
		V_{BUS} rising, OVP_SEL pin Floating	7.3	7.85		V
		Hysteresis	200			mV
T_{GATE_RISE}	GATE Voltage rise time	VBUS=5V, Gate cap = 4nF V_{GATE}=1V to VIN+4V		3.6		ms
D_{GATE_FALL}	Delay from input OVP to GATE Voltage pull down	VGATE Pull down Time, Gate cap = 4nF V_{GATE} = VIN+4V to VIN		400		ns
I_{GATE_LKG}	GATE Leakage	VBUS_SNS=0V, REG_IN=5V, VGATE=10V	-1		+1	µA
Input Average Current Sense						
$ISEN_{IR}$	Input Range	ISNSP_IN, ISNSN_IN	REGIN -0.3V	-	REGIN +0.15V	V
$ISEN_{ACC}$	Measured Current sense accuracy	V_{REGIN} = 4.5 to 7.2V, I_{SENSR} = 1.5A, Note 1		+/- 3		%

Table 4. Device Characteristics, Continued

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IBUS} = 1µF, C_{BYPASS} = 40µF, Coil = A5, C_{OUT_T1} = 400nF, T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typ	Max	Units
Analog to Digital Converter						
N	Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			125		kSa/s
ADC_{CLK}	Clock Rate			2		MHz
$V_{IN,FS}$	Full scale Input voltage			2.44		V
LDO2P5V: Note 3						
V_{IN}	Input voltage			5		V
V_{OUT}	Output voltage	I_{LOAD} = 5 mA		2.5		V
I_{OUT_MAX}	Maximum Output current				5	mA
LDO5V: Note 3						
V_{IN}	Input voltage		4.5		6.9	V
V_{OUT}	Output voltage	I_{LOAD}=10 mA, REG_IN=5.5		5		V
I_{OUT_MAX}	Maximum Output Current				10	mA
Thermal Shutdown						
T_{SD}	Thermal shutdown	Threshold Rising		140		°C
		Threshold Falling		110		°C
Microcontroller						
F_{CLOCK}	Clock frequency			40		MHz
V_{IN}	Input voltage			2.5		V
$\overline{EN}$						
V_{IH}			1.1			V
V_{IL}					0.3	V
$I_{\overline{EN}}$	$\overline{EN}$ input current	$V_{\overline{EN}}$ = 6.9V			25	µA
General Purpose Inputs / Outputs (GPIO)						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
V_{OH}	Output Logic High	I_{OH}=-8mA	4			V
V_{OL}	Output Logic Low	I_{OL}=8mA			0.5	V
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
DP/DM CHARGER DETECTION						
V_{DP_SRC} V_{DM_SRC}	DP and DM Voltage Source			0.6		V
	DP and DM Voltage Source Output Source Current	V_{DP} or V_{DM} between 0.5V and 0.7V	250			µA
	DP and DM Voltage Source Output Sink Current	V_{DP} or V_{DM} at 2.2 V			500	µA

Table 4. Device Characteristics, Continued

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IBUS} = 1µF, C_{BYPASS} = 40µF, Coil = A5, C_{OUT_T1} = 400nF, T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Symbol	Description	Conditions/Notes	Min	Typ	Max	Units
IDP_SINK IDM_SINK	Current Sink		25	100	175	µA
IDP_SRC	Current Source		7		13	µA
VDAT_REF	Data detect voltage		0.25		0.4	V
VDP/DM_LGCHI	Logic High		2.0			V
VDP/DM_LGCLO	Logic Low				0.8	V
RDP_DWN	Pull-down Resistance		14.25	19.5	24.8	kOhms
CI	Input Capacitance	Dm pin, Switch Open		4.5	5	pF
		Dp pin, Switch Open		4.5	5	pF
IILK	Input Leakage	Dm pin, Switch Open V = 5.0	-1		+1	µA
		Dp pin, Switch Open V = 5.0	-1		+1	µA
SCL, SDA (I²C Interface)						
f_{SCL_MSTR1}	Clock Frequency	EEPROM Loading, Step 1 IDTP9038 at Master		300		kHz
f_{SCL_MSTR2}	Clock Frequency	EEPROM Loading, Step 2, IDTP9038 as Master		100		kHz
f_{SCL_SLV}	Clock Frequency	IDTP9038 as Slave	0		400	kHz
$t_{HD,STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD:DAT}$	Data Hold Time	I2C-bus devices	10			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU:STA}$	Set-up Time for Repeated START Condition		100			ns
t_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance[5]			5		pF
V_{IL}	Input Threshold Low				0.4	V
V_{IH}	Input Threshold High		1.4			V
I_{LKG}	Input Leakage Current	V = 0 V & 5 V	-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I = 2mA			0.25	V

NOTE 1: 10mΩ, 1% or better sense resistor & 10 Ω, 1% input filter resistors are required to meet the FOD specification
NOTE 2: This current is the sum of the input currents for REG_IN, IN, ISNSP_IN, ISNSN_IN, and EN_B
NOTE 3: For IC operation only - do not externally load
NOTE 4: Guaranteed by Design

PIN CONFIGURATION & DESCRIPTION

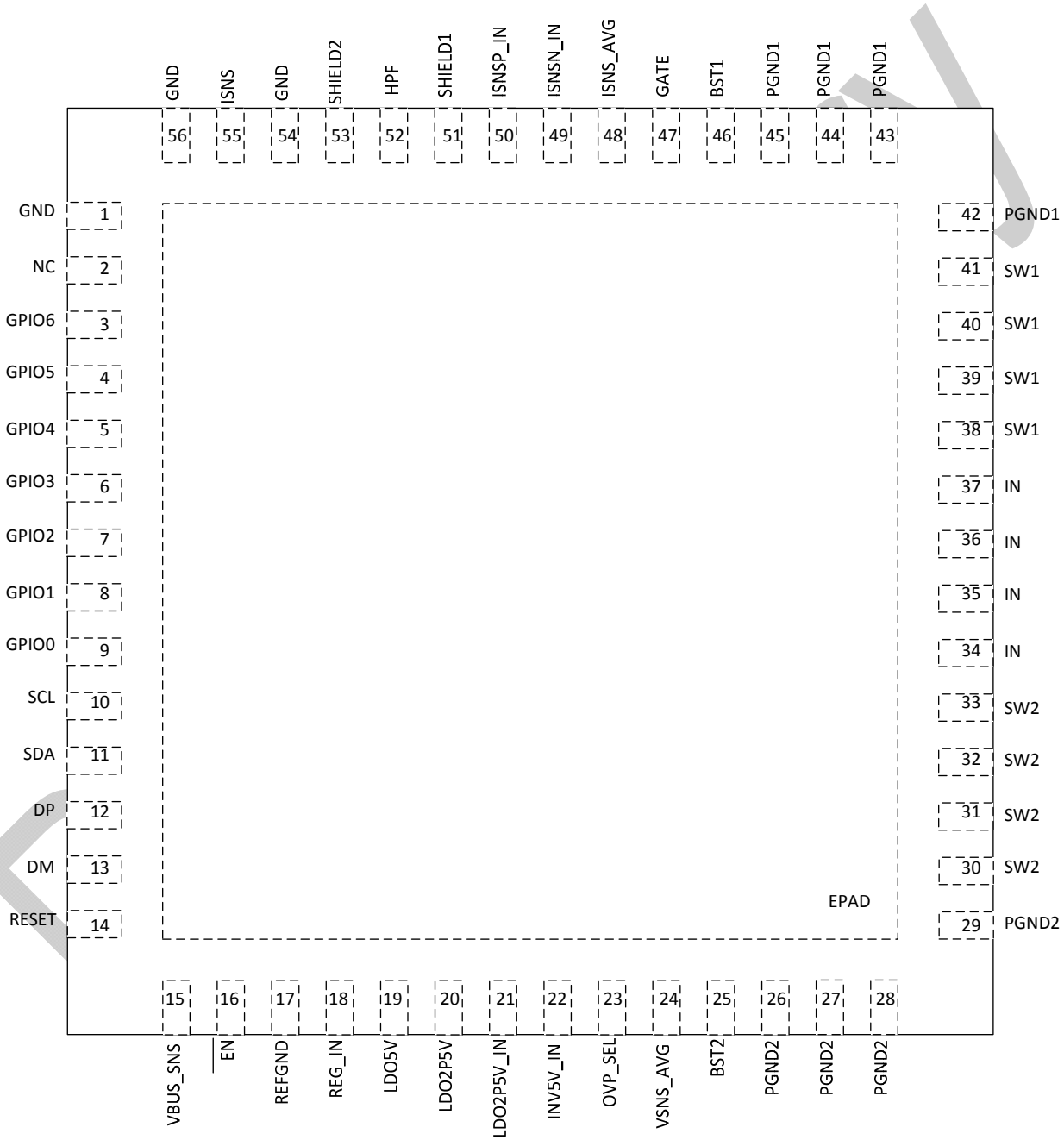


Figure 1. TQFN-56 7mmx7mm

Table 5. Pin Descriptions

PIN(s)	Name	Type	Function
1	GND	I	Signal Ground Connection.
2	NC	-	Internally connected, do not connect
3	GPIO6	I/O	General Purpose Input/Output. Configured as an output.
4	GPIO5	I/O	General Purpose Input/Output
5	GPIO4	I/O	General Purpose Input/Output. Configured as an output.
6	GPIO3	I/O	General Purpose Input/Output. Configured as an output.
7	GPIO2	I/O	General Purpose Input/Output. Configured as an input.
8	GPIO1	I/O	General Purpose Input/Output. Configured as an input.
9	GPIO0	I/O	General Purpose Input/Output
10	SCL	I/O	I^2C Clock
11	SDA	I/O	I^2C Data
12	DP	I/O	USB Data Positive Input
13	DM	I/O	USB Data Negative Input
14	RESET	I	Active-high Reset Pin. 1uF to LDO5V and 100kohms to GND
15	VBUS_SNS	I	VBUS OVP sense point & supply for OVP circuitry
16	$\overline{EN}$	I	Active-low Enable Pin.
17	REFGND	PWR	Signal Ground Connection. Connect to AGND
18	REG_IN	PWR	5V LDO Input
19	LDO5V	O	5V LDO Output. 1uF Capacitor to GND
20	LOD2P5V	O	2.5V LDO Output. 1uF Capacitor to GND
21	LDO2P5_IN	PWR	2.5V LDO Input
22	INV5V_IN	PWR	5V Inverter Driver Stage Input Supply
23	OVP_SEL	I	Selects 3 OVP thresholds (tie to GND, float, tie to LDO5V)
24	VSNS_AVG	I	Scaled average input voltage sense signal used for FOD.
25	BST2	I	Bootstrap pin for SW2 Bridge Node
26,27,28,29	PGND2	GND	Power Ground
30,31,32,33	SW2	O	Full H-Bridge Switch Node 2
34,35,36,37	IN	I	Full H-Bridge Power Supply Input
38,39,40,41	SW1	O	H-Bridge Switch Node 1
42,43,44,45	PGND1	GND	Power Ground
46	BST1	I	Bootstrap pin for SW2 Bridge Node
47	GATE	O	Inrush FET Gate Driver Node
48	ISNS_AVG	I	Scaled average input current sense signal used for FOD. Adjust cap to GND for filtering
49	ISNSN_IN	I	Input Current Sense Negative Input
50	ISNSP_IN	I	Input Current Sense Positive Input
51	SHIELD1	O	Shield output for HPF pin
52	HPF	I	High Pass Filter Input for Demodulator
53	SHIELD2	O	Shield output for HPF pin
54	GND	I	Signal Ground Connection.
55	ISNS	O	High side current ISNS Output Signal
56	GND	I	Signal Ground Connection.
EP	EP	GND	Exposed Pad. Connect to GND

INTERNAL BLOCK DIAGRAM

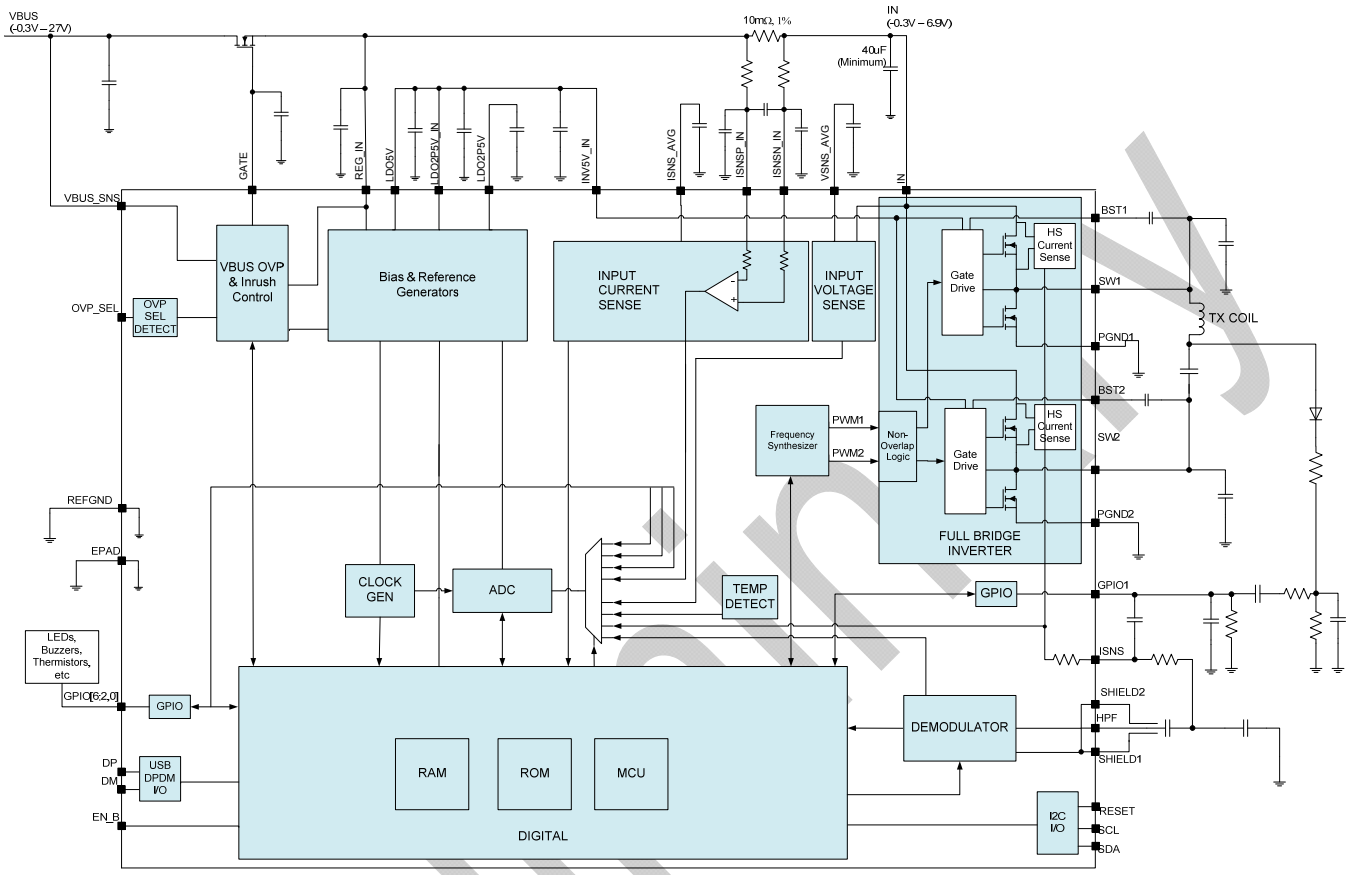


Figure 2. IDTP9038 Internal Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

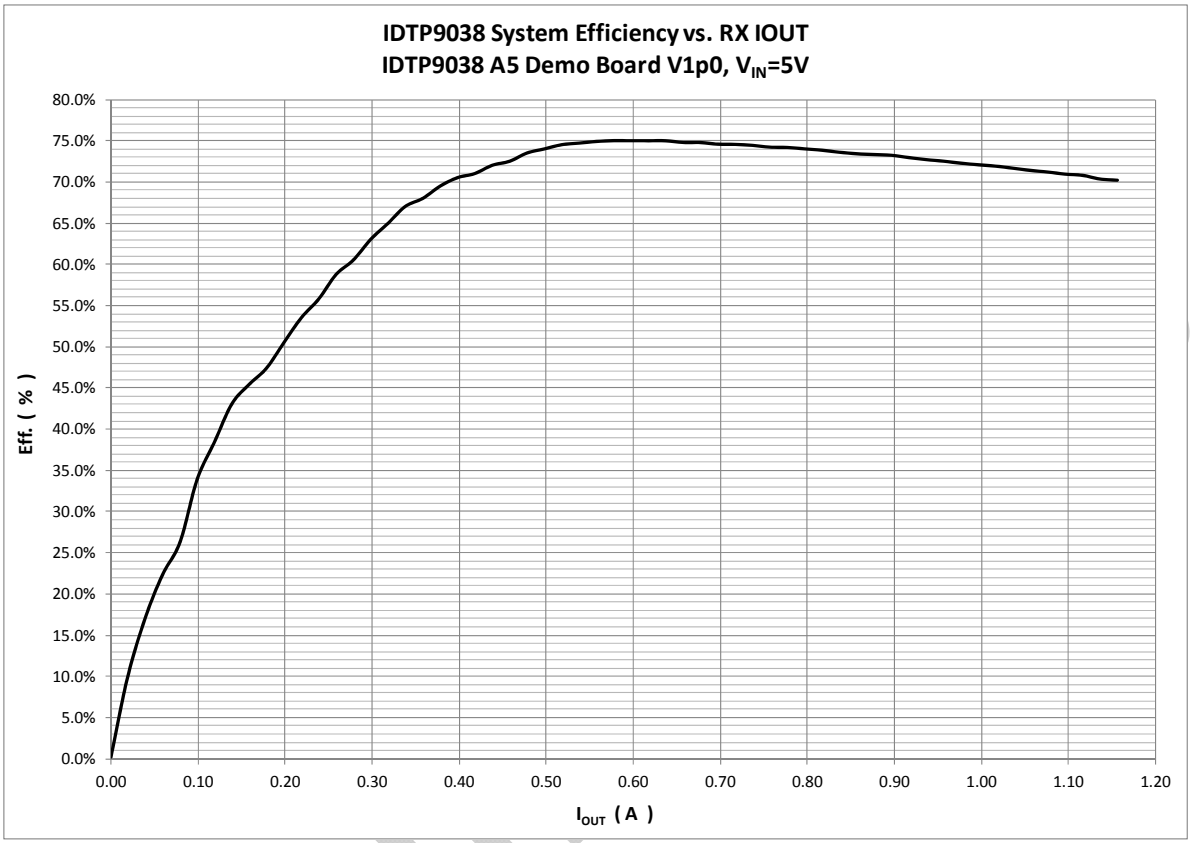


Figure 3. Efficiency vs RX Output Current, VIN=5V

Table 6. IDTP9038 Die Temperature No Load vs RX IOUT=5A, T_A=25C

Input Voltage	Temp (°C) No Load	Temp (°C) Full Load	Temp. Change
4.5V	34.7	37.2	2.5
5.0V	34.9	37.4	2.5
5.5V	35.2	38.5	3.3

Figure 4. Inrush Current Limit Operation

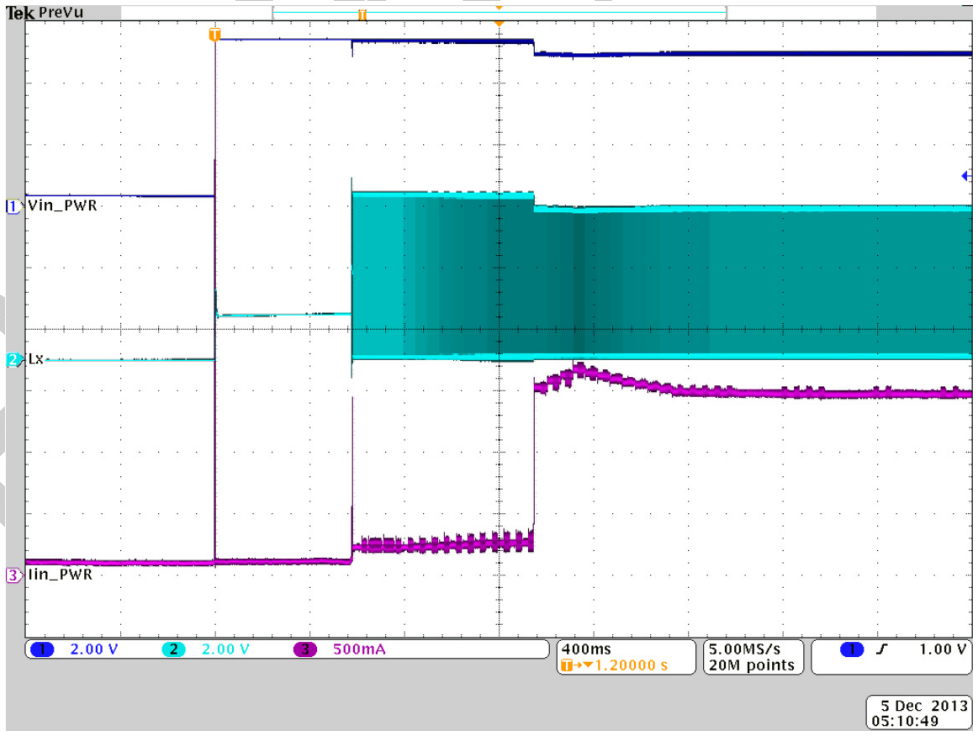


Figure 5. System Startup with RX IOUT=1A

SIMPLIFIED APPLICATION DIAGRAM

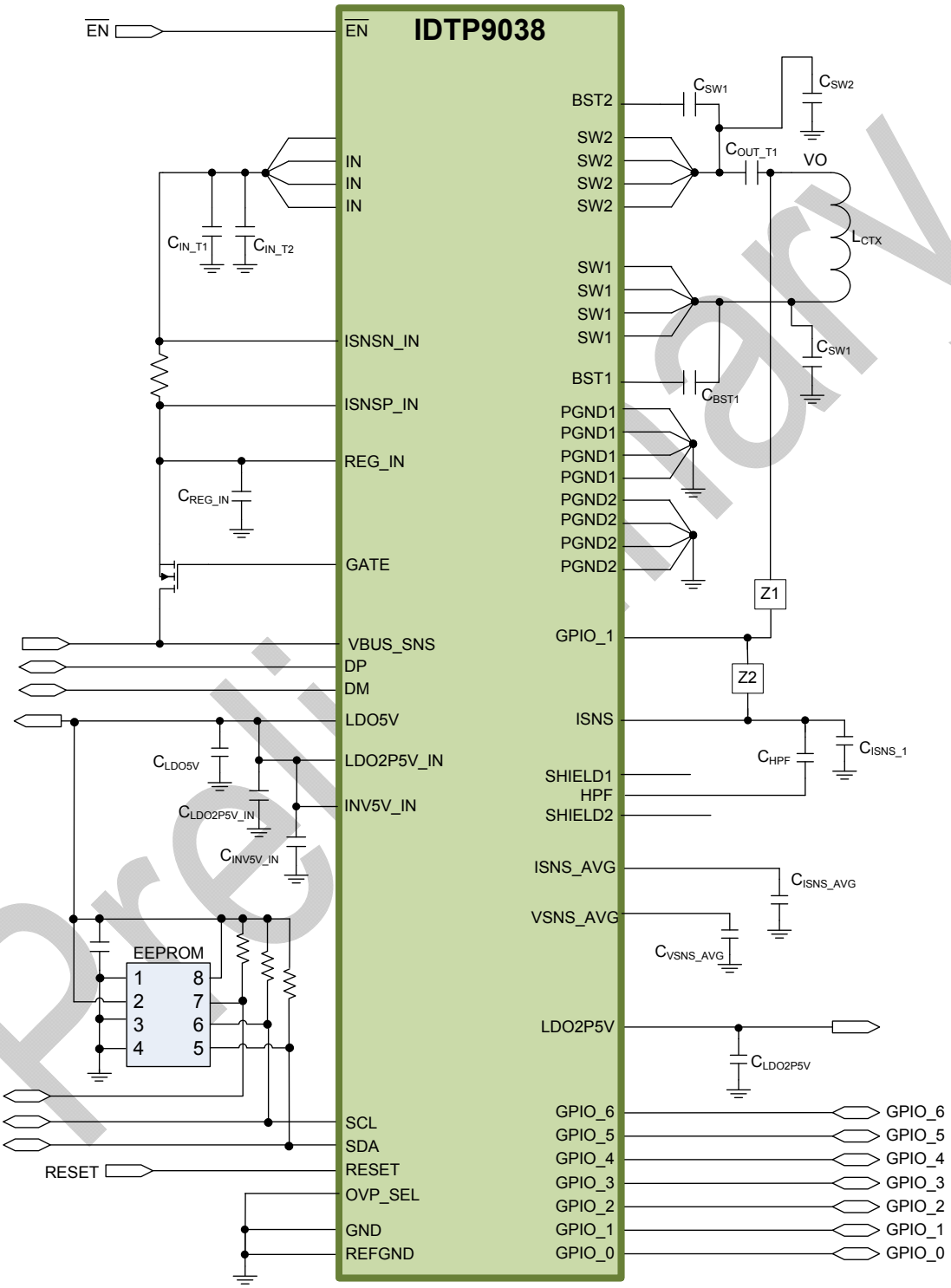


Figure 6. Typical Application Circuit, 4.5 V to OVP

SIMPLIFIED SYSTEM APPLICATION DIAGRAM

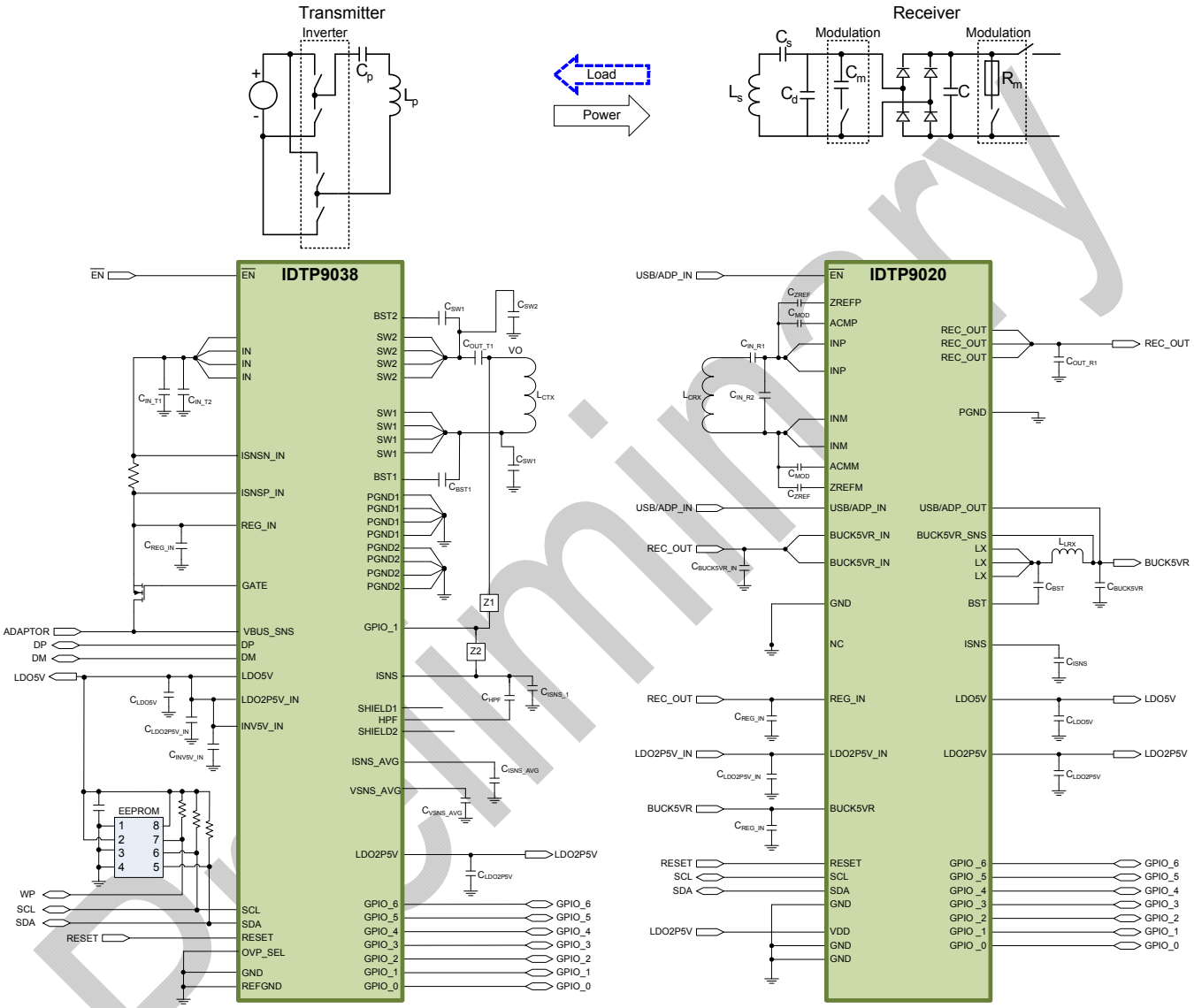


Figure 7. Typical System Application Circuit

Description of the Wireless Power Charging System

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. A WPC[1] transmitter may be a *free-positioning* or *magnetically-guided* type. A *free-positioning* type of transmitter has an array of coils that gives limited spatial freedom to the end-user, whereas a *magnetically-guided* type of transmitter helps the end-user align the receiver to the transmitter with a magnetic attraction.

The amount of power transferred to the mobile device is controlled by the receiver. The receiver sends communication packets to the transmitter to increase power, decrease power, or maintain the power level. The communication is purely digital, and communication 1's and 0's ride on top of the power link that exists between the two coils.

To conserve power, the transmitter places itself in a very-low-power sleep mode unless it detects the presence of a receiver. Once a receiver is detected, the transmitter exits sleep mode and begins the power transfer per the WPC specification.

INPUT SUPPLIES AND UNDER-VOLTAGE LOCKOUT

The IDTP9038 receives a VBUS input voltage that is filtered and limited to generate an input rail (REG_IN) which powers the IC and its inverters, and to which the majority of the input bulk decoupling capacitance is attached. The REG_IN rail has a nominal operating range of 4.5V to 6.9V, with over-voltage protection (OVP) limiting the voltage up to 7.85V. This voltage range is measured at the VBUS input to the system. The actual voltage at REG_IN will be lower than that at VBUS due to the voltage drop in the OVP MOSFET. The REG_IN UVLO enables and disables the IDTP9038's power inverters.

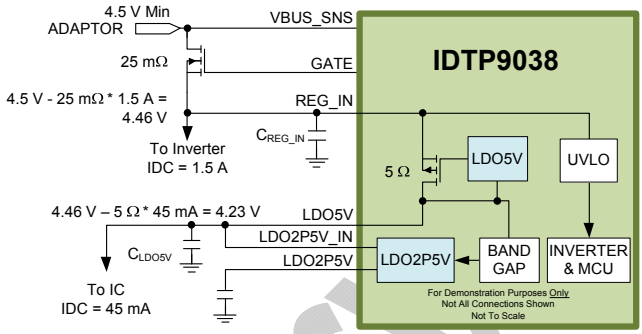


Figure 8. Input Voltage Support Range (UVLO)

The GATE pin and associated MOSFET shown in Fig. 8 provide protection for the IDTP9038 from input over-voltage events and control current inrush. Both of these features are described in subsequent sections of this document.

FULL-BRIDGE MOSFET DRIVE AND MOSFET CURRENT SENSE

The IDTP9038 incorporates an integrated full-bridge inverter. Each half-bridge contains a high-side current sense block that is used for control and for peak current protection. For EMI reduction purposes, the switching rising and falling rates of the internal MOSFETs are limited.

INPUT OVER-VOLTAGE PROTECTION AND SLEW RATE CONTROL

The IDTP9038 is powered from a VBUS input which may be subjected to voltages above 5.5V under normal operation. The IDTP9038 is required to support voltages as high as 27 V on this input. An external OVP MOSFET is used to isolate pins that would be damaged by a 27 V transient on the VBUS input. The OVP MOSFET has a second function: limiting inrush current from the VBUS line to 150 mA during startup. This is necessary due to the USB inrush specification and the large total effective capacitance (~40μF) on the REG_IN and IN pins of the IC.

The IDTP9038 monitors the VBUS_SNS pin for OVP events and shuts off the OVP MOSFET should one be detected. In order to protect the VBUS line from regulator-induced OVP events, the REG_IN pin is also monitored for over-voltage faults. The OVP trip threshold can be configured via a single pin to one of 3 preprogrammed Over-Voltage Protection set points, as shown in Table 7.

Table 7. VBUS OVP Threshold Selection

OVP_SEL pin connection	OVP threshold
220kΩ to ground	6.3V
Grounded	7.15V
Floating	7.85V

A secondary over voltage protection with a 9.5V threshold is implemented on REG_IN for cases where the OVP MOSFET is bypassed. The IC is disabled until the REG_IN voltage drops below 8V.

DEMODULATION

Power transfer from the IDTP9038 to a WPC-compliant wireless power receiver is controlled by the receiver. Communication packets are superimposed on the power link between the two devices, and are demodulated by the IDTP9038. Further information about the WPC communication protocol can be found at the WPC website[1]. Communication can be made more robust by running traces from Shield1 and Shield2 along the HPF trace.

ANALOG-TO-DIGITAL CONVERTER [ADC]

The ADC is the main functional block which the MCU uses for IC protection including Foreign Object Detection. It also digitizes several internal and external voltages and currents for overall system control and improved demodulation functionality.

USB DP/DM FUNCTIONALITY

The IDTP9038 implements USB D+/D- detection derived from the BCS1.2 specification. The type of USB port powering the IDTP9038 is recognized and stored in internal registers for use by firmware or for customer specific functions.

FOREIGN OBJECT DETECTION AND INPUT OVER-CURRENT PROTECTION

The IDTP9038 makes precision measurements of the input voltage and input current, which are sampled by the internal ADC and processed in firmware for WPC 1.1 Foreign Object Detection [FOD] compliance. Two external pins, ISNS_AVG and VSNS_AVG, are provided for filtering the input current sense and input voltage sense signals respectively.

The input current sense signal is generated from the ISNSP_IN and ISNSN_IN pins. This input current sense signal is filtered with an internal 50kΩ resistor and an external capacitor on the ISNS_AVG pin (1nF Typical).

The output impedance of the VSNS_AVG pin is approximately 33kOhms. A capacitor on the VSNS_AVG pin provides filtering for input voltage measurements. It is recommended that matching large time constants be used on VSNS_AVG and ISNS_AVG signals, on the order of 500 μs, to prevent ADC aliasing of the resulting measurements.

EXTERNAL CHIP RESET and $\overline{EN}$

The IDTP9038 can be externally reset by pulling the RESET pin to a logic high (above the V_{IH} level).

The RESET pin is a dedicated high-impedance active-high digital input, and its effect is similar to the power-up reset function. Because of the internal low voltage monitoring scheme, the use of the external RESET pin is not mandatory. If desired, a manual external reset scheme can be added by connecting 5V to the RESET pin through a simple switch. When RESET is HIGH, the microcontroller's registers are set to the default configuration. When the RESET pin is released to a LOW, the microcontroller starts loading and executing the code from the external EEPROM.

If the particular application requires the IDTP9038 to be disabled, this can be accomplished with the $\overline{EN}$ pin. When the $\overline{EN}$ pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active.

The current into $\overline{EN}$ is approximately equal to:

$$I(\overline{EN}) = \frac{V(\overline{EN}-2V)}{300k},$$

or close to zero if V($\overline{EN}$) is less than 2V.

SYSTEM FEEDBACK CONTROL

For the full description of the communication and control protocol used by the IDTP9038, please refer to the WPC website[1].

Note 1 - Refer to the WPC specification at http://www.wirelesspowerconsortium.com/ for the most current information

APPLICATIONS INFORMATION

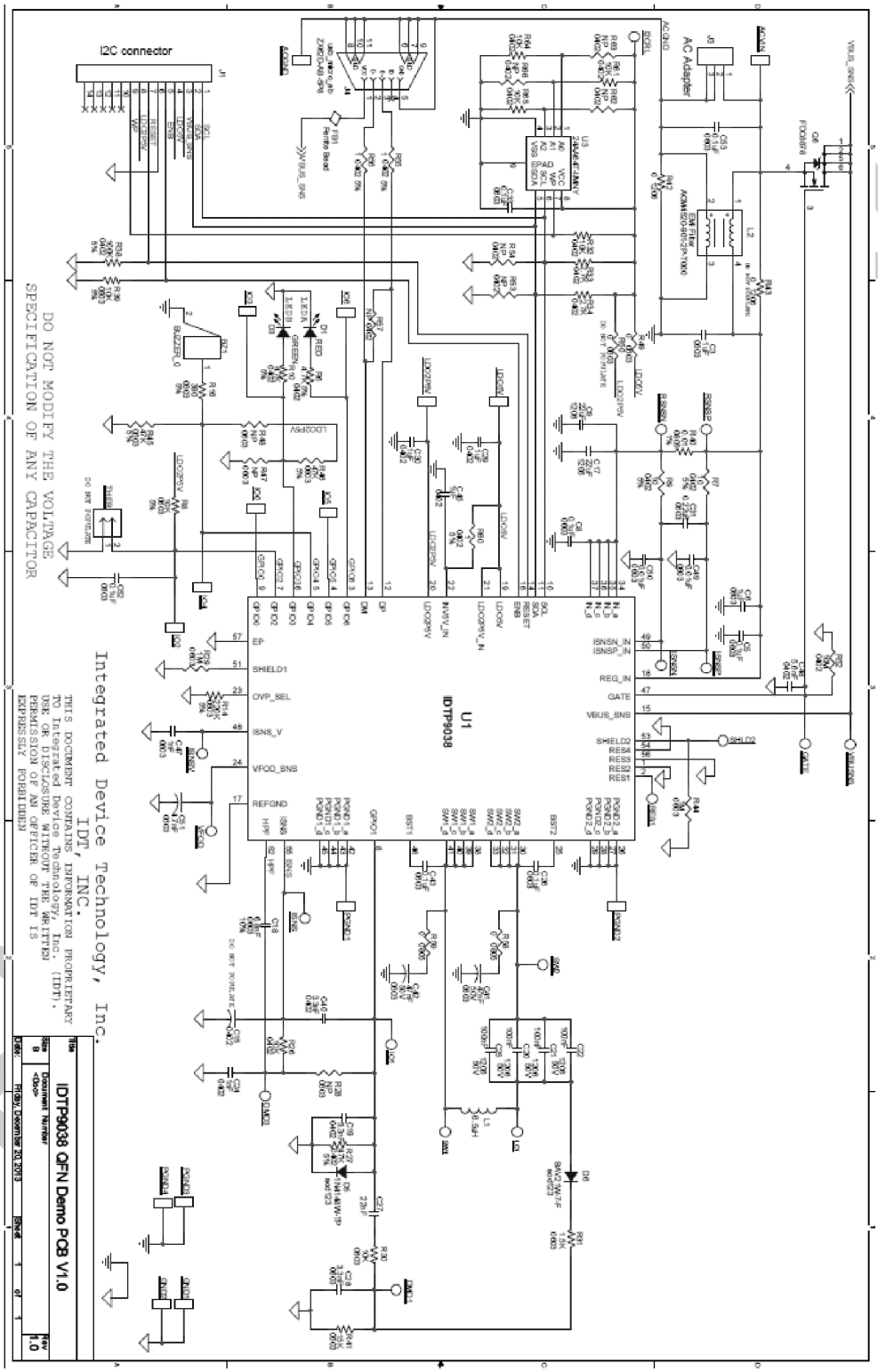


Figure 9. IDTP9038 Preliminary Application Schematic

Components Selection

Table 8. Component List

Item	Qty	Reference	Part	Part_Number	PCB Footprint
1	1	BZ1	Buzzer_0	PS1240P02CT3	buzz_ps1240
2	2	C3,C6	1uF	C1608X7R1E105K	0603
3	7	C5,C8,C26,C33,C43,C52,C53	0.1uF	GRM188R71H104KA93D	0603
4	2	C9,C17	22uF	GRM31CR61E226KE15L	1206
5	1	C15	NP	NP	0402
6	1	C18	6.8nF	C1608X8R1H682K080AA	0603
7	1	C19	3.3nF	C1005X7R1H332K	0402
8	4	C20,C21,C22,C25	100nF	C3216C0G1H104J160AA	1206
9	1	C24	1nF	C1005X7R1H102K	0402
10	1	C27	22nF	C1608X7R1H223K	0603
11	1	C28	3.3nF	C1608X7R2A332K	0603
12	3	C29,C30,C45	1uF	0402ZD105KAT2A	0402
13	1	C31	0.22uF	C0603C224J4RACTU	0603
14	1	C40	3.3nF	C1005X7R1H332K050BA	0402
15	2	C41,C42	47nF	C0603C473K5RACTU	0603
16	1	C47	1nF	C1608C0G2A102J	0603
17	1	C48	5.6nF	C1608C0G1H562J	0603
18	2	C49,C50	0.01uF	06035C103KAT2A	0603
19	1	C51	4.7nF	06035C472KAT2A	0603
20	1	D1	RED	LS L29K-G1J2-1-Z	0603_DIODE
21	1	D3	GREEN	LG L29K-G2J1-24-Z	0603_DIODE
22	1	D5	DIO_SW	1N4148W-TP	sod123
23	1	D6	Diode	BAV21W-7-F	sod123
24	1	FB1	Ferrite Bead	MPZ1608S300A	0603
25	1	J1	I2C connector	5103308-2	LOPRO14PIN01INREVB
26	1	J3	AC Adapter	PJ-018H	CONN_POWER_JACK5_5MM
27	1	J4	5P	ZX62D-AB-5P8	usb_micro_ab
28	1	L1	6.5uH	760308111	IND_Y31-60014F
29	1	L2	EMI Filter	ACM4520-901-2P-T000	tdk_acm4520
30	1	THER	2p header	22032021 (NP)	P_002_1R
31	1	Q6	FDC8878	FDC8878	ssot6
32	2	R6,R10	4.7K	ERJ-2GEJ472X	0402
33	2	R7,R9	10	AC0402JR-0710RL	0402
34	2	R8,R39	10K	ERJ-2GEJ103X	0603
35	1	R14	220K	ERJ-3GEYJ224V	0603
36	1	R16	390	ERJ-3GEYJ391V	0603
37	5	R26,R32,R61,R64,R65	10K	RC0402FR-0710KL	0402
38	1	R27	47K	ERJ-2GEJ473X	0402
39	3	R28,R47,R48	NP	NP	0603
40	2	R29,R44	1M	ERJ-3GEYJ105V	0603
41	1	R30	10K	ERJ-3EKF1002V	0603
42	1	R31	1.5K	ERJ-3EKF1501V	0603
43	2	R33,R34	2.7K	ERJ-2GEJ272X	0402
44	1	R38	100K	ERJ-2GEJ104X	0402
45	1	R40	0.01	TLRH2ATTD10L0F	0805
46	1	R41	15K	ERJ-3GEYJ153V	0603
47	1	R42	0	ERJ-8GEY0R00V	1206
48	1	R43	NP	ERJ-8GEY0R00V (DO NOT POPULATE)	1206
49	1	R45	47K	ERJ-3GEYJ473V	0603
50	1	R49	0	CRCW06030000ZSTA	0603
51	2	R46,R50	NP	NP	0603
52	1	R52	10M	RK73H1JTTD1005F	0603
53	6	R53, R54,R57,R62,R63,R66	NP	NP	0402
54	2	R58,R59	0	ERJ-6GEY0R00V	0805
55	3	R55,R56,R60	1	RK73B1JTTDD1R0J	0402
56	16	PGND1, GND1, PGND2, IO2, GND2, PGND3, IO3, PGND4, IO4, LDO5V, IO5, IO6, LDO2P5V, IO0, ACVIN, ACGND	Test Point_SM	5015	test_pt_sm_135x70
57	1	U1	IDTP9038	IDTP9038	qfn56_idt
58	1	U3	24AA64T-I/MNY	24AA64T-I/MNY	DFN8
59	18	SW1, RES1, LC1, IO1, DMD1, SW2, SHLD2, I2CRL, DMD3, VFOD, VBUSNS, RSNSP, RSNSN, ISNSV, ISNSP, ISNSN, ISNS, GATE	30AWG	NP	30AWG

External Components

The IDTP9038 requires a minimum number of external components for proper operation (see the BOM in Table 8). A complete design schematic compliant to the WPC "Qi" standard is given in Figure 9. It includes WPC "Qi" LED and buzzer signaling, and an EEPROM for loading IDTP9038 firmware.

I²C Communication

The IDTP9038 includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the IDTP9038 will initially acts as an I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the IDTP9038 does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the IDTP9038 has finished any firmware uploading and has released control of the bus as I²C Master. After any firmware uploading from external memory is complete, and when the IDTP9038 begins normal operation, the IDTP9038 is normally configured by the firmware to be exclusively in I²C Slave mode.

For maximum flexibility, the IDTP9038 tries to communicate with the first address on the EEPROM at 300kHz. If no ACK is received, communication is attempted at the other addresses at 100kHz.

EEPROM

The IDTP9038 EVK uses an external EEPROM memory chip, pre-programmed with a standard start-up program that is automatically loaded when 5V power is applied. The IDTP9038 uses I²C master address 0x52 to access the EEPROM. The IDTP9038 slave address is 0x39. The EEPROM can be reprogrammed to update the start-up program using the IDT Windows GUI (see the IDTP9038-Qi Demo Board User Manual for complete details). A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard firmware is not suitable for the application, custom EEPROM options are possible. IDT will provide the appropriate image in the format best suited to the application. The IDTP9038 contains an internal ROM that can be modified to match application requirements. Please contact IDT sales for more information.

Overview of Standard GPIO Usage

There are 7 GPIO's on the IDTP9038 transmitter IC, of which four are available for use as follows:

- GPIO2: This pin can be connected to an external thermister, the voltage of which is digitized by the IDTP9038's ADC.
- GPIO3: Green LED_B to indicate standby, power transfer, and power complete; see Table 9.
- GPIO4: AC or DC buzzer (optional) with resistor options for different buzzer configurations
- GPIO6: Red LED_A to indicate standby, fault conditions, and FOD warnings. Table 9 lists how the red and green LEDs can be used to display information about the IDTP9038's operating modes. The table also includes information about external resistors or internal pull up/down options to select LED modes. Eight of the ten LED modes (those associated with advanced charging modes) are currently designated as "Future" modes.

All GPIOs are configured as inputs during the boot process, and then reconfigured according to Table 9.

LED FUNCTIONS

The two GPIOs used to drive LEDs indicate, through various on/off and illumination options, the state of charging and some possible fault conditions.

A red LED indicates various Fault and FOD ("Foreign Object Detection") states. The green LED indicates Power Transfer and Charge Complete state information. Upon power up, the two LEDs together may optionally indicate the Standby State and remain in this state until another of the defined Operational States occurs

As shown in Figure 10, one or two resistors configure the defined LED option combinations. The DC voltage set in this way is read one time during power-on to determine the LED configuration. To avoid interfering with the LED operation, the useful DC voltage range must be limited to not greater than 1Vdc.

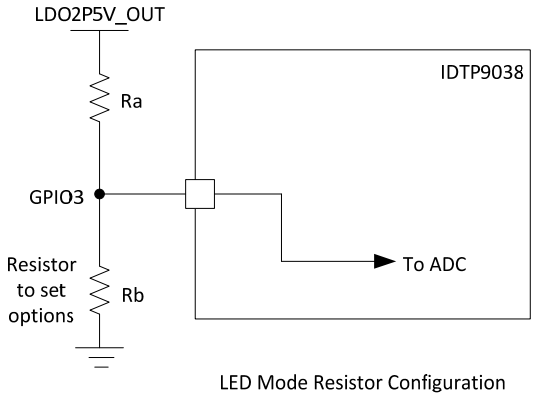


Figure 10. IDTP9038 LED Resistor Options

LED Pattern Operational Status Definitions:

Table 9 – IDTP9038 LED Resistor Optioning (Not all options supported, shaded rows are for future development).

LED Control Option	LED Select Resistor Value	Description	LED #/ Color	Operational Status				FOD Warning
				Standby	Transfer	Complete	Condition	
1	Pull Down	Standby LEDs ON	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
2	R1	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
3	R2	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
4	R3	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
5	R4	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
6	Pull Up	Standby LEDs OFF	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
7	R5	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
8	R6	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
9	R7	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
10	R8	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST

R1-R8 are created using combination of two 1% resistors.

Designates Future Option

Buzzer Function

An optional buzzer feature is supported on GPIO4. The default configuration is an "AC" buzzer. The signal is created by toggling GPIO4 active-high/active-low at a 2kHz frequency.

Buzzer Action: Power Transfer Indication

The IDTP9038 supports audible notification when the device operation successfully reaches the Power Transfer state. The duration of the power transfer indication sound is 400ms.

The latency between reaching the Power Transfer state and sounding the buzzer does not exceed 500ms. Additionally, the buzzer sound is concurrent within

±250ms of any change to the LED configuration indicating the start of power transfer.

Buzzer Action: No Power Transfer Due to Foreign Object Detected (FOD)

Power transfer will fail to initiate or will be terminated for safety reasons when a major FOD situation is detected. Should this event occur, the buzzer will sound in the following repeating sequence:

For 30 seconds: 400ms ON, 800ms OFF, repeat

Next 30 seconds: Off/silence (but no change to LED on/off patterns)

The pattern is repeated while the error condition exists.

The buzzer is synchronized with the FOD LED such that the 400ms ON tone corresponds with the red LED illumination and 800ms OFF (no sound) corresponds with the red LED being off.

Decoupling/Bulk Capacitors

As with any high-performance mixed-signal IC, the IDTP9038 must be isolated from system power supply noise to perform optimally. In general, a decoupling capacitor of 0.1µF must be connected between each power supply and the PCB ground plane as close to these pins as possible. For optimum device performance, the decoupling capacitor must be mounted on the component side of the PCB. The value of the capacitors will decrease due to capacitance-to-applied voltage characteristics of the commonly-used ceramic dielectrics. For example, a 22µF X7R 6.3V capacitor's value can actually be 6µF when operating at 5V, depending on the manufacturer. Typically, 10V- or 16V-rated capacitors are required. The recommended external components are shown in Table 8.

Ceramic capacitors in the 10µF, 44uF, and 1uF range must be used at the REG_IN, IN, and INV5V_IN pins respectively. These power stage input capacitors must be located as physically close as possible to the related power pins and power ground (PGND). Ceramic capacitors are recommended for their low ESR and small profile. Also, ceramic capacitors are inherently more capable than tantalum capacitors and are able to withstand input current surges from low impedance sources such as batteries used in portable devices. Use of ceramic capacitors is important for proper LDO operation because they have been designed to function with very low ESR capacitors. These capacitors must be located as physically close as possible to the related pins (LDO5V, LDO2P5V) and the ICs quiet ground (EP).

ADC Considerations

The GPIO pins can be configured to connect internally to the successive approximation ADC through the ADC's input multiplexer. The ADC has a limited input range, so attention must be paid to the maximum VIN (2.44V). 0.01µF decoupling capacitors to REF_GND can be added to the GPIO inputs to minimize noise.

WPC TX-A5 and A11 Coils

The SW pins connect to a series-resonance circuit comprising a WPC Type-A5 or A11 coil and a series resonant capacitor, as shown in Figure 9. The coil serves as the primary winding in a loosely-coupled transformer, the secondary of which is the coil connected to the power receiver (IDTP9020 or another).

The power transmitter coil is mounted on a ferrite shield per the WPC specification. The coil assembly can be mounted next to the IDTP9038. Either a ground plane or grounded copper shielding can be added beneath the ferrite shield for a reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the IDTP9038 ground plane by a single trace.

Resonance Capacitors

The resonance capacitors must be C0G type dielectric and have a DC rating to 100V. The highest-efficiency combination is four 100nF in parallel to get the lowest ESR. The part numbers are shown in Table 8.

PCB Layout Considerations

For optimum device performance and lowest output phase noise, the following guidelines must be observed. Please contact IDT for Gerber files that contain the recommended board layout.

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths.

All input decoupling capacitors, (eg. the 0.1µF decoupling capacitor on LDO2P5V_IN) must be mounted on the component side of the board as close as possible to the

pins intended to be decoupled. Keep PCB traces to each VDD pin and to ground vias as short as possible.

To optimize board layout, place all components on the same side of the board. Route any unrelated signal traces away from the IDTP9038.

The NDG56 7.0 mm x 7.0 mm x 0.85mm 56L package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.

The package center exposed pad (EP) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EP) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of plated-through-hole (PTH) vias embedded in the PCB center land pad for the NDG56. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board.

On the solder side of the board, these thermal vias embed in a copper fill having the same dimensions as the center land pad on the component side. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.

Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques must then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:

PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces.

In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.

Thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.

Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).

Power Dissipation/Thermal Requirements

The IDTP9038 is offered in a VFQFN-56L package. The maximum power dissipation capability is 1.57W, limited by the die's specified maximum operating junction temperature, T_J, of 125°C. The junction temperature rises with the device power dissipation based on the package thermal resistance. The package offers a typical thermal resistance, junction to ambient (Θ_{JA}), of 25.5°C/W when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout, as well as the placement of the IDTP9038 IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal metric θ_{JA} combines with the characteristics of the PCB itself upon which the VFQFN is mounted. Changing the design or configuration of the PCB impacts the overall thermal resistivity and, thus, the board's heat sinking efficiency.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation must be calculated:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the IDTP9038 device is 125°C. The thermal resistance of the 56-pin NDG package (NDG56) is optimally θ_{JA}=25.5°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is:

$P_{D(Max)}$ = (125°C - 85°C) / 25.5°C/W ≅ 1.57 Watt

Thermal Overload Protection

The IDTP9038 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 140°C. To allow the maximum load current on each regulator and resonant transmitter, and to prevent thermal overload, it is important to ensure that the heat generated by the IDTP9038 is dissipated into the PCB. The package exposed paddle must be soldered to the PCB, with multiple vias evenly distributed under the exposed paddle and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes

NDG VFQFN-56 Package Assembly

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

Packages

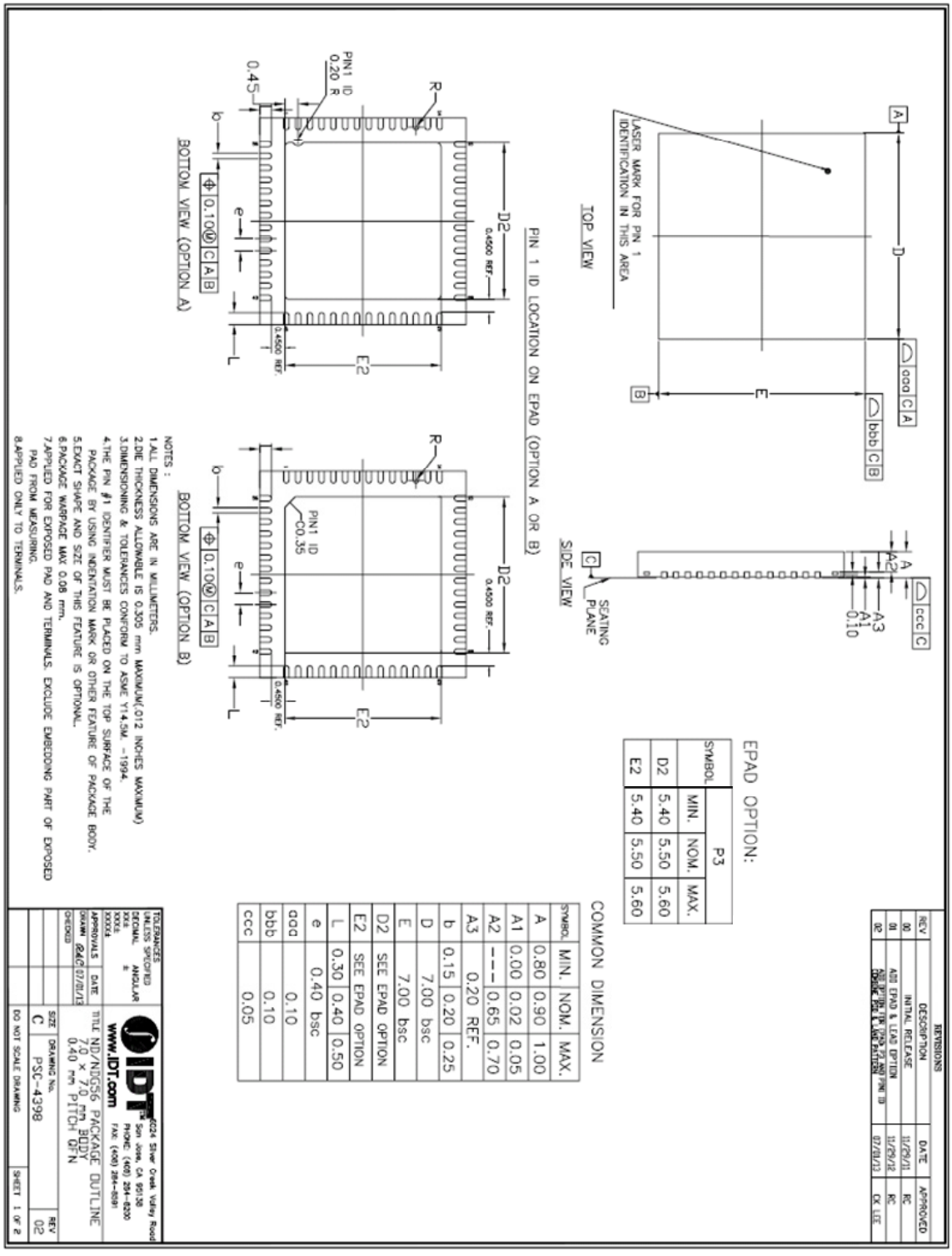


Figure 11. VFQFN-56 7mmx7mm Package Outline Drawing (POD) Page 1

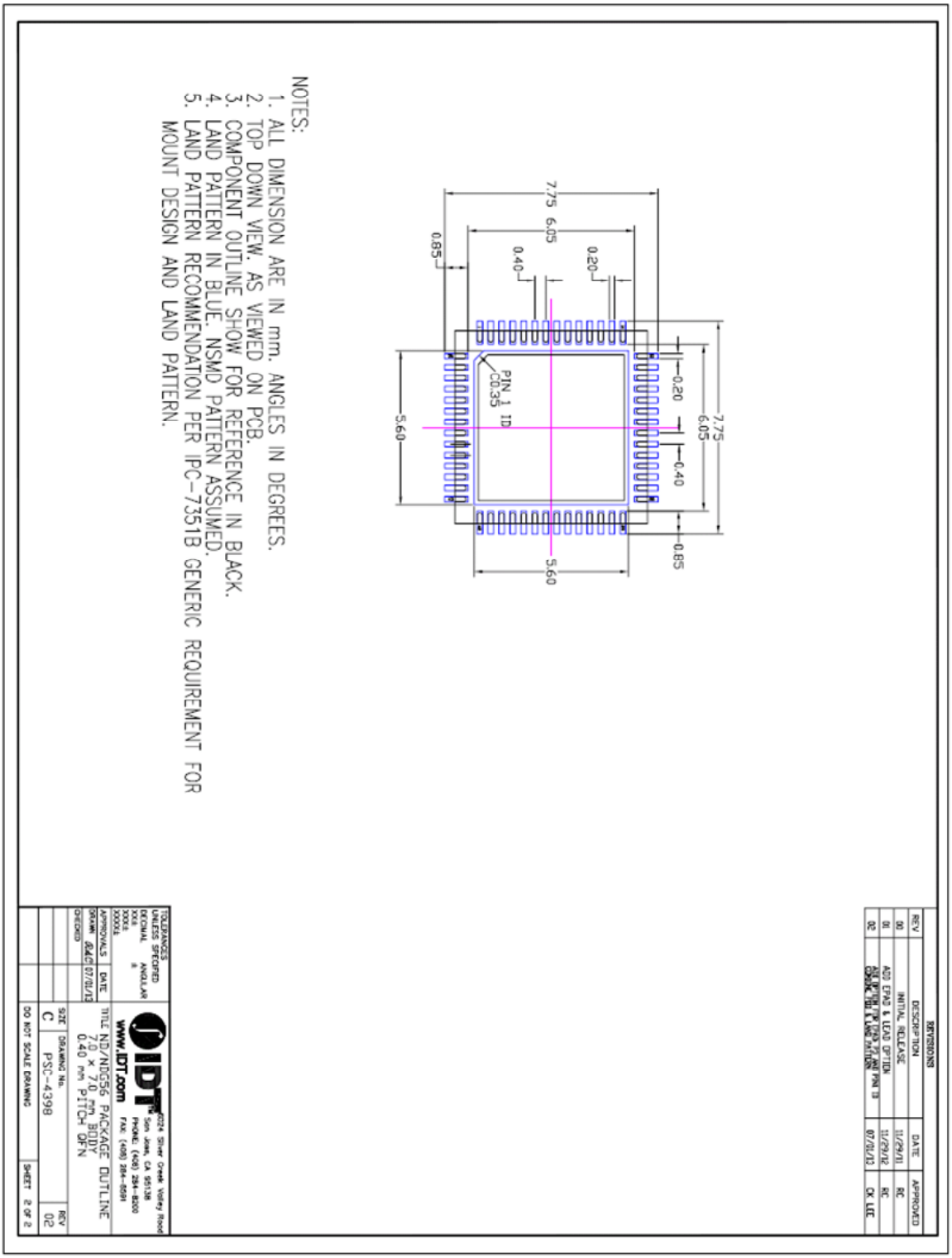


Figure 12. VFQFN-56 7mmx7mm Pacakge Outline Drawing (POD) Page2

ORDERING GUIDE

Table 10. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER
IDTP9038-0NDGI	P9038-0NDGI	NDG56 - VFQFN-56 7x7x0.85	-40°C to +85°C	Tray
IDTP9038-0NDGI8	P9038-0NDGI	NDG56 - VFQFN-56 7x7x0.85	-40°C to +85°C	Tape and reel

