



# HIGH-SPEED CMOS 8-BIT BUFFER/LINE DRIVER

**IDTQS74FCT2244T/AT/CT**

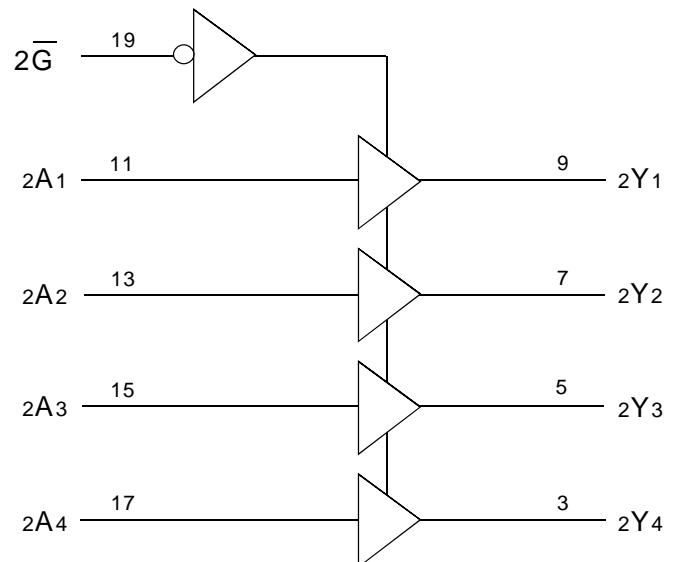
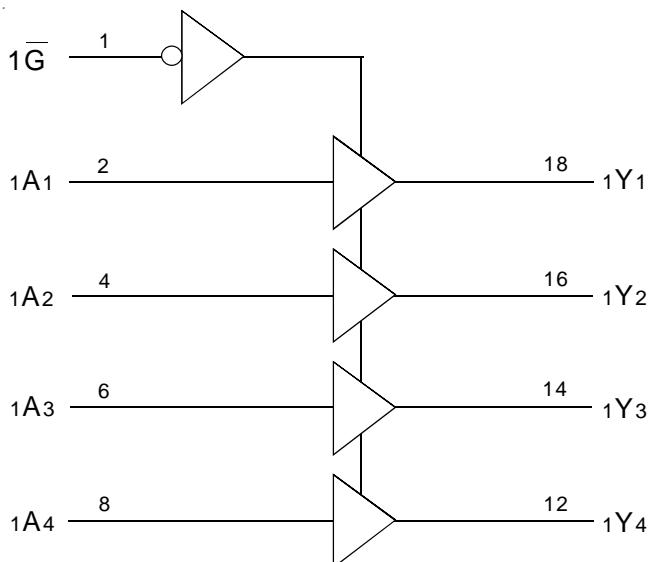
## FEATURES:

- CMOS power levels: <7.5mW static
- Undershoot clamp diodes on all inputs
- True TTL input and output compatibility
- Ground bounce controlled outputs
- Reduced output swing of 0 to 3.5V
- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A, and C speed grades with 4.1ns tPD for C
- IOL = 12mA
- Available in SOIC and QSOP packages

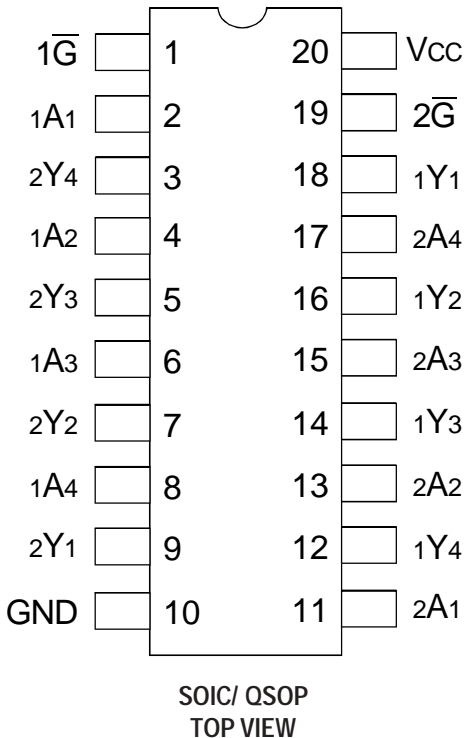
## DESCRIPTION:

The IDTQS74FCT2244T is an 8-bit buffer/line driver with three-state outputs and a 25Ω resistor, ideal for driving transmission lines and reducing system noise. The 2244 series part can replace the 244 series to reduce noise in an existing design. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression. Outputs will not load an active bus when Vcc is removed from the device.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current Max Current Sink/Pin	+120	mA
I <sub>IK</sub>	Input Diode Current, V <sub>IN</sub> < 0	-20	mA
I <sub>OK</sub>	DC Output Current, V <sub>OUT</sub> < 0	-50	mA

### NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4	—	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	—	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
$\overline{1G}$ - $\overline{2G}$	3-State Output Enable Inputs (Active LOW)
xA0 - xA4	Inputs
xY0 - xY4	Outputs

## FUNCTION TABLE<sup>(1)</sup>

Inputs			Outputs
$\overline{1G}$	$\overline{2G}$	xAx	xYx
L	L	L	H
L	L	H	L
H	H	X	Z

### NOTE:

- H = HIGH Voltage Level  
X = Don't Care  
L = LOW Voltage Level  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions		Min.	Typ. <sup>(1)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for all inputs		—	0.2	—	V
$I_{IH}$	Input HIGH Current	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{IL}$	Input LOW Current						
$I_{OZ}$	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}$	$0 \leq V_{IN} \leq V_{CC}$	—	—	$\pm 5$	$\mu\text{A}$
$I_{OR}$	Current Drive	$V_{CC} = \text{Max.}, V_{OUT} = 2V^{(2)}$		50	—	—	mA
$V_{IC}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^{\circ}\text{C}^{(2)}$		—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$	$I_{OH} = -15\text{mA}$	2.4	—	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	—	—	0.5	V
$R_{OUT}$	Output Resistance	$V_{CC} = \text{Min.}$	$I_{OL} = 12\text{mA}$	20	28	40	$\Omega$

### NOTES:

- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
- This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $\text{freq} = 0$ $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC} - 0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
$\Delta I_{CC}$	Supply Current per Input TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4\text{V}^{(2)}$ $\text{freq} = 0$	—	2	mA
$I_{CCD}$	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$ Outputs Open and Enabled One Bit Toggling 50% Duty Cycle Other inputs at GND or $V_{CC}^{(3,4)}$	—	0.25	mA/ MHz

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under DC Electrical Characteristics.
- Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
- For flip-flops,  $I_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance.

$$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4\text{V}$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_T$  = Number of TTL Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current caused by an Output Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Output Frequency

$N_i$  = Number of Outputs at  $f_i$

All currents are in milliamps and all frequencies are in megahertz.

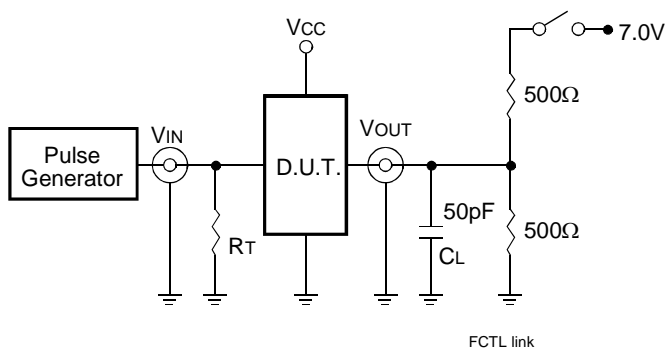
SWITCHING CHARACTERISTICS OVER OPERATING RANGE<sup>(1)</sup>

Symbol	Parameter <sup>(2)</sup>	74FCT2244T		74FCT2244AT		74FCT2244CT		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>PLH</sub>	Propagation Delay	1.5	6.5	1.5	4.8	1.5	4.1	ns
t <sub>PHL</sub>	xAx to xYx							
t <sub>PZH</sub>	Output Enable Time	1.5	8	1.5	6.2	1.5	5.8	ns
t <sub>PZL</sub>	$\overline{xG}$ to xYx							
t <sub>PHZ</sub>	Output Disable Time <sup>(3)</sup>	1.5	7	1.5	5.6	1.5	5.2	ns
t <sub>PLZ</sub>	$\overline{xG}$ to xYx							

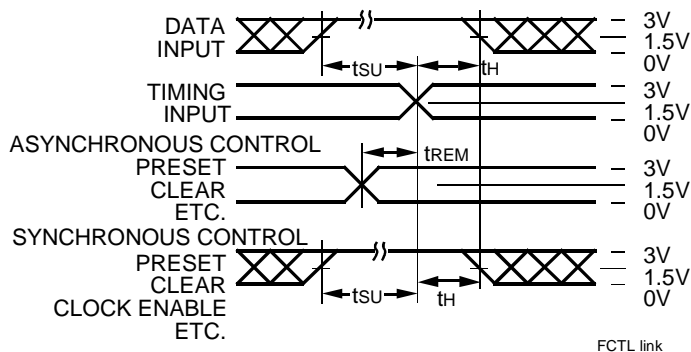
NOTES:

1. C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.
2. Minimums guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.

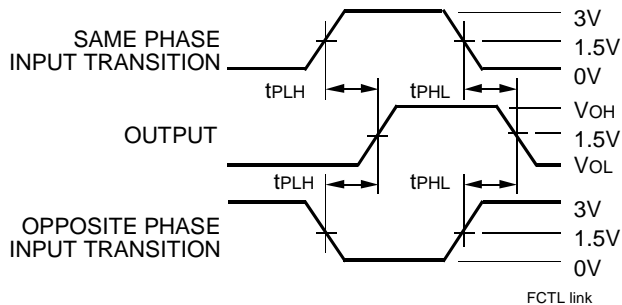
## TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



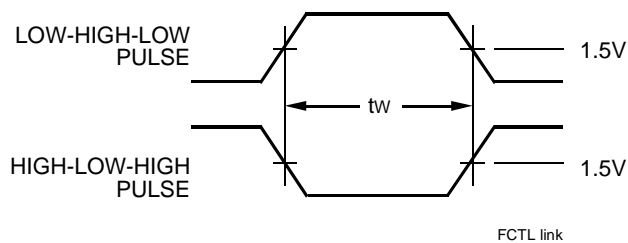
Propagation Delay

## SWITCH POSITION

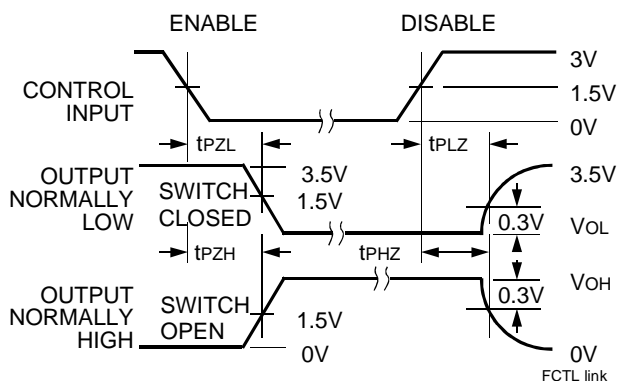
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

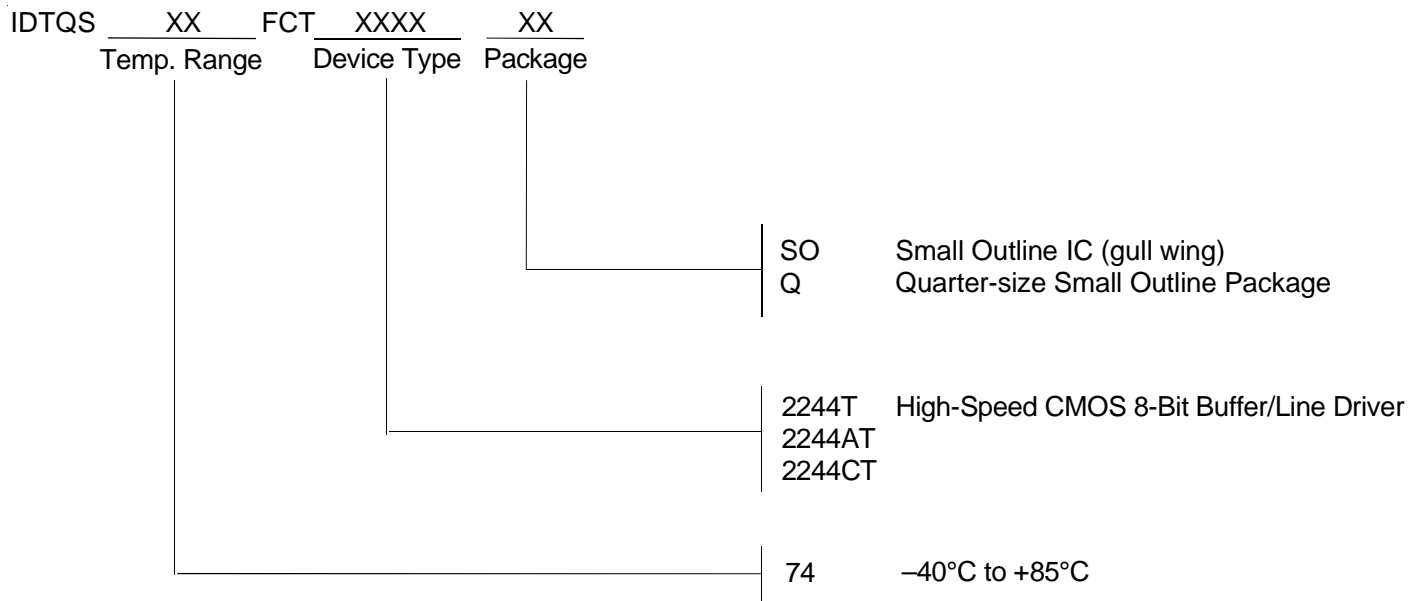


Enable and Disable Times

### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



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