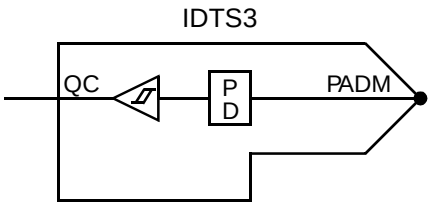
Description

IDTS3 is a non-inverting, TTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDTS3 inst_IDTS3 (QC, PADM);

VHDL..... inst_IDTS3 : IDTS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	15.8	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.99 1.72	1.03 1.89	1.11 2.02	1.20 2.12	1.33 2.21

Delay will vary with input conditions. See page 2-17 for interconnect estimates.