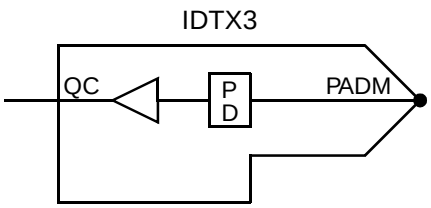
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

IDTX3 is a non-inverting, TTL-level, input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDTX3 *inst_name (*QC, PADM);

VHDL..... *inst_name*: IDTX3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	10.4	Eq-load

See page 2-15 for power equation.

Input Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.53 0.72	0.67 0.87	0.78 0.99	0.89 1.10	1.00 1.22

Delay will vary with input conditions. See page 2-17 for interconnect estimates.