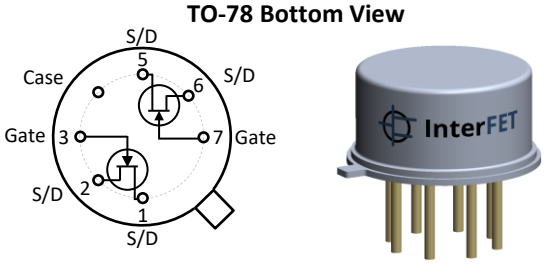
IF3602 Dual Matched N-Channel JFET

Features

- InterFET N3600L Geometry
- Low noise: 0.35 nV/√Hz typical
- High gain: 175mS typical
- Low $V_{GS(OFF)}$: -1.5 typical
- Typical I_{DSS}: 300mA
- Typical BV_{GSS}: -30V
- High radiation tolerance
- RoHS, REACH, CMR compliant
- Custom test and binning options available
- SMT, TH, and bare die package options
- Edge case SPICE modeling: InterFET SPICE

TO-78 Bottom View



NOTE: S/D pins are interchangeable Source Drain connections

Industry Standard Crosses

- InterFET exclusive

InterFET Similar Parts

- IF3601

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone Preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The -20V InterFET IF3602 JFET is presently the lowest noise JFET on the market. Targeted for ultra low noise high gain differential amplifier designs the IF3602 is the default standard for ultra low noise measurement equipment at very low frequencies. Custom specifications, matching, and packaging options are available.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF3602T78	Through-Hole	TO-78	Bulk
IF3602COT *	Chip Orientated Tray (COT Waffle Pack)	COT	30/Waffle Pack
IF3602CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	30/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		TO-78	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation[1]	500	mW
P	Power Derating[1]	3.3	mW/°C
T_J	Operating Junction Temperature	-65 to 175	°C
T_{STG}	Storage Temperature	-65 to 175	°C

[1] Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

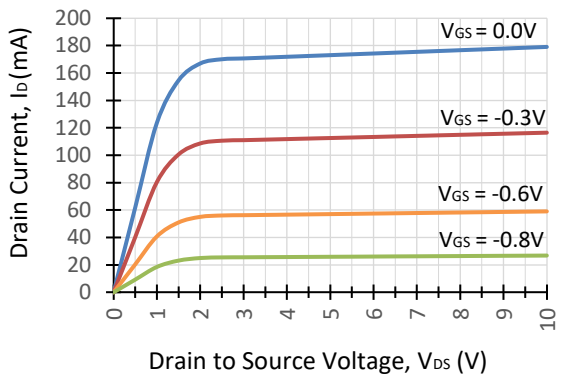
Parameters		Conditions	Min	Typ	Max	Unit
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-20			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -10V, V_{DS} = 0V			-0.5	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 0.5nA	-0.35		-3.0	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 10V (Pulsed)	30	300		mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

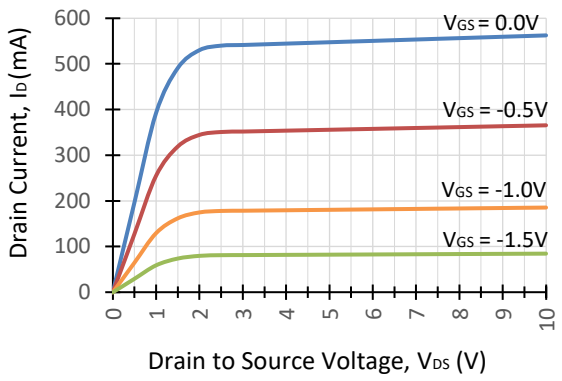
Parameters		Conditions	Min	Typ	Max	Unit
G_{FS}	Forward Transconductance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz		175		mS
C_{iss}	Input Capacitance	V_{DS} = 0V, V_{GS} = -4V, f = 1MHz		650		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 0V, V_{GS} = -4V, f = 1MHz		80		pF
e_n	Equivalent Circuit Input Noise Voltage	V_{DS} = 3V, I_D = 5mA, f = 100Hz		0.35		nV/√Hz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 500pA			100	mV

Typical IF3602 Characteristics

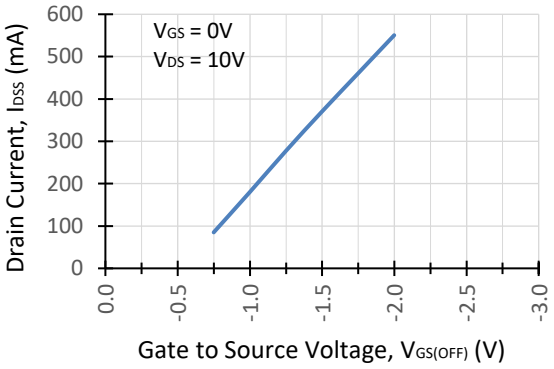
Typical Output @ $V_{GS(OFF)}$ = -1.0V



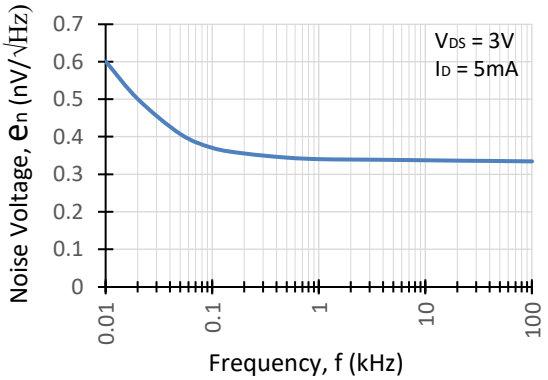
Typical Output @ $V_{GS(OFF)}$ = -2.0V



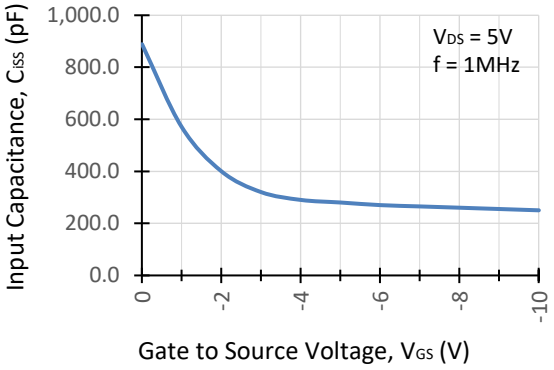
Typical I_{DSS} - $V_{GS(OFF)}$



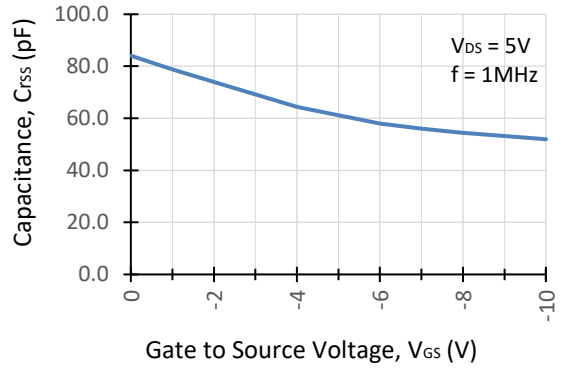
Typical Noise (nV/√Hz)



Typical C_{iss} - V_{GS}

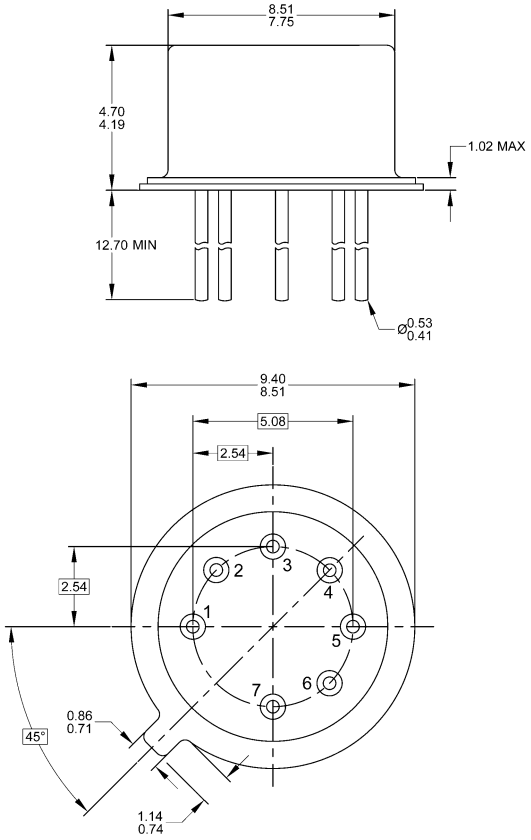


Typical C_{rss} - V_{GS}



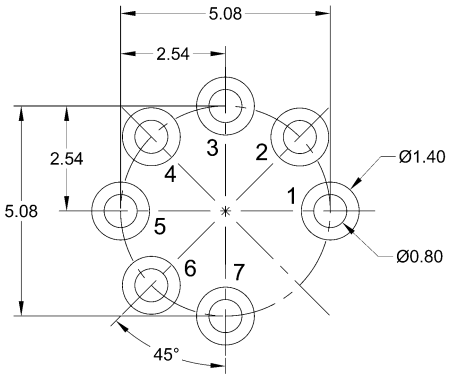
TO-78 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 7.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.

Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.InterFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 – 0.2%	0.05 – 0.2%	0.05 – 0.15%	
P	0.015 – 0.15%	0.015 – 0.15%	0.015 – 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
C				<0.01%
Au				Plating

Package tests

Parameters	SOT23	SOIC8	TO-92	Metal Case
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM	Class M4 Machine Model Class 3B HBM

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