IF389A, IF389B, IF389C, IF389D Dual Matched N-Channel JFET

Features

- InterFET N0132 Geometry
- Low Noise: 1.0 nV/√Hz Typical
- High Gain: 24mS Typical
- Low Cutoff Voltage: 2.0V Maximum
- Thermally Optimized SOIC8 Package
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

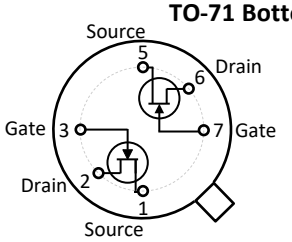
Applications

- Differential Audio Amplifiers
- Low Noise High Gain Amplifier
- Instrumentation Amplifiers
- Acoustic and Vibration Sensors
- Replacement Parts for 2SK389 and LSK389x

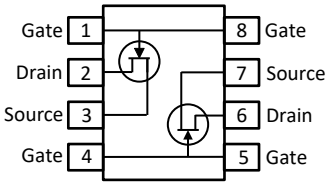
Description

The -30V InterFET IF389x matched pair JFET is targeted for low noise high gain differential amplifier designs. The TO-71 package is hermetically sealed and suitable for military uses. Higher breakdown voltage parts are available through InterFET custom ordering. The IF170x is a single part option.

TO-71 Bottom View



SOIC8 Top View



Note: The SOIC8 package is pinned out differently than the LSK389x part to optimize thermal performance. Package and pinout variations are available through InterFET custom ordering.

Product Summary

Parameters	IF389A Min	IF389B Min	IF389C Min	IF389D Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	-30	-30	-30	-30	V
I_{DSS} Drain to Source Saturation Current	2.6	6.0	10.0	18.0	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.2	-0.2	-0.2	-0.2	V
G_{FS} Full Forward Transconductance	15 (Typ)	20 (Typ)	24 (Typ)	28 (Typ)	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF389AT71, IF389BT71, IF389CT71, IF389DT71	Through-Hole	TO-71	Bulk
IF389AS08, IF389BS08, IF389CS08, IF389DS08	Surface Mount	SOIC8	Bulk
IF389AS08TR, IF389BS08TR, IF389CS08TR, IF389DS08TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IF389ACOT, IF389BCOT, IF389CCOT, IF389DCOT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IF389ACFT, IF389BCFT, IF389CCFT, IF389DCFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-30	V
I_{FG}	Continuous Forward Gate Current	10	mA
P_D	Continuous Device Power Dissipation	300	mW
P	Power Derating	1.8	mW/°C
T_J	Operating Junction Temperature	-55 to 135	°C
T_{STG}	Storage Temperature	-65 to 200	°C

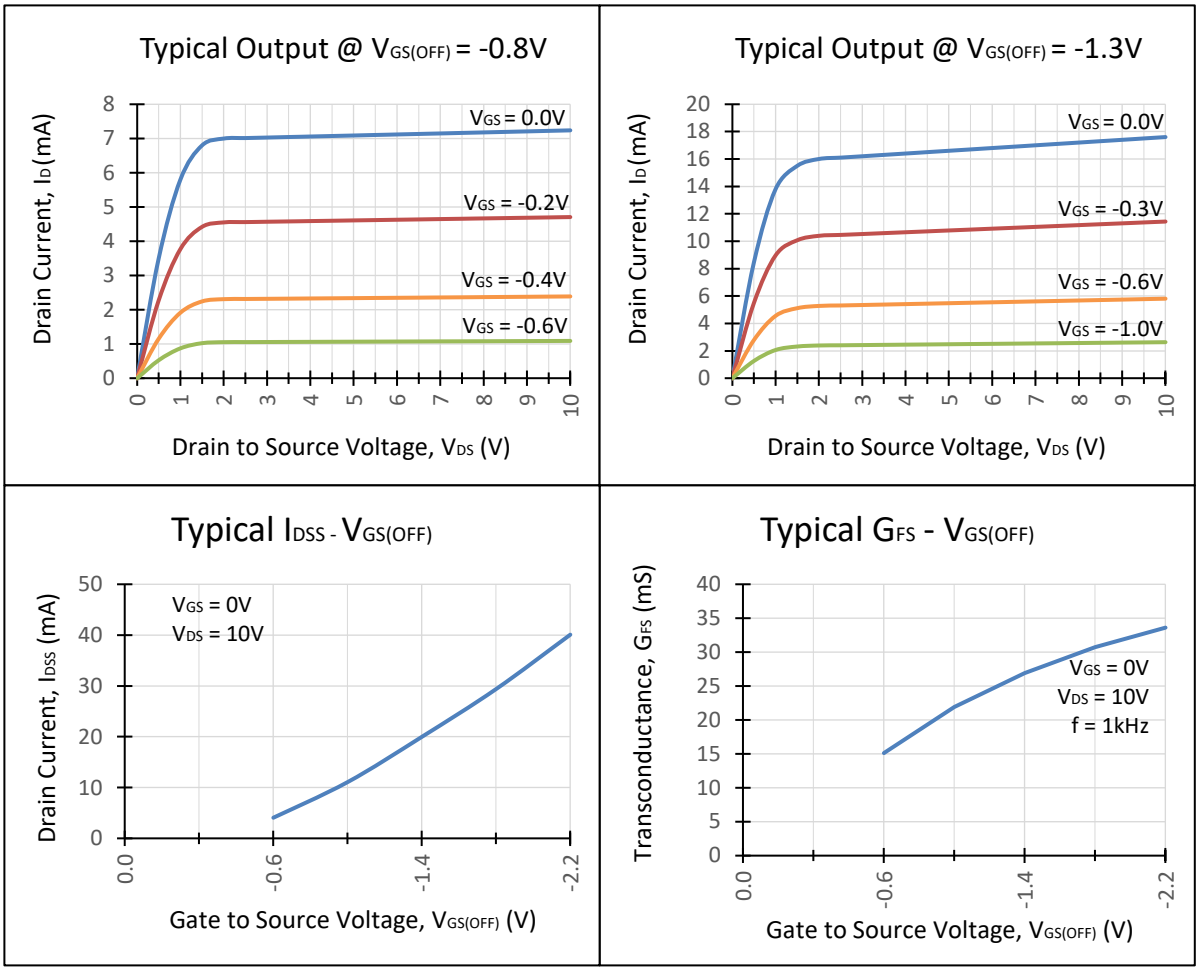
Static Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions		Min	Max	Units
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	I_G = -1µA, V_{DS} = 0V		-30		V
I_{GSS}	Gate to Source Reverse Current	V_{DS} = 0V, V_{GS} = -10V			-0.1	nA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 10V, I_D = 1nA		-0.2	-2.0	V
I_{DSS}	Drain to Source Saturation Current	V_{DS} = 10V, V_{GS} = 0V (Pulsed)	IF389A IF389B IF389C IF389D	2.6 6.0 10.0 18.0	6.5 12.0 20.0 30.0	mA

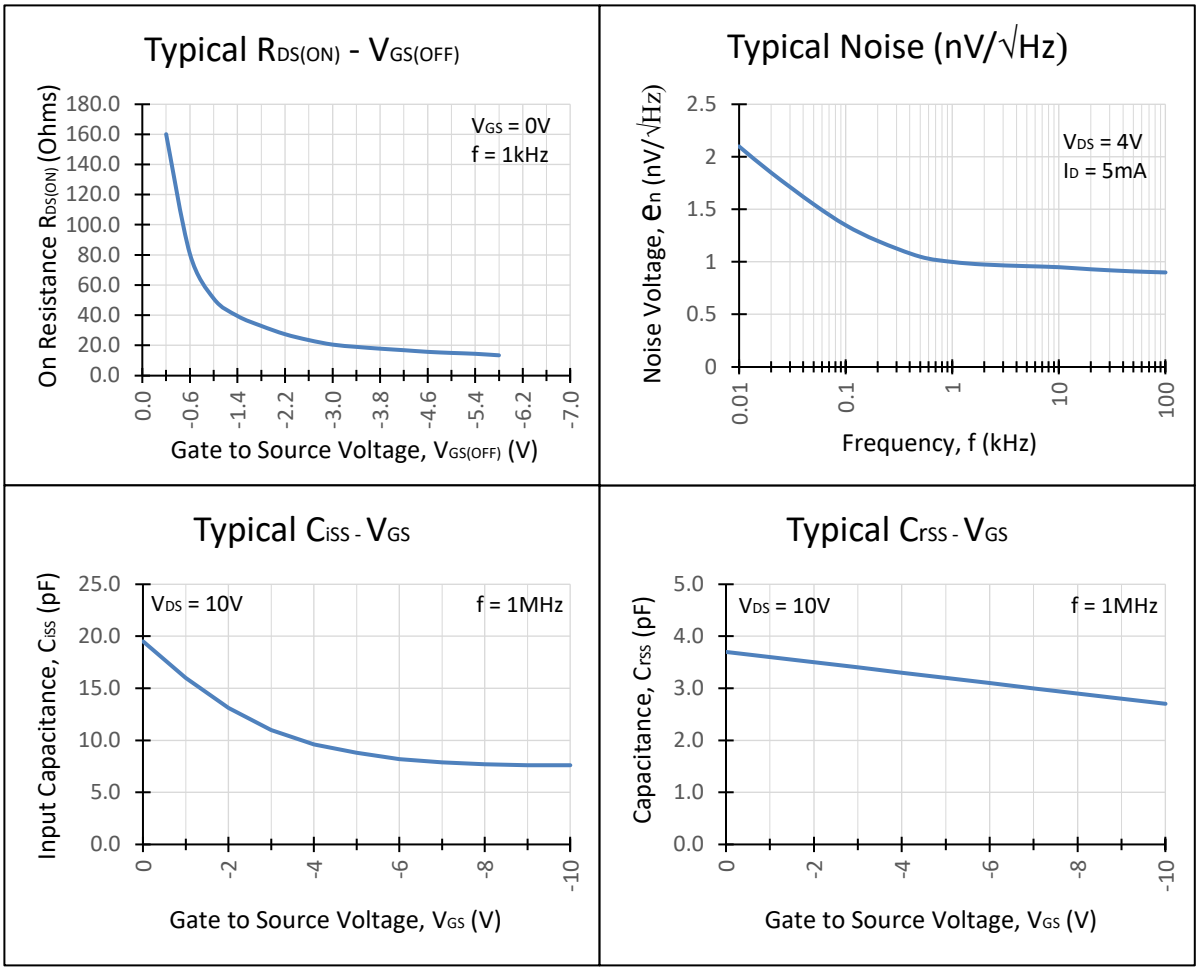
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

Parameters		Conditions	Min	Max	Units
G_{FS}	Full Forward Transconductance	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz	14		mS
$G_{FS(TYP)}$	Typical Transconductance	V_{DS} = 15V, I_D = 1mA	6		mS
C_{iss}	Input Capacitance	V_{DS} = 10V, I_D = 2mA, f = 1MHz		20	pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 10V, I_D = 2mA, f = 1MHz		4.5	pF
e_n	Noise Voltage	V_{DS} = 10V, I_D = 2mA, f = 1kHz	1.0 (Typical)		nV/√Hz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate Source Voltage	V_{DS} = 10V, I_D = 1mA		30	mV

Typical IF389x Characteristics

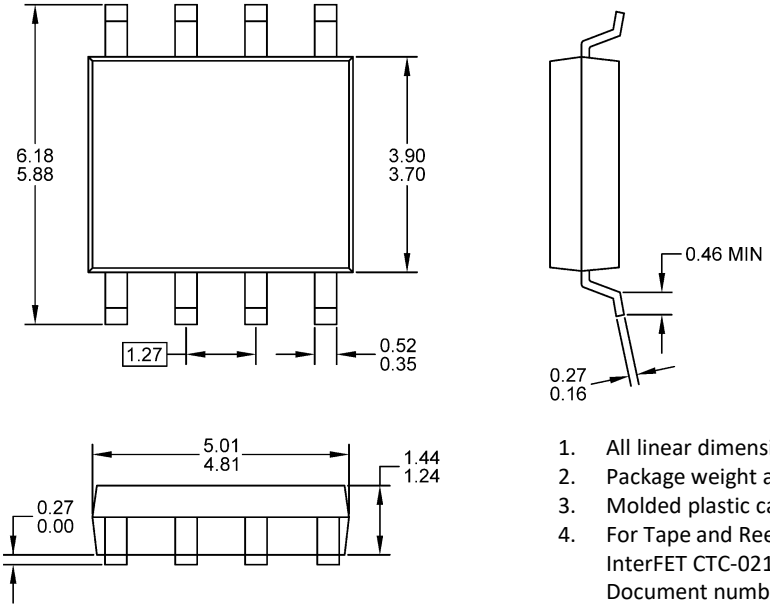


Typical IF389x Characteristics (Continued)



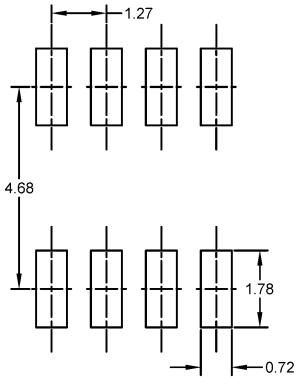
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

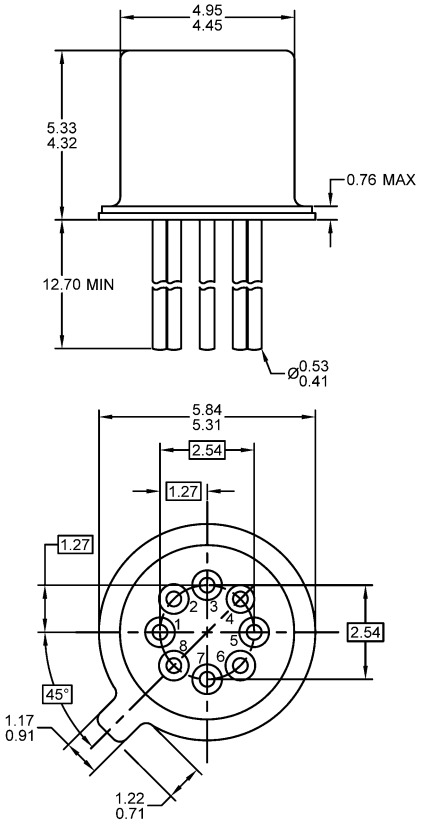
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

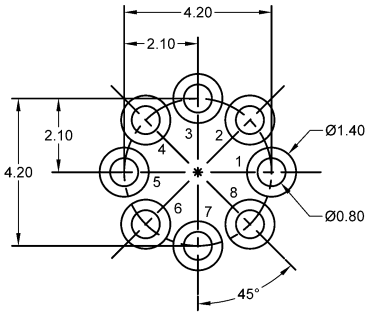
TO-71 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.35 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Bent Lead Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.