







IF4520 N-Channel JFET

Features

- InterFET N0450S Geometry
- Low Noise: 1.0 nV/VHz Typical
- Replacement for SNJ450113
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

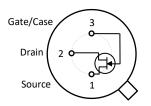
Applications

- · Low R(ON) Switch
- · Low-Noise, High Gain Amplifier

Description

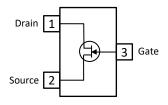
The -40V InterFET IF4520 is a higher voltage version of the low noise high gain IF4500 JFET. The TO-72 package is hermetically sealed and suitable for military applications.

TO-18 Bottom View





SOT23 Top View





Product Summary

	Parameters	IF4520 Min	Unit	
BV _{GSS}	Gate to Source Breakdown Voltage	-40	V	
I _{DSS}	Drain to Source Saturation Current	8	mA	
V _{GS(off)}	Gate to Source Cutoff Voltage	-0.3	V	
GFS	Forward Transconductance	20 (Typ)	mS	

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
IF4520T18	Through-Hole	TO-18	Bulk
IF4520ST3	Surface Mount	SOT23	Bulk
	7" Tape and Reel: Max 3,000 Pieces		Minimum 1,000 Pieces
IF4520ST3TR	13" Tape and Reel: Max 9,000 Pieces	SOT23	Tape and Reel
IF4520COT	Chip Orientated Tray (COT Waffle Pack)	СОТ	400/Waffle Pack
IF4520CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.









Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I _{FG}	Continuous Forward Gate Current	10	mA
PD	Continuous Device Power Dissipation	300	mW
Р	Power Derating	2.8	mW/°C
TJ	Operating Junction Temperature	-55 to 150	°C
T _{STG}	Storage Temperature	-65 to 175	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			IF4520			
	Parameters	Conditions	Min	Тур	Max	Unit
V _{(BR)GSS}	Gate to Source Breakdown Voltage	V _{DS} = 0V, I _G = -1μA	-40	-45		V
I _{GSS}	Gate to Source Reverse Current	V _{GS} = -10V, V _{DS} = 0V		-50	-1000	рА
V _{GS(OFF)}	Gate to Source Cutoff Voltage	V _{DS} = 10V, I _D = 1nA	-0.3			V
I _{DSS}	Drain to Source Saturation Current	$V_{GS} = 0V$, $V_{DS} = 15V$ (Pulsed)	8		20	mA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

			IF4520			
	Parameters	Conditions	Min	Тур	Max	Unit
G _{FS}	Forward Transconductance	V _{DS} = 15V, V _{GS} = 0V, f = 1kHz		20	30	mS
Ciss	Input Capacitance	V _{DS} = 0V, V _{GS} = -10V, f = 1MHz			75	pF
Crss	Reverse Transfer Capacitance	V _{DS} = 0V, V _{GS} = -10V, f = 1MHz		15		pF



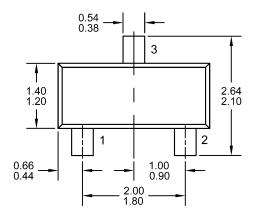


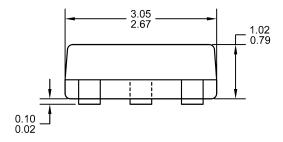


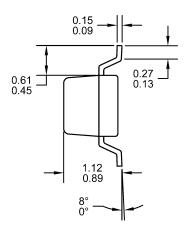


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

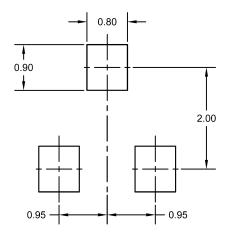






- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.12 grams
- 3. Molded plastic case UL 94V-0 rated
- For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



- 1. All linear dimensions are in millimeters.
- 2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.



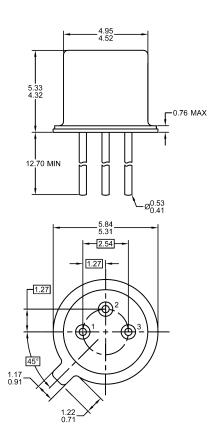






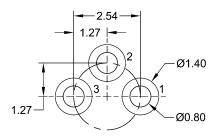
TO-18 Mechanical and Layout Data

Package Outline Data



- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.29 grams
- 3. Bulk product is shipped in standard ESD shipping material
- 4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



- 1. All linear dimensions are in millimeters.
- The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.