

IFN424, IFN425, IFN426 Dual Matched N-Channel JFET

Features

- InterFET [N0001H Geometry](#)
- Low Leakage: 0.25 pA Typical
- Low Input Capacitance: 2.0 pF Typical
- High Input Impedance
- Replacement for U424, U425, U426
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

- Low Leakage Input Buffer
- High Frequency Amplifier/Buffer
- Ultrahigh Impedance Pre-Amplifier
- Impedance Converters

Description

The -40V InterFET IFNU424, IFNU425, and IFNU426 JFET's are targeted for ultra high input impedance applications for differential amplification and impedance matching. Gate leakages are less than 1pA at room temperatures. The TO-78 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.

Product Summary

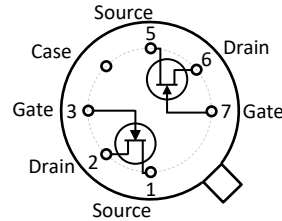
Parameters	IFN424 Min	IFN425 Min	IFN426 Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	-40	-40	-40	V
I_{DSS} Drain to Source Saturation Current	60	60	60	μA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	-0.4	-0.4	-0.4	V
G_{FS} Forward Transconductance	300	300	300	μS

Ordering Information Custom Part and Binning Options Available

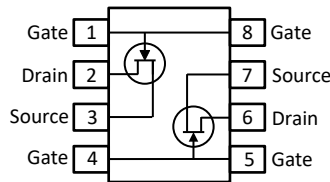
Part Number	Description	Case	Packaging
IFNU424; IFNU425; IFNU426	Through-Hole	TO-78	Bulk
SMP424; SMP425; SMP426;	Through-Hole	SOIC8	Bulk
SMP424TR; SMP425TR; SMP426TR	7" Tape and Reel: Max 500 Pieces 13" Tape and Reel: Max 2,500 Pieces	SOIC8	Minimum 500 Pieces Tape and Reel
IFNU424COT; IFNU425COT; IFNU426COT *	Chip Orientated Tray (COT Waffle Pack)	COT	70/Waffle Pack
IFNU424CFT; IFNU425CFT; IFNU426CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack

* Bare die packaged options are designed for matched specifications but not 100% tested

TO-78 Bottom View



SOIC8 Top View



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG} Continuous Forward Gate Current	50	mA
P_D Continuous Device Power Dissipation	400	mW
P Power Derating	3.2	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 150	$^\circ\text{C}$
T_{STG} Storage Temperature	-60 to 200	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

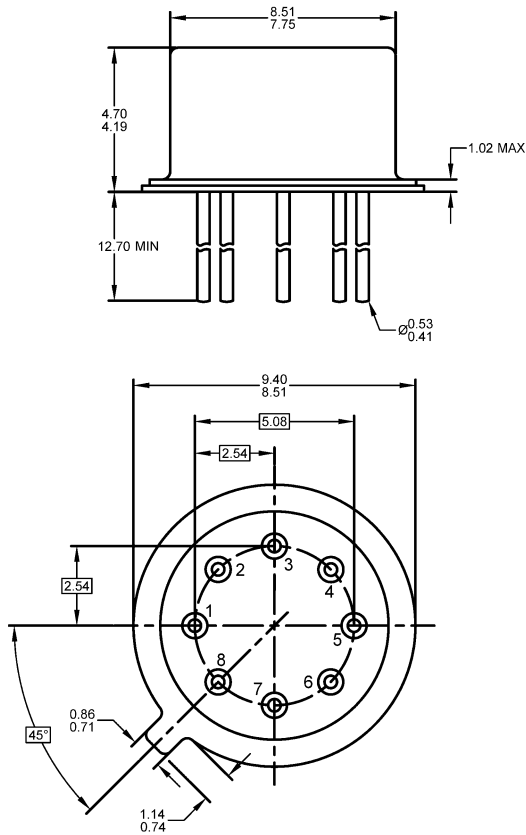
Parameters	Conditions	IFN424, IFN425, IFN426			Unit
		Min	Typ	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$	-40	-60		V
BV_{G1G2} Gate to Gate Breakdown Voltage	$I_G = -1\mu\text{A}, I_D = 0\text{A}, I_S = 0\text{A}$	± 40			V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}, T_A = 25^\circ\text{C}$			-3	pA
	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}, T_A = 125^\circ\text{C}$			-3	nA
I_G Gate Operating Current	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}, T_A = 25^\circ\text{C}$			-0.5	pA
	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}, T_A = 125^\circ\text{C}$			-500	pA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = 10\text{V}, I_D = 1\text{nA}$	-0.4		-3	V
V_{GS} Gate Source Voltage	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}$			-2.9	V
I_{DSS} Drain to Source Saturation Current	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$ (Pulsed)	60	1800		μA

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	IFN424, IFN425, IFN426			Unit
		Min	Typ	Max	
G_{FS} Forward Transconductance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{kHz}$	300		1500	μS
G_{OS} Output Conductance	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}, f = 1\text{kHz}$			3	μS
C_{iss} Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$			3	pF
C_{rss} Reverse Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$			1.5	pF
e_n Equivalent Circuit Input Noise Voltage	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}, f = 10\text{Hz}$		20	70	$\text{nV}/\sqrt{\text{Hz}}$
NF Noise Figure	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}, f = 10\text{Hz}, R_G = 1\text{M}\Omega$			1	dB
$ V_{GS1} - V_{GS2} $ Differential Gate Source Voltage	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}$	IFN424		10	mV
		IFN425		15	
		IFN426		25	
$\frac{ V_{GS1} - V_{GS2} }{\Delta T}$ Differential Gate Source Voltage with Temperature	$V_{DS} = 10\text{V}, I_D = 30\mu\text{A}$ $T_A = -55^\circ\text{C}, T_B = 25^\circ\text{C}, T_C = 125^\circ\text{C}$	IFN424		1	mV/ $^\circ\text{C}$
		IFN425		2.5	
		IFN426		5	
CMRR Common Mode Rejection Ratio	$V_{DD} = 10\text{V to } 20\text{V}, I_D = 30\mu\text{A}$	IFN424	90		dB
		IFN425	80		
		IFN426	80		

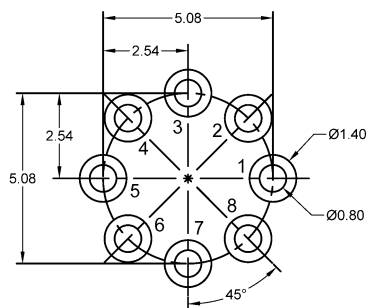
TO-78 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Eight leaded device. Not all leads are shown in drawing views.
3. Some package configurations will not populate pin 8 and/or pin 4.
4. Package weight approximately 0.44 grams
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

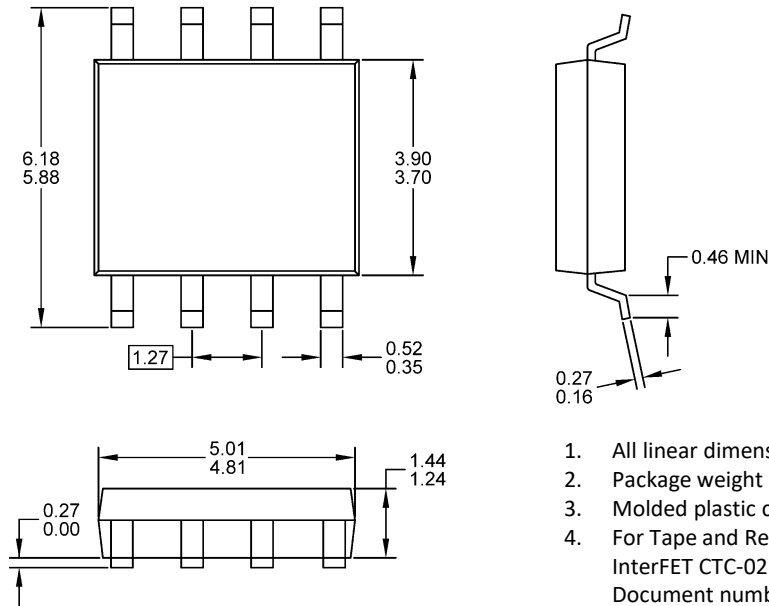
Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. Pads 8 and/or pad 4 can be eliminated for devices with less pins.
3. The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.

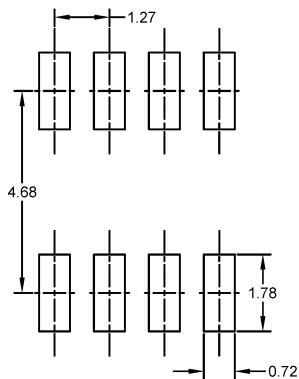
SOIC8 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.21 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.