







## IFNU234, IFNU235 Dual Matched N-Channel JFET

#### **Features**

InterFET <u>N0016H Geometry</u>

· Low Leakage: 10 pA Typical

· Low Input Capacitance: 3.5 pF Typical

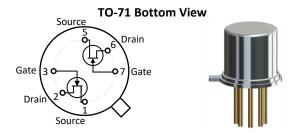
- · High Input Impedance
- Replacement for U234, U235
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

#### **Applications**

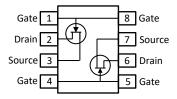
- · Low Noise Differential Amplifier
- · Differential Amplifier
- · Wide-Band Amplifier

#### Description

The -50V InterFET IFNU234, and IFNU235 JFET's are targeted for low noise differential amplifier designs. Gate leakages are less than 10pA at room temperatures. The TO-71 package is hermetically sealed and suitable for military applications. Custom specifications, matching, and packaging options are available.



### **SOIC8 Top View**





#### **Product Summary**

	Parameters	IFNU234 Min	IFNU235 Min	Unit
$BV_GSS$	Gate to Source Breakdown Voltage	-50	-50	V
I <sub>DSS</sub>	Drain to Source Saturation Current	0.5	0.5	mA
V <sub>GS(off)</sub>	Gate to Source Cutoff Voltage	-0.5	-0.5	V
G <sub>FS</sub>	Forward Transconductance	0.6	0.6	mS

#### Ordering Information Custom Part and Binning Options Available

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Part Number	Description	Case	Packaging		
IFNU234; IFNU235	Through-Hole	TO-71	Bulk		
SMPU234; SMPU235	Surface Mount	SOIC8	Bulk		
	7" Tape and Reel: Max 500 Pieces		Minimum 500 Pieces		
SMPU234TR; SMPU235TR	13" Tape and Reel: Max 2,500 Pieces	SOIC8	Tape and Reel		
IFNU234COT; IFNU235COT *	Chip Orientated Tray (COT Waffle Pack)	СОТ	70/Waffle Pack		
IFNU234CFT; IFNU235CFT *	Chip Face-up Tray (CFT Waffle Pack)	CFT	70/Waffle Pack		

<sup>\*</sup> Bare die packaged options are designed for matched specifications but not 100% tested



**Disclaimer:** It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.









### **Electrical Characteristics**

Maximum Ratings (@ T<sub>A</sub> = 25°C, Unless otherwise specified)

	Parameters	Value	Unit
$V_{RGS}$	Reverse Gate Source and Gate Drain Voltage	-50	V
I <sub>FG</sub>	Continuous Forward Gate Current	50	mA
PD	Continuous Device Power Dissipation	300	mW
Р	Power Derating	4.3	mW/°C
TJ	Operating Junction Temperature	-55 to 125	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			IFNU234, IFNU235		
	Parameters	Conditions	Min	Max	Unit
V <sub>(BR)GSS</sub>	Gate to Source Breakdown Voltage	$V_{DS} = 0V$ , $I_{G} = -1\mu A$	-50		V
I <sub>GSS</sub>	Gate to Source Reverse Current	$V_{GS} = -30V$ , $V_{DS} = 0V$ , $T_A = 25$ °C $V_{GS} = -30V$ , $V_{DS} = 0V$ , $T_A = 150$ °C		-100 -500	pA nA
V <sub>GS(OFF)</sub>	Gate to Source Cutoff Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 1nA	-0.5	-4.5	V
V <sub>GS</sub>	Gate to Source Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA	-0.3	-4	V
I <sub>DSS</sub>	Drain to Source Saturation Current	$V_{DS} = 20V$ , $V_{GS} = 0V$ (Pulsed)	0.5		5
IG	Gate Current	$V_{DS} = 20V$ , $I_D = 200\mu A$ , $T_A = 25^{\circ}C$ $V_{DS} = 20V$ , $I_D = 200\mu A$ , $T_A = 125^{\circ}C$		-50 -250	pA nA

**Dynamic Characteristics** (@ TA = 25°C, Unless otherwise specified)

				IFNU234, IFNU235		
	Parameters	Conditions		Min	Max	Unit
G <sub>FS</sub>	Forward Transconductance	$V_{DS} = 20V$ , $I_{D} = 200\mu A$ ,	f = 1kHz	0.6	1.6	mS
Gos	Output Conductance	$V_{DS} = 20V$ , $I_{D} = 200\mu A$ ,	f = 1kHz		10	μS
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f :	= 1MHz		6	рF
Crss	Reverse Transfer Capacitance	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V, f =	= 1MHz		2	рF
e <sub>n</sub>	Equivalent Circuit Input Noise Voltage	$V_{DS} = 20V, V_{GS} = 0V, f = 0$	= 100Hz		80	nV/√Hz
$ V_{GS1} - V_{GS} $	Differential Gate Source Voltage	V <sub>DS</sub> = 20V, I <sub>D</sub> = 200μA	IFNU234 IFNU235		0 5	mV
V <sub>GS1</sub> -V <sub>GS2</sub>	Differential Gate	$V_{DS} = 20V$ , $I_D = 200\mu A$ , $T_A = -55^{\circ}C$ , $T_B = 25^{\circ}C$ , $T_C = 125^{\circ}C$	IFNU234 IFNU235		5	mV/°C



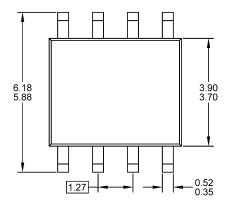


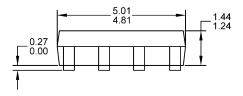


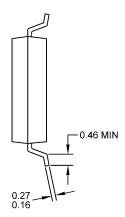


## **SOIC8 Mechanical and Layout Data**

### **Package Outline Data**

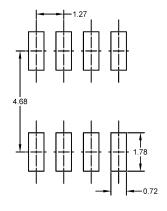






- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.21 grams
- 3. Molded plastic case UL 94V-0 rated
- For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

# **Suggested Pad Layout**



- 1. All linear dimensions are in millimeters.
- 2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.



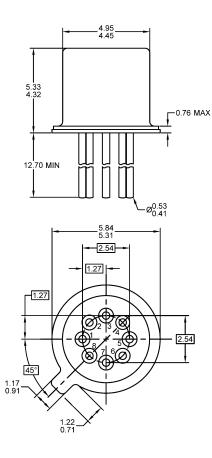






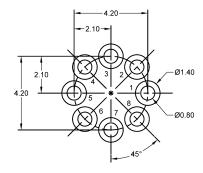
## **TO-71 Mechanical and Layout Data**

### **Package Outline Data**



- 1. All linear dimensions are in millimeters.
- Eight leaded device. Not all leads are shown in drawing views.
- 3. Some package configurations will not populate pin 8 and/or pin 4.
- 4. Package weight approximately 0.35 grams
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

## **Suggested Bent Lead Through-Hole Layout**



- 1. All linear dimensions are in millimeters.
- Pads 8 and/or pad 4 can be eliminated for devices with less pins.
- The suggested land pattern dimensions have been provided as an eight pin bent lead reference only. A more robust pattern may be desired for wave soldering or reduced pin count.