Never stop thinking

IFX9201SG

6 A H-Bridge with SPI

Data Sheet

Rev. 1.1, 2015-02-15

Automotive Power

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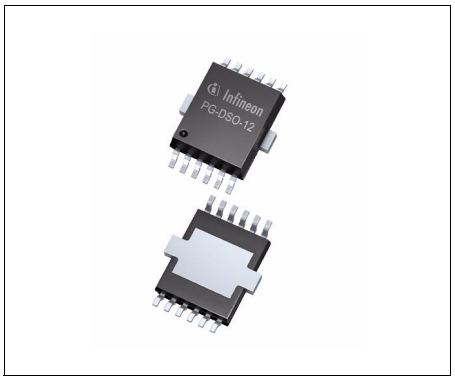
1 Overview



PG-DSO-12-17

Features

- R_{DSon} of 100 mΩ per switch typ. at Tj=25 °C
- Logic inputs 3.3 V and 5.0 V TTL/CMOS-compatible
- Low standby current
- Chopper current limitation
- Short circuit shut down with latch behavior
- Overtemperature shut down with latch behavior
- VS undervoltage shutdown
- Open load detection in ON and OFF state
- Detailed SPI diagnosis or simple error flag
- Green product (RoHS compliant)

Description

The IFX9201SG is a general purpose 6 A H-Bridge, designed for the control of DC motors or other inductive loads. The outputs can be pulse width modulated at frequencies up to 20kHz. PWM/DIR control reduces the number of PWM capable pins needed on the microcontroler side.

For load currents above the current limitation threshold (8A typ.) the H-Bridge goes into chopper current limitation mode. It is protected against short circuits and overtemperature and provides extensive diagnosis via SPI or basic feedback via error flag. Open load can be detected when the bridge is disabled or during PWM operation of inductive loads.

The robust PG-DSO-12-17 package provides excellent thermal capabilites due to the thick copper heat slug. Thanks to the protruding edges of the heatslug the package is well suited for automatic optical solder inspection.

The IFX9201SG is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications. For automotive applications please refer to the TLE9201SG.

Type	Package	Marking
IFX9201SG	PG-DSO-12-17	IFX9201SG

2 Pin Configuration

2.1 Pin Assignment

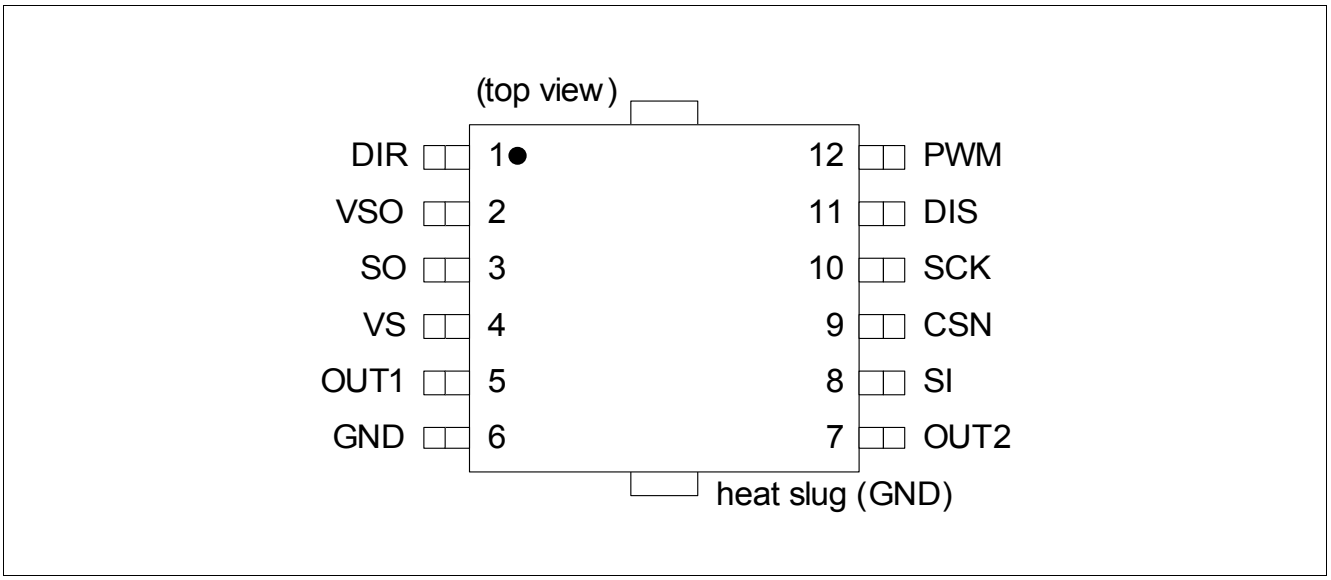


Figure 1 Pin Assignment IFX9201SG

2.2 Pin Definitions and Functions

Pin	Symbol	Function
1	DIR	Direction input to define direction of the motor current
2	VSO	Supply pin for SO output. Connect to 5V or 3.3V depending on desired logic level
3	SO	SPI serial output
4	VS	Supply voltage
5	OUT1	Output 1
6	GND	Ground
7	OUT2	Output 2
8	SI	SPI serial input
9	CSN	SPI chip select (low active)
10	SCK	SPI clock input
11	DIS	Disable. Disables the outputs (all MOSFETS off)
12	PWM	Pulse width modulation input

2.3 Terms

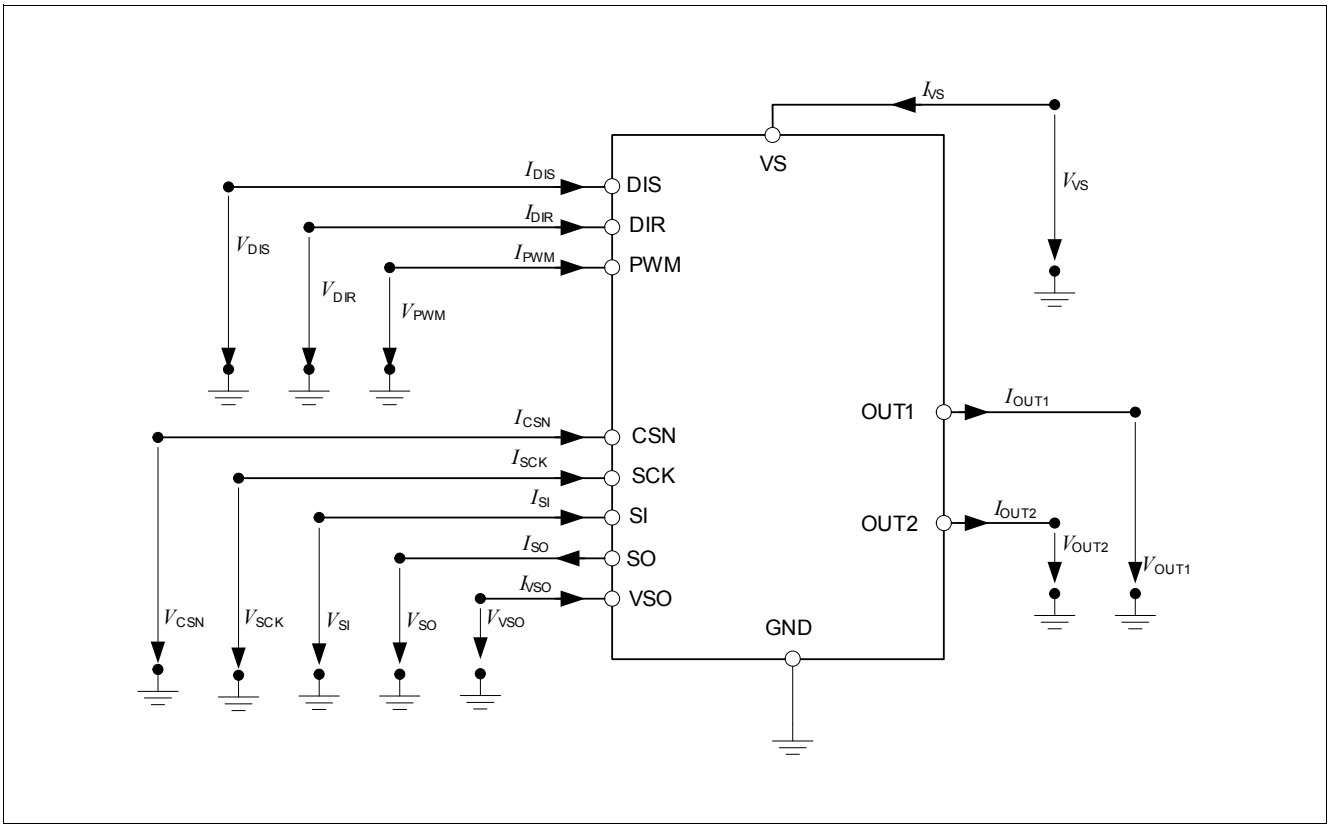


Figure 2 Terms IFX9201SG

3 Block Diagram

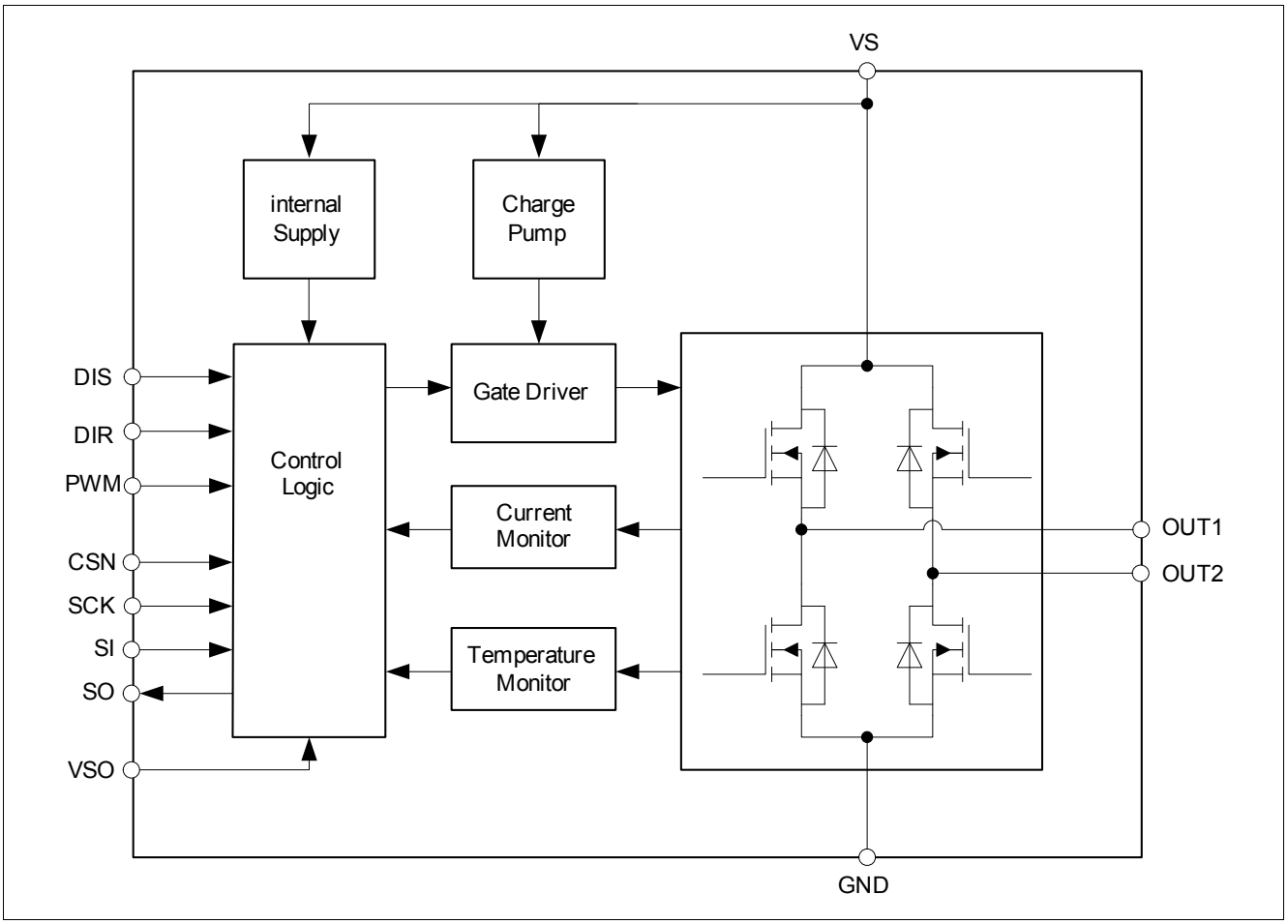


Figure 3 Block Diagram

4 Block Description

4.1 Power Supply

All internal supply voltages are derived from the pin VS. A charge pump provides the gate voltage for the high side switches. The charge pump does not require an external capacitor.

The output buffer of the digital output SO is supplied by the pin VSO. Therefore the output level at SO can be easily configured for 3.3 V or 5 V logic by connecting VSO to the respective voltage.

4.2 Sleep Mode

In order to minimize current consumption during inactive phases the device can be put into sleep mode by pulling the VSO pin to GND. This functionality can also be used to provide a second switch off path for the outputs similar to an enable pin, simply by driving VSO directly from a microcontroller output.

Since VSO is supplying also the output buffer of the SO signal it has to be ensured that the microcontroller output can provide sufficient current. Alternatively an external mosfet or a driver stage could be used to switch the VSO supply voltage. To account for dynamic switching currents it might be advisable to buffer VSO with a small capacitor (see **Figure 7 “Application Example VSO as Enable Input” on Page 24**).

Please note that the push pull stage of the SO output provides a current return path to VSO via the bulk diode of the highside mosfet. Therefore it has to be ensured that the voltage at SO never exceeds the voltage at VSO by more than 0.3V.

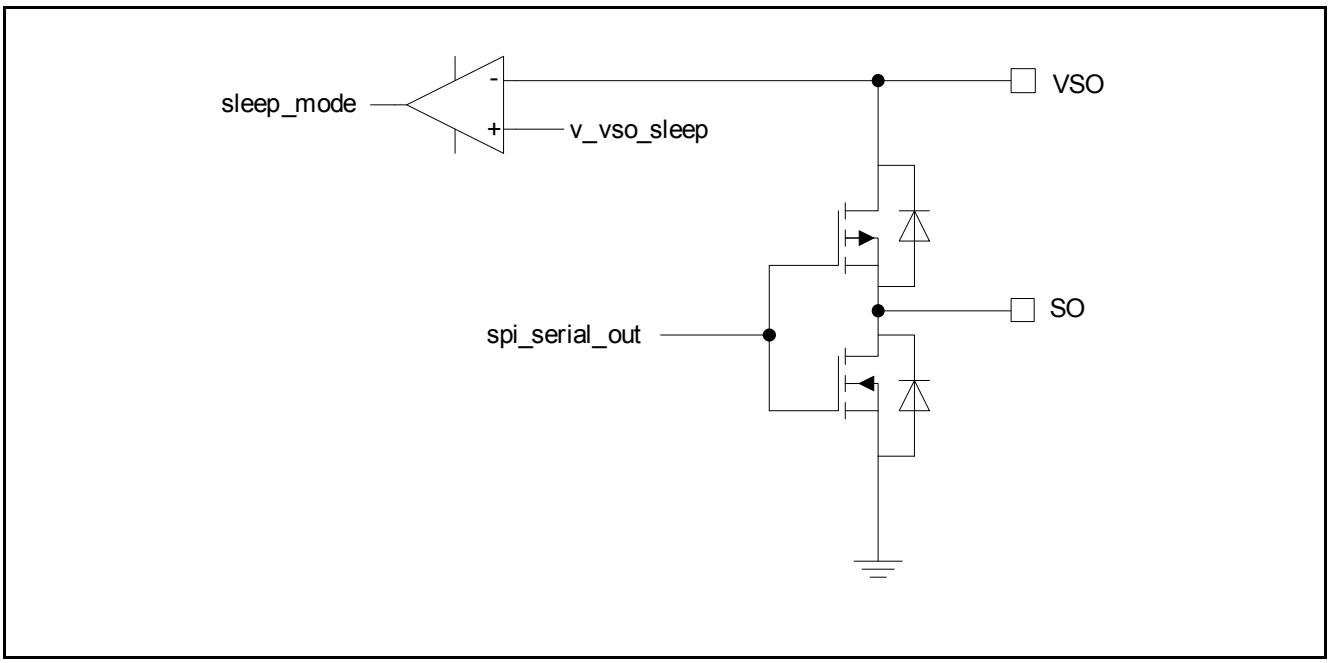


Figure 4-1 SO output buffer

4.3 Output Stages

The output stages consist of four n-channel mosfets in H-bridge configuration. The outputs are protected against short circuits and over temperature.

The bridge is controlled using the inputs PWM and DIR. The signal at DIR is defining the direction of the driven DC motor whereas the PWM signal sets the duty cycle.

The outputs can be set tristate (i.e. high side and low side switches are turned off) by setting DIS to high level.

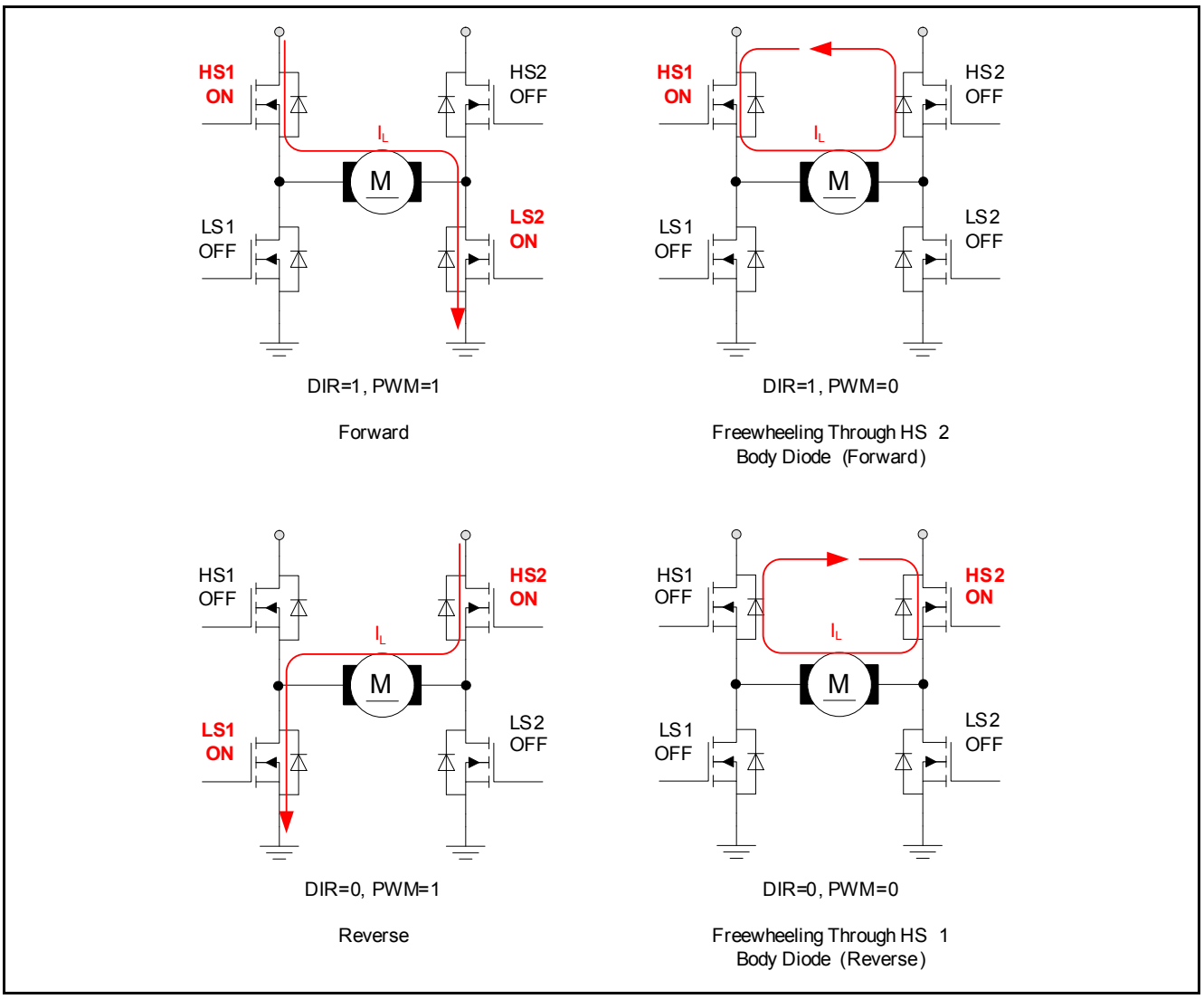


Figure 4-2 Operation Modes

Table 4-1 Output Truth Table

DIS	PWM	DIR	OUT1	OUT2	Comment
1	X	X	Z	Z	disabled, outputs tristate
0	1	1	H	L	forward / clockwise
0	1	0	L	H	reverse / counterclockwise
0	0	1	H	Z	freewheeling in HS (forward)
0	0	0	Z	H	freewheeling in HS (reverse)

4.4 Protection and Diagnostics

Both output stages of the IFX9201SG are equipped with fault diagnostic functions:

- Short to supply voltage (SCVS)
- Short to ground (SCG)
- Open load (OL)
- Over-temperature (OT)

4.5 Current Limitation

To limit the output current a chopper current limitation is integrated. Current measurement for current limitation is done in the high side path.

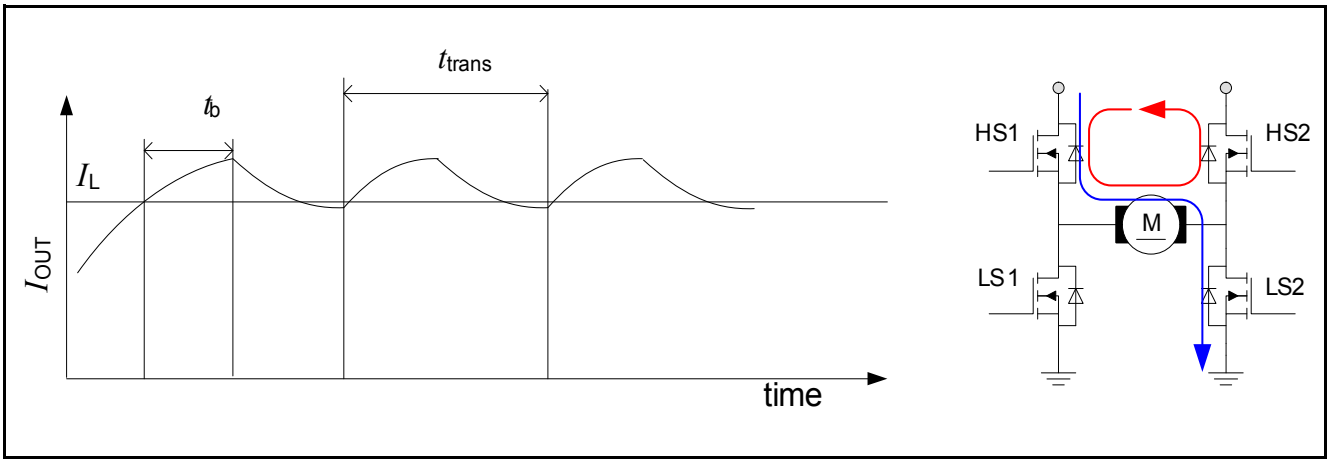


Figure 4-3 Chopper Current Limitation

Figure 4-3 shows the behavior of the current limitation for over current detection in HS1. It applies accordingly also for HS2.

When the current in high-side switch of OUT1 (HS1) exceeds the limit I_L longer than the blanking time t_b, the low side switch of OUT2 (LS2) is switched off, independent of the input signal at PWM. This leads to freewheeling through the bulk diode of HS2 and therefore to a decrease of the load current. As soon as the current falls below I_L, OUT2 is switched back to normal operation, i.e. the outputs follow the inputs according to the truth table. To avoid high switching frequencies in case of low inductive loads the minimum time between two transitions is limited to t_{trans}.

4.6 Short Circuit to Ground

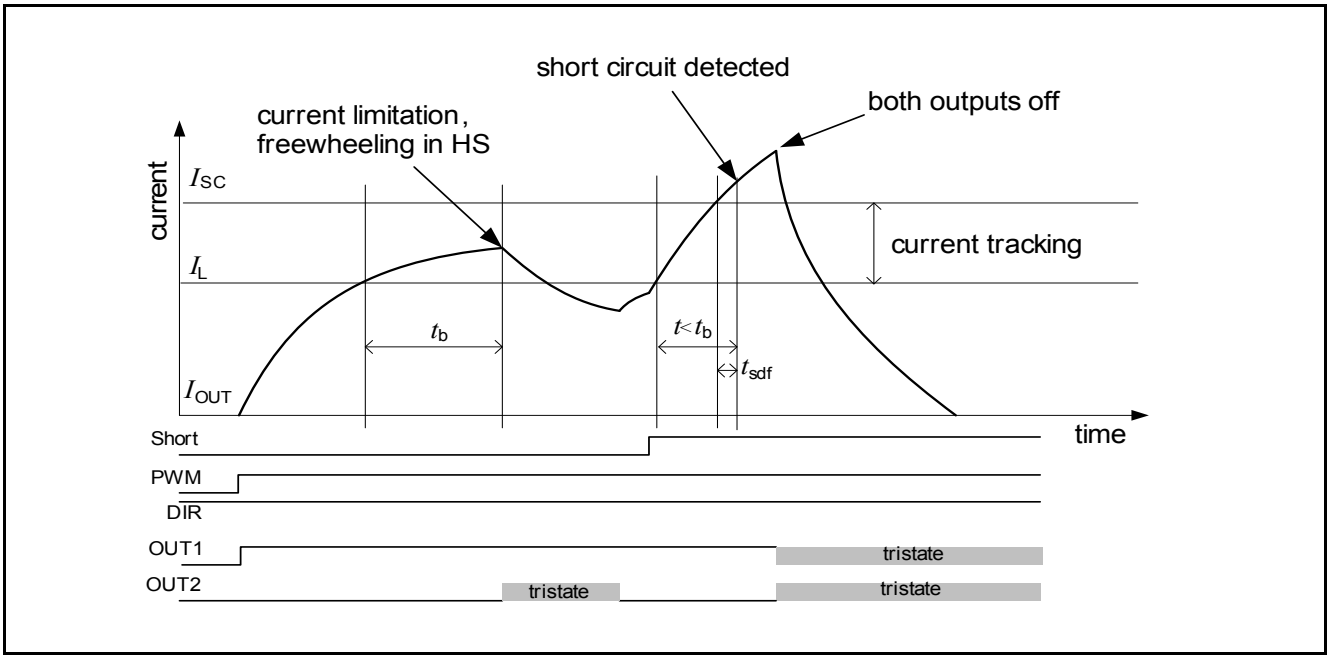


Figure 4-4 Short to Ground Detection

The short circuit to ground detection is activated when the current through one of the high side switches rises over the threshold I_{SC} and remains higher than I_{SC} for at least the filter time t_{sdf} within the blanking time t_b. Both outputs will be switched off and the failure will be reported in the SPI diagnosis register. The outputs can be re-activated by disabling and enabling the bridge via the disable signal DIS, pulling VSO to GND or by a reset command via SPI.

4.7 Short Circuit to Supply

A short circuit to the supply voltage VS is detected in the same way as a short circuit to ground, only in the low side switch instead of the high side switch.

4.8 Short Circuit over Load

Short circuit over load will trigger the short circuit detection either of the high side or the low side switch (whichever is faster).

4.9 Overtemperature

In case of high DC-currents, insufficient cooling or high ambient temperature, the chip temperature may rise above the thermal shut-down temperature T_{jSD}. In that case, all output transistors are turned off. Overtemperature shutdown is latching.

The outputs can be re-activated as soon as the junction temperature has fallen below the switch-on temperature T_{jSO}.

4.10 Undervoltage Shut-Down

If the supply voltage at the VS pins falls below the undervoltage detection threshold V_{UV_OFF}, the outputs are turned off. The undervoltage detection is not latching. That means that as soon as V_S rises above V_{UV_ON} again, the device is returning to normal operation.

4.11 Open Load Detection

4.11.1 Open Load Detection in OFF state

When the bridge is disabled (DIS=high) the open load in OFF detection becomes active. Two diagnostic current sources will then be connected to the outputs, a pull up current source at OUT1 and a pull down current source at OUT2. The pull down current source is stronger than the pull up current source and therefore will pull down OUT1 if a load is present. If no load is present OUT1 will be pulled high by the pull up current source. This is detected by a comparator and reported in the SPI diagnosis register.

Please note that capacitors that might be placed at the outputs for EMC reasons first have to be discharged by the pull down current source at OUT2 for the open load detection to work properly.

Also, if current is flowing through the load at the time of disabling the freewheeling current will force the outputs towards supply voltage V_S. This may lead to an erroneous reporting of open load.

Therefore the first diagnostic reading after disabling should be discarded and a second reading should be taken after the load is deenergized and the output capacitors are discharged completely.

The open load detection can be disabled by setting the OLDIS bit in the CTRL_REG register. This will disconnect the diagnostic current sources and suppress the reporting of open load in the DIA_REG register.

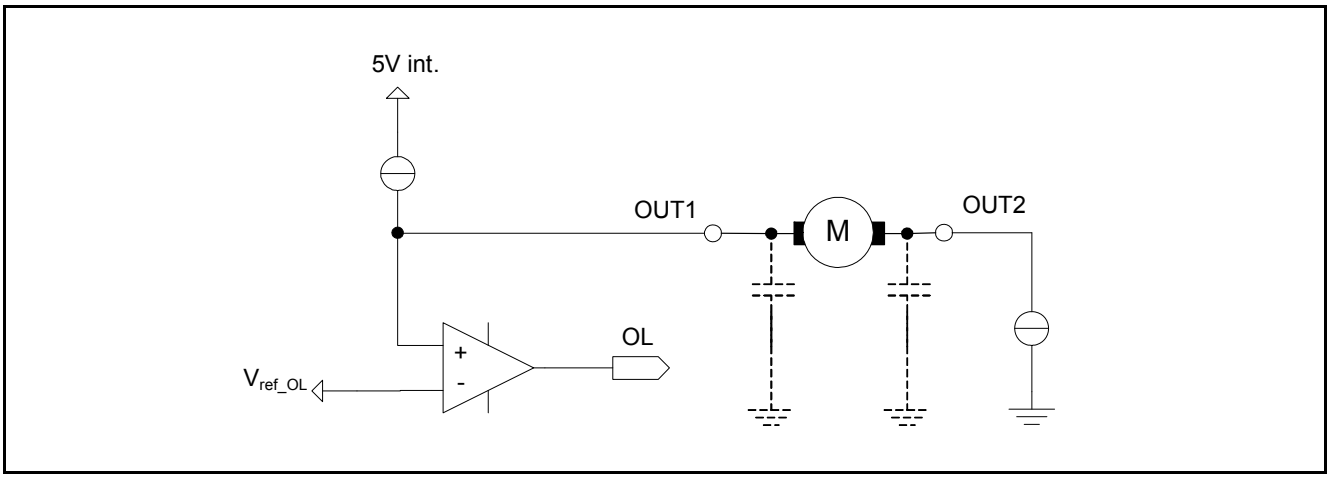


Figure 4-5 Open Load Detection in OFF state

4.11.2 Open Load Detection in ON state

The IFX9201SG contains an open load diagnosis during operation for inductive loads. It evaluates whether freewheeling occurs in the switching phase. In order to avoid inadvertent triggering of the open load diagnosis a failure counter is implemented. There have to be at least 5 occurances of the internal open load signal (i.e. 5 PWM pulses without freewheeling detected) before open load is reported in the SPI diagnosis register.

Depending on the operation conditions and on external circuitry like the output capacitors it is possible that open load is indicated although the load is present. This might be the case for example during a direction change or for small load currents respectively small PWM duty cycles. Therefore it is recommended to evaluate the open load diagnosis only in known suitable operating conditions and to ignore it otherwise.

The open load diagnosis is not latching.

4.12 Serial Peripheral Interface (SPI)

For diagnosis purposes the IFX9201SG is equipped with a “Serial Peripheral Interface“ (SPI).

The SPI of several IFX9201SGs can be connected in daisy chain configuration in order to save microcontroller interface pins.

The IFX9201SG is configured as a “slave” device. This means that the µC as the master is providing the chip select (CSN) and clock signal (SCK).

A data transfer on the SPI bus is initiaded with a falling edge on CSN and is terminated by a rising edge on CSN. The data on the serial input pin SI is sampled with the falling edge of SCK, the serial data output at SO is determined by the rising clock edge. The data is transferred “MSB first”.

The word length of the SPI is 8 bit. Please note that there is no check for the number of clocks within a SPI frame. Any low pulse at CSN will be regarded as one frame.

4.12.1 Error Flag

Between the falling edge of CSN and the first rising edge of SCK an additional error flag signal is set asynchronously at the SO pin. The error flag signal set to high whenever the output stages are shut down (tristate) due to a failure or due to disabling of the output stages. Additionally the EF signal is OR’ed with the SI input signal. By connecting the SO of one device to the SI of the next device the EF signal can be routed through similar to a SPI daisy chain configuration.

This flag can be used for simple error feedback without SPI communication by connecting SCK and CSN to GND permanently (see **Figure 5 “Application Example H-Bridge with Error Flag” on Page 22**).

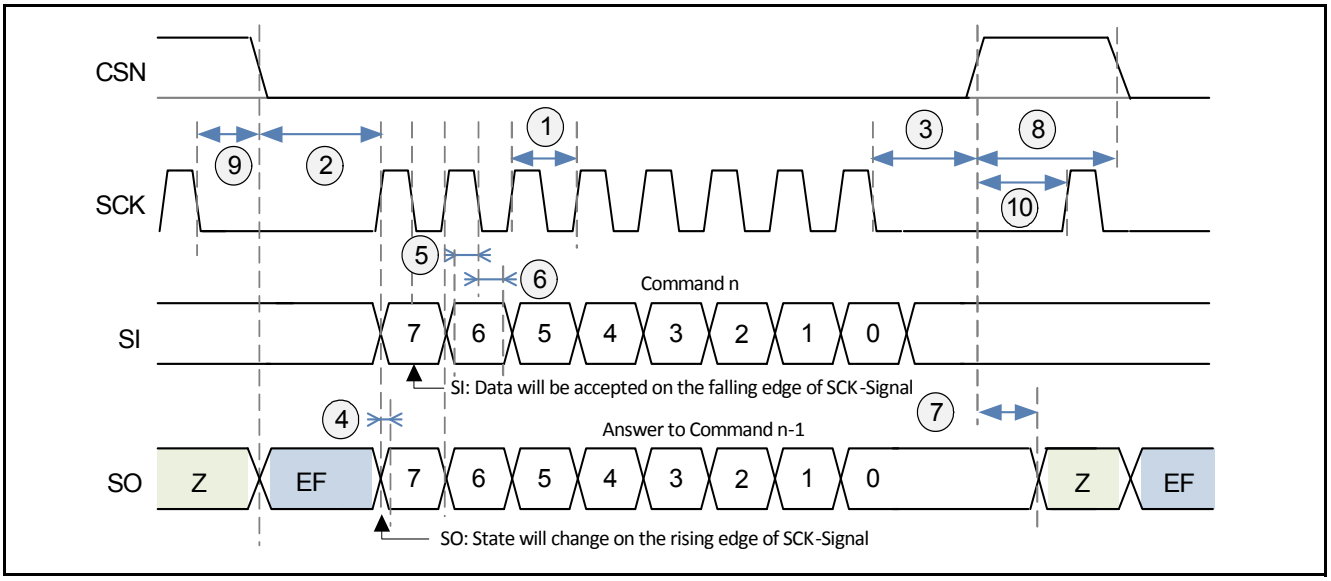


Figure 4-6 SPI Timing Definition (drawing not to scale)

4.12.2 SPI Register Description

The IFX9201SG provides detailed diagnosis and the option to control the outputs via SPI. Following commands are available (x=don't care, d=data):

Table 4-2 SPI Command Set

Command	Input Byte	Description
RD_DIA	000x xxxx	Read Diagnosis Register
RES_DIA	100x xxxx	Reset Diagnosis Register
RD_REV	001x xxxx	Read Device Revision Number
RD_CTRL	011x xxxx	Read Control Register
WR_CTRL	111d dddd	Write Control - sets and returns Control Register values
WR_CTRL_RD_DIA	110d dddd	Write Control and Read Diagnosis- sets Control Register values and returns Diagnosis Register values

The first SPI response provided after power up is the device revision number (RD_REV). For any unspecified commands the device will respond with the content of the diagnosis register (RD_DIA).

4.12.2.1 Control Register

Control Register

CTRL_REG	Offset	Reset Value
ControlRegister	01_H	00_H

7	5	4	3	2	1	0
CMD		OLDIS	SIN	SEN	SDIR	SPWM
rw		rw	rw	rw	rw	rw

Field	Bits	Type	Description
CMD	7:5	rw	**Command** **011: RD_CTRL** **110: WR_CTRL_RD_DIA** **111: WR_CTRL**
OLDIS	4	rw	**Open Load Disconnect** **1: Open load current source disconnected.**
SIN	3	rw	**SPI control** **0: Control outputs via PWM/DIR inputs** **1: Control outputs via SPI** **Note: can only be set if DIS=0 and PWM=0 and DIR=0. Any change of the DIS, PWM or DIR signals will reset this bit and revert to standard control via PWM/DIR**
SEN	2	rw	**1: Enable outputs in case of SPI control (SIN=1)** **0: Disable outputs in case of SPI control (SIN=1)**
SDIR	1	rw	**DIR Signal in case of SPI control (SIN=1)**
SPWM	0	rw	**PWM Signal in case of SPI control (SIN=1)**

4.12.2.2 Diagnosis Register

Diagnosis Register

DIA_REG	Offset	Reset Value
Diagnosis Register	00_H	DF_H

7	6	5	4	3	2	1	0
EN	OT	TV	CL	DIA4	DIA3	DIA2	DIA1
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
EN	7	r	**1= outputs enabled by low signal on pin DIS** **0 = outputs disabled by high signal on pin DIS**
OT	6	r	**0 = overtemperature shutdown**
TV	5	r	**Always 0 - used for transmission validation**
CL	4	r	**0 = current limitation active**
DIA4	3	r	**Diagnosis bit 4**
DIA3	2	r	**Diagnosis bit 3**
DIA2	1	r	**Diagnosis bit 2**
DIA1	0	r	**Diagnosis bit 1**

Diagnosis Truth Table

The short circuit and VS undervoltage diagnosis is coded in the DIA bits according to the following truth table. Together with transmission validation bit TV (always 0) it is ensured that there is always at least one 1->0 change at SO during a valid transmission. Therefore a “stuck at” failure of the SO pin can be detected.

Table 4-3 Encoding of Diagnosis Bits (sorted by hex value, only listed combinations are valid)

Type	DIA4	DIA3	DIA2	DIA1	Hex	Comment
No failure	1	1	1	1	0xF	-
Short to GND at OUT1 (SCG1)	1	1	1	0	0xE	latched
Short to VS at OUT1 (SCVS1)	1	1	0	1	0xD	latched
Open Load (OL)	1	1	0	0	0xC	not latched
Short to GND at OUT2 (SCG2)	1	0	1	1	0xB	latched
Short to GND at OUT1 and OUT2 (SCG1, SCG2)	1	0	1	0	0xA	latched
Short to VS at OUT1 and short to GND at OUT2 (SCVS1, SCG2)	1	0	0	1	0x9	latched
Short to Supply at OUT2 (SCVS2)	0	1	1	1	0x7	latched
Short to GND at OUT1 and short to VS at OUT2 (SCG1, SCVS2)	0	1	1	0	0x6	latched
Short to VS at OUT1 and OUT2 (SCVS1, SCVS2)	0	1	0	1	0x5	latched
VS Undervoltage (VS_UV)	0	0	1	1	0x3	not latched

Reset Behavior of Diagnosis Register

The diagnosis register is reset by the following events

Table 4-4 Diagnosis Reset Types

Name	Type	Comment
POR	Power On Reset	Reset due to power up, undervoltage or sleep mode
ENR	Enable Reset	Reset due to disabling/enabling of the outputs by DIS pin or bit SEN in CTRL_REG
SPIR	SPI Reset	Reset by sending the RES_DIA command via SPI

A change of the DIR signal will lead to a reset of current limitation (CL) or open load in on (OL) error messages. The open load in on failure will also be reset automatically if the open load condition no longer persits, i.e. freewheeling is detected for five or more consecutive pulses.

4.12.2.3 Revision Register

The Revision Register contains the device revision corresponding to the mask set.

Revision Register

REV_REG	Offset	Reset Value
Revision Register	01_H	00_H

7	6	5	4	3 … 0
0	0	1	0	REV
r	r	r	r	r

Field	Bits	Type	Description
0	7	r	**fixed to 0**
0	6	r	**fixed to 0**
1	5	r	**fixed to 1**
0	4	r	**fixed to 0**
REV	3:0	r	**Device Revision corresponding to mask set**

5 General Product Characteristics

5.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to 125 °C; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction temperature	T_j	-40	–	150	°C	–	P_5.1.1
Storage temperature	T_s	-55	–	150	°C	–	P_5.1.2
Supply voltage	V_{VS}	-0.3	–	40	V	–	P_5.1.4
Supply for logic output	V_{VSO}	-0.3	–	5.5	V	–	P_5.1.5
Voltage at logic inputs	V_{IN}	-0.3	–	5.5	V	–	P_5.1.6
Voltage at logic output SO	V_{SO}	-0.3	–	V_{VSO} +0.3	V	both conditions must be observed	P_5.1.7
		-0.3	–	5.5			
ESD Susceptibility							
ESD Susceptibility to GND acc. HBM	V_{ESD}	-2	–	2	kV	HBM[2)]	P_5.1.8
ESD Susceptibility to GND acc. CDM	V_{ESD}	-500	–	500	V	CDM[3)]	P_5.1.9
ESD Susceptibility to GND acc. CDM, Corner Pins	V_{ESD}	-750	–	750	V	CDM[3)], Corner Pins	P_5.1.10

1) Not subject to production test, specified by design.

2) ESD susceptibility HBM according to EIA/JESD22-A114-B (1.5kΩ, 100pF)

3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

5.2 Functional Range

Table 2 Functional Range[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range	V_S	V_{UV_OFF}	–	36	V	–	P_5.2.1
V_S supply voltage slew rate	dV_S/dt	-10	–	10	V/µs	–	P_5.2.2
SO buffer supply voltage	V_{SO}	2.9	–	5.5	V	–	P_5.2.3
Junction Temperature	T_j	-40	–	125	°C	–	P_5.2.4

1) Not subject to production test, specified by design.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

5.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case	R_{thJC}	–	–	2	K/W	–	P_5.3.1
Junction to Ambient	R_{thJA}	–	30	–	K/W	2)	P_5.3.2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

6 Electrical Characteristics

Table 4 Electrical Characteristics

V_{VS} = 8 V to 36 V; V_{VSO} = 5.0 V; T_j = -40 °C to 125 °C; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply							
Supply Current	I_{VS}	–	5	13	mA	f_{PWM} = 2 kHz; I_{OUT} = 0 A; V_{VS} = 13.5 V;	P_6.0.1
Supply Current Sleep Mode	I_{VS}	–	19	30	µA	V_{VS} = 13.5 V; V_{VSO} = 0 V; V_{OUTx} = 0 V; T_j = 25 °C	P_6.0.2
VSO Sleep Mode Threshold	V_{VSO_sleep}	0.5	–	2.0	V	–	P_6.0.4
VSO Input Current, CSN high	I_{VSO}	–	–	100	µA	I_{SO} = 0 A; V_{CSN} > 2 V	P_6.0.5
VSO Input Current, CSN low	I_{VSO}	–	–	1.0	mA	I_{SO} = 0 A; V_{CSN} = 0 V	P_6.0.6
VS Undervoltage							
Undervoltage at VS	$V_{UV\ OFF}$	3.5	4.2	5.0	V	Switch Off Threshold	P_6.0.7
Undervoltage at VS	$V_{UV\ ON}$	3.6	4.4	5.2	V	Switch On Threshold	P_6.0.8
Undervoltage at VS	$V_{UV\ HY}$	100	200	500	mV	Hysteresis	P_6.0.9
VS Undervoltage Detection Filter Time [1]	t_{UV}	–	1	–	µs	–	P_6.0.10
Inputs PWM, DIR, SCK, SI							
Low level	V_{input_L}	–	–	0.8	V	–	P_6.0.11
High level	V_{input_H}	2.0	–	–	V	–	P_6.0.12
Hysteresis	V_{input_HYS}	0.1	0.3	–	V	–	P_6.0.13
Pull Down Current	I_{in_pd}	9	38	85	µA	V_{in} = 5.5 V	P_6.0.14
Input Capacity[1]	C_{in}	–	–	15	pF	V_{bias} = 2 V; V_{test} = 20 mVpp; f = 1 MHz	P_6.0.15
Inputs DIS, CSN							
Low level	V_{input_L}	–	–	0.8	V	–	P_6.0.16
High level	V_{input_H}	2.0	–	–	V	–	P_6.0.17
Hysteresis	V_{input_HYS}	0.1	0.3	–	V	–	P_6.0.18
Pull Up Current	I_{in_pu}	9	38	85	µA	V_{in} = 0 V	P_6.0.19
Input Capacity[1]	C_{in}	–	–	15	pF	V_{bias} = 2 V; V_{test} = 20 mVpp; f = 1 MHz	P_6.0.20

Table 4 Electrical Characteristics

V_{VS} = 8 V to 36 V; V_{VSO} = 5.0 V; T_j = -40 °C to 125 °C; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output SO							
Low level	V_{SO_L}	0.0	–	0.4	V	I_{SO} = -1 mA	P_6.0.21
High level	V_{SO_H}	V_{VSO}-0.75	–	V_{VSO}	V	I_{SO} = 1 mA ; 2.9 V < V_{VSO} < 5.5 V	P_6.0.22
Tristage Leakage Current	I_{SO}	-5	–	5	µA	0V < V_{SO} < V_{VSO}; V_{VSO} = 5.5 V	P_6.0.23
Output Capacity[1)]	C_{SO}	–	–	19	pF	V_{bias} = 2 V; V_{test} = 20 mVpp; f = 1 MHz	P_6.0.24
Power Outputs OUT1, OUT2							
On resistance low side	R_{OUTL}	–	100	–	mΩ	I_{OUT} = 2 A; T_j = 25 °C	P_6.0.25
		–	–	200	mΩ	I_{OUT} = 2 A; T_j = 125 °C	
On resistance high side	R_{OUTH}	–	100	–	mΩ	I_{OUT} = 2 A; T_j = 25 °C	P_6.0.26
		–	–	200	mΩ	I_{OUT} = 2 A; T_j = 125 °C	
Leakage current	$I_{OUT1(off)}$ $I_{OUT2(off)}$	-25	–	25	µA	V_{VS} = 13.5 V; Outputs off; OLDIS high	P_6.0.27
		-100	–	25	µA	V_{VS} = 13.5 V; Sleep Mode	
Free-wheel diode forward voltage	U_D	–	0.9	1.0	V	I_D = 2 A	P_6.0.28
Output Switching Times [2)]							
Voltage Slew Rate HS	dV_{OUT}/dt	0.20	–	1.62	V/µs	V_{VS} = 13.5 V; R_{Load} = 6.8 Ω	P_6.0.29
Voltage Slew Rate LS	dV_{OUT}/dt	1.15	–	8.1	V/µs		P_6.0.31
PWM Frequency[1)]	f_{PWM}	0	–	20	kHz	–	P_6.0.33
Output Delay Times [2)]							
Output on-delay HS	$t_{d\_on(HS)}$	–	–	80	µs	V_{VS} = 13.5 V; R_{Load} = 6.8 Ω	P_6.0.34
Output off-delay HS	$t_{d\_off(HS)}$	–	–	80	µs		P_6.0.35
Output on-delay LS	$t_{d\_on(LS)}$	–	–	10	µs		P_6.0.36
Output off-delay LS	$t_{d\_off(LS)}$	–	–	10	µs		P_6.0.37
Disable delay time	t_{d_dis}	–	–	80	µs		P_6.0.38
Enable delay time	t_{d_en}	–	–	80	µs		P_6.0.39
Disable/Enable filter time[1)]	t_{f_en}	0.4	–	3	µs		P_6.0.40
Wake Up delay time[1)]	t_{wu}	–	–	1	ms	VSO high --> OUT high	P_6.0.41
Chopper Current Limitation							
Current Limit	I_L	6.0	8.0	10.0	A	V_{VS} = 13.5 V	P_6.0.42
Blanking time[1)]	t_b	5	8	13	µs	–	P_6.0.43
Minimum transition time[1)]	t_{trans}	–	95	–	µs	–	P_6.0.44

Table 4 Electrical Characteristics

V_{VS} = 8 V to 36 V; V_{VSO} = 5.0 V; T_j = -40 °C to 125 °C; (unless specified otherwise)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Short Circuit Detection							
Short circuit detection threshold high side switch	I_{SC_H}	8.0	11.5	14.5	A	V_{VS} = 13.5 V	P_6.0.45
Short circuit detection threshold low side switch	I_{SC_L}	8.0	11.5	14.5	A		P_6.0.46
Current tracking high side	I_{SC_H} - I_L	2.0	4.0	5.2	A		P_6.0.47
Current tracking low side	I_{SC_L} - I_L	1.8	3.5	5.2	A		P_6.0.48
Short Circuit detection filter time[1)]	t_{sdf}	–	2	–	µs	–	P_6.0.49
Open Load Detection in OFF State							
Pull up Current at OUT1	I_{OUT1_OL}	60	140	200	µA	V_{VS} = 13.5 V; V_{OUT1} = 0V	P_6.0.50
Pull down Current at OUT2	I_{OUT2_OL}	200	350	500	µA	V_{VS} = V_{OUT2} = 13.5 V	P_6.0.51
Ratio of current sources	$Ratio\_I_{OL}$	1.8	2.5	3.5	–	–	P_6.0.52
Open load detection in OFF filter time[1)]	t_{f_OL}	40	–	–	µs	–	P_6.0.53
SPI Timing (see Figure 4-6)[1)]							
Cycle-time (1)	t_{cyc}	490	–	–	ns	Referred to master	P_6.0.54
Enable Lead Time (2)	t_{lead}	50	–	–	ns	Referred to master	P_6.0.55
Enable Lag Time (3)	t_{lag}	150	–	–	ns	Referred to master	P_6.0.56
Data Valid (4) [3)]	t_v	– –	– –	150 230	ns	CL = 200 pF CL = 350 pF Referred to IFX9201SG	P_6.0.57
Data Setup Time (5)	t_{su}	40	–	–	ns	Referred to master	P_6.0.58
Data Hold Time (6)	t_h	40	–	–	ns	Referred to master	P_6.0.59
Disable Time (7)	t_{dis}	–	–	100	ns	Referred to IFX9201SG	P_6.0.60
Transfer Delay (8)	t_d	2	–	–	µs	Referred to master	P_6.0.61
Disable Lead Time (9)	t_{dld}	250	–	–	ns	Referred to master	P_6.0.62
Disable Lag Time (10)	t_{dlg}	250	–	–	ns	Referred to master	P_6.0.63
Thermal Shutdown							
Thermal Shutdown Junction Temperature[1)]	T_{jSD}	150	175	–	°C	–	P_6.0.64
Thermal Switch-On Junction Temperature[1)]	T_{jSO}	125	–	–	°C	–	P_6.0.65

1) Not subject to production test, specified by design.

2) Output switching times are measured between 20% and 80% of the output swing

3) V_{SO} timing thresholds are 20% / 80% of V_{VSO} for 4.5V<V_{VSO}<5.5V and 30% / 70% of V_{VSO} for 2.9V<V_{VSO}<4.5V

7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application

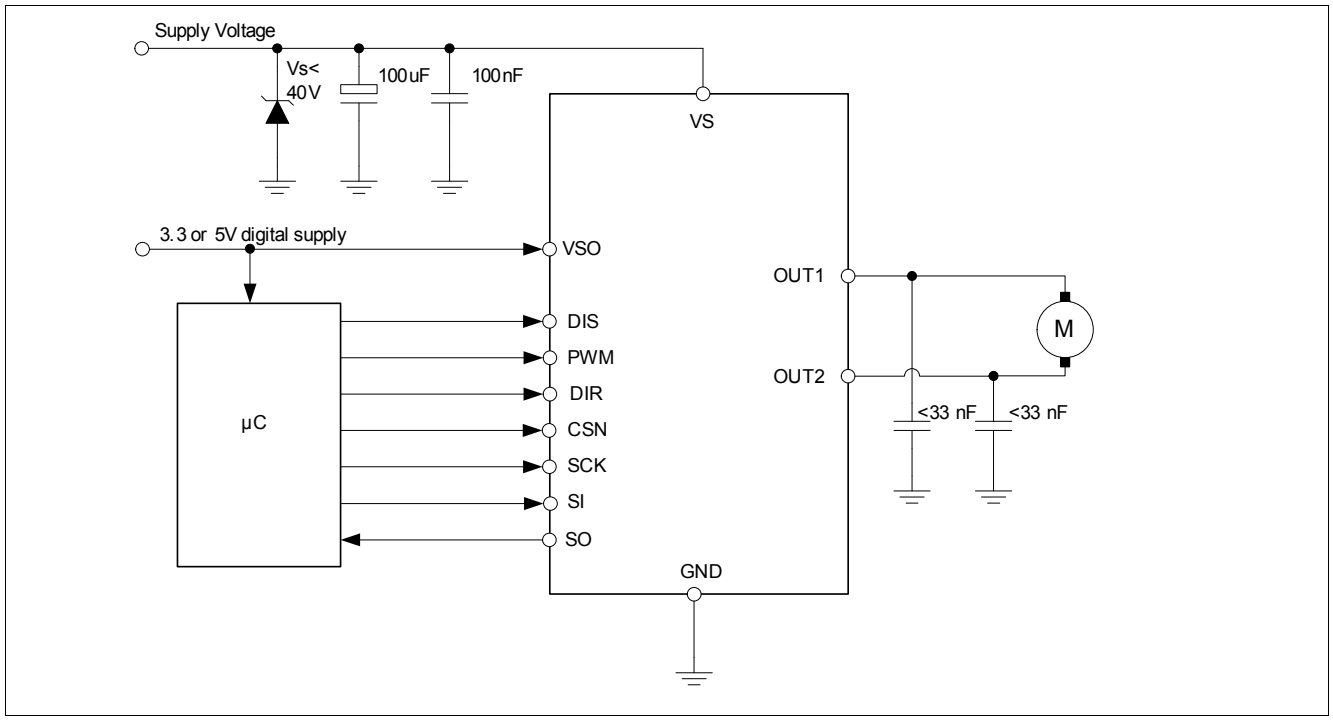


Figure 4 Application Example H-Bridge with SPI interface

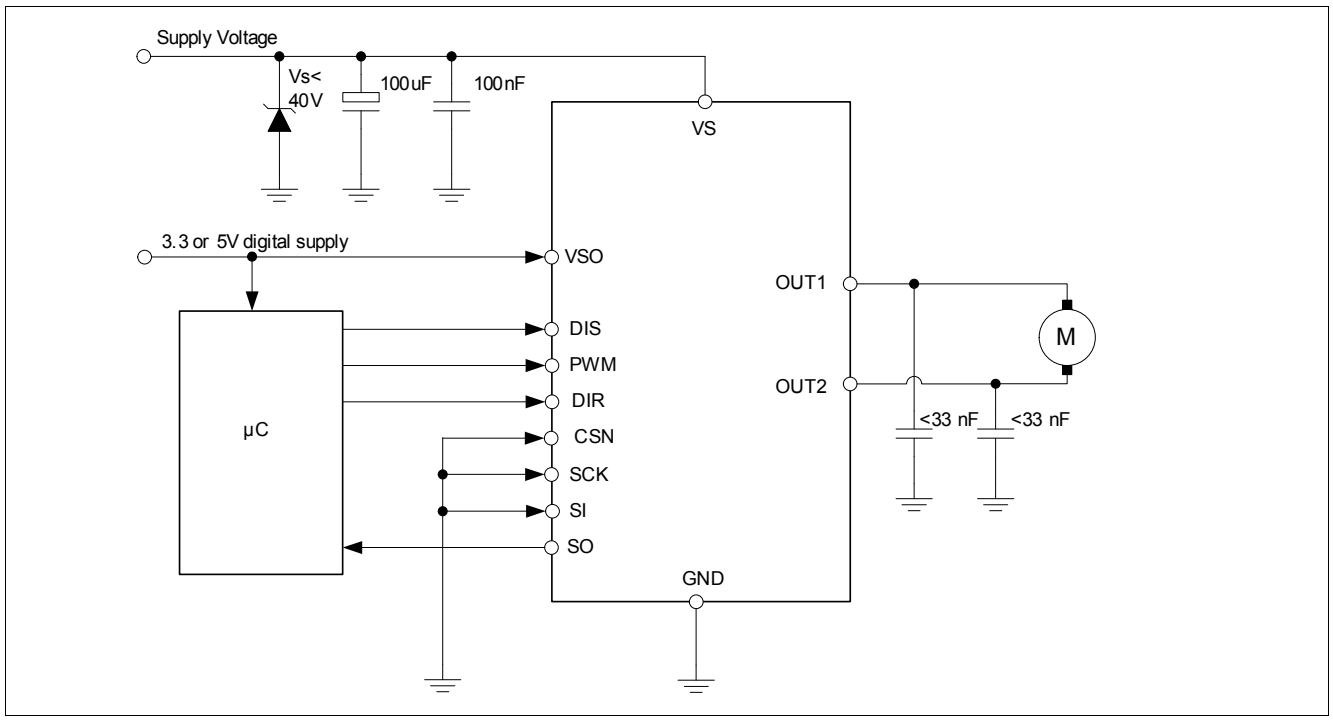


Figure 5 Application Example H-Bridge with Error Flag

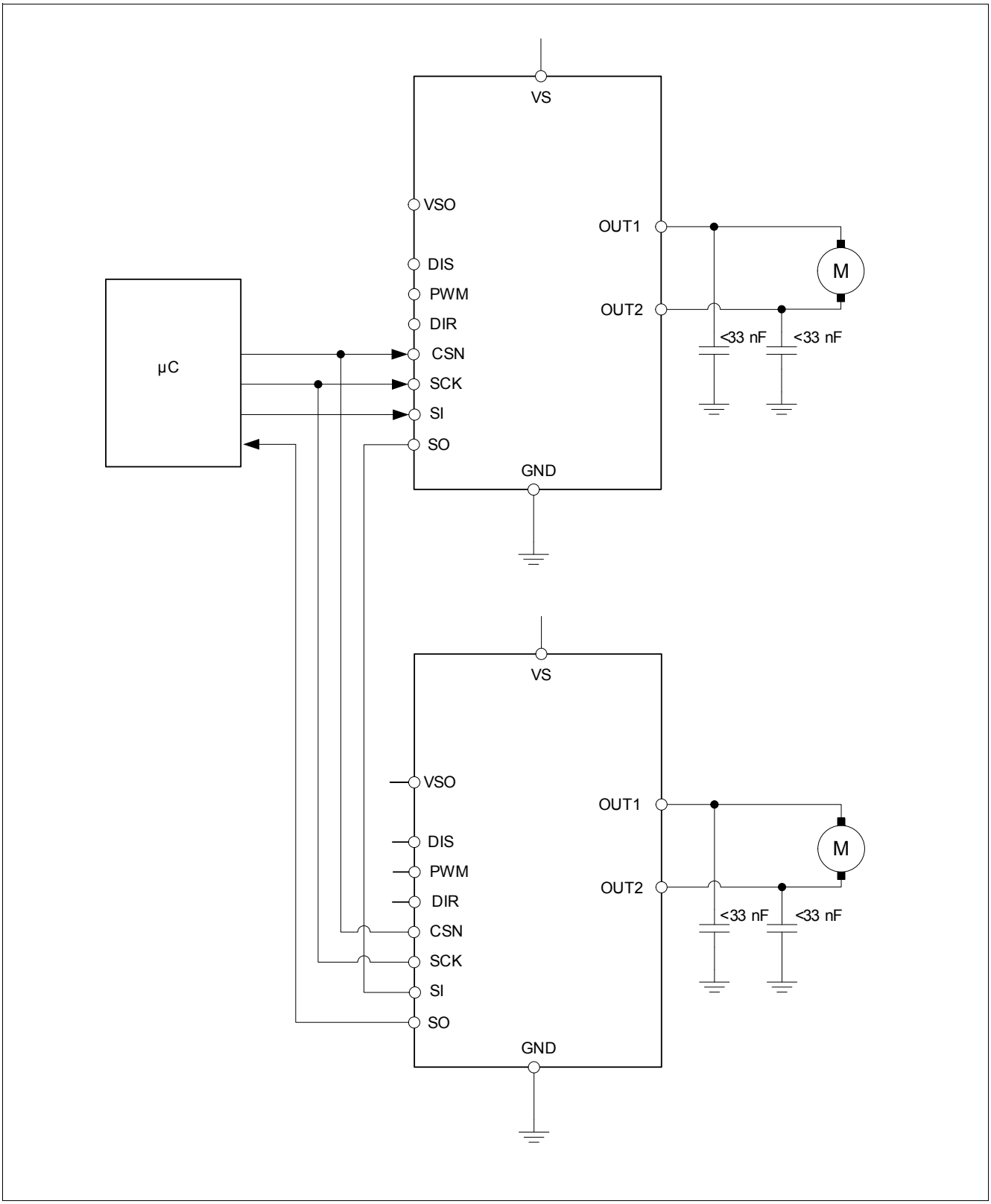


Figure 6 SPI Daisy Chain Konfiguration (other signals omitted for clarity)

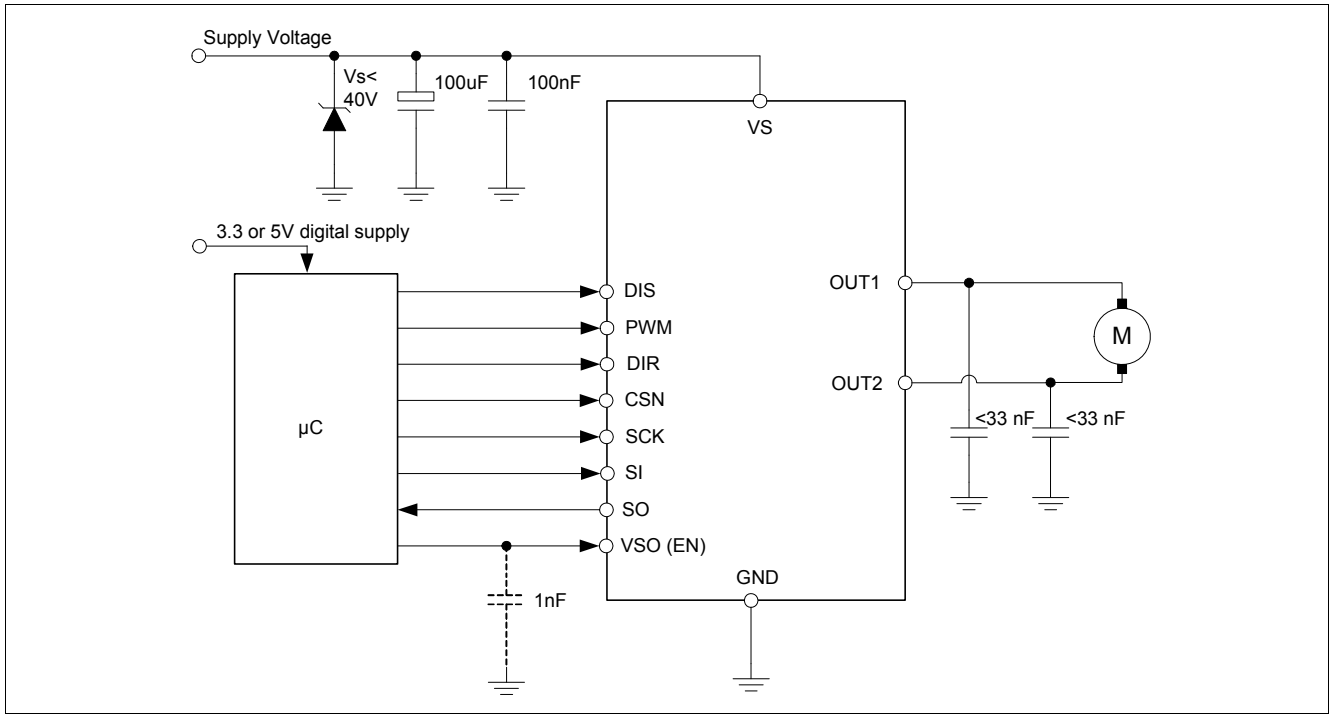


Figure 7 Application Example VSO as Enable Input

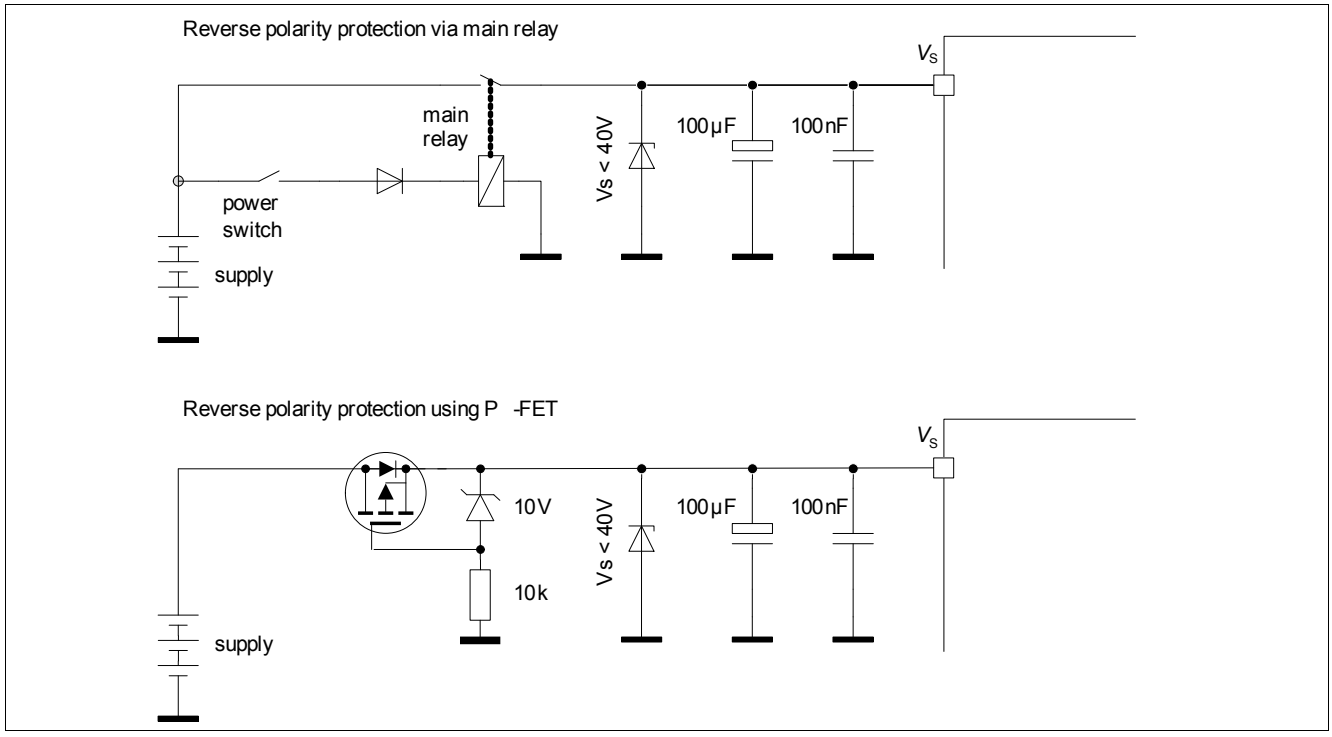
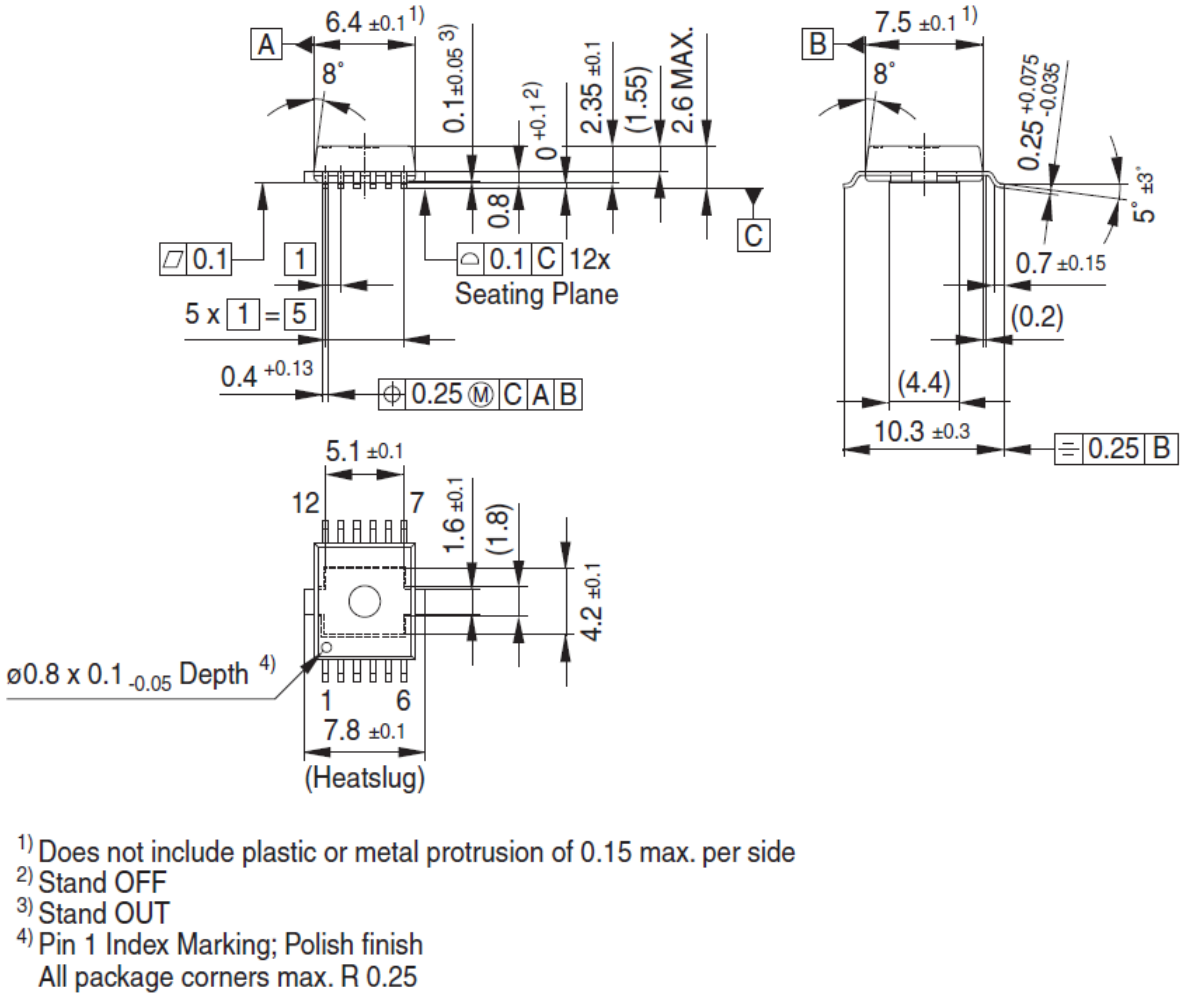


Figure 8 Examples for Reverse Polarity Protection

The IFX9201SG is not protected against reverse polarity. External measures have to be taken to ensure the right polarity of the supply voltage.

8 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Stand OFF
3) Stand OUT
4) Pin 1 Index Marking; Polish finish
All package corners max. R 0.25

Figure 9 PG-DSO-12-17

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
0.1	2014-04-16	Initial Product Proposal
0.2	2014-07-08	Target Data Sheet
0.3	2014-08-19	P_5.2.1: Supply voltage range max. changed to 36V Table 4: Voltage range for electrical characteristics changed to V_{VS} = 8V to 36V
1.0	2015-01-30	Data Sheet
1.1	2015-02-15	Device description updated in Overview page (page 3) Disclaimer updated

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