ILLUMINANT 北極光企業有限公司

PRODUCT SPECIFICATION FOR LCM

CUSTOMER:	
MODEL NO:	IG-B322401-6BFLWA
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
北极光 2007.12.24 贺秋芳	北极光 2007.12.24 隆茂生	北极光 2007.12.24 隆茂生

□Approval for Specifications Only

■Approval for Specifications and Sample

Note: 1. Version of Specifications : 1

2. Others: Rohs Compliment

TAIWAN

1F, #15, LANE 75, MIN CHUAN E. RD., SEC 3, TAIPEI, TAIWAN.

Tel +886-2-25175115 Fax +886-2-25175099

CHINA

5F DONGWU COMMERICAL BLDG., LANSHAN RD., NORTH DISTRICT, HI-TECH INDUSTRIAL PARK, SHENZHEN, PRC.

TEL + 86-755-86154466 FAX +86-755-86154366

KOREA

RM 1201, IT MIRAE TOWER, 60-21, GASAN-DONG, GEUMCHEON-GU, SEOUL, 153-801, KOREA

TEL + 82-2-2027-5391~2 FAX +82-2-2027-5393

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Version	Date	Contents
1	07/12/24	Initial Release

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3. GENERAL SPECIFICATIONS :

3-1 SCOPE :

This specification covers the delivery requirements for the liquid crystal display delivered by ILLUMINANT to Customer.

3-2 PRODUCTS :

Liquid Crystal Display Module (LCM)

3-3 MODULE NAME

IG-B322401-6BFLWA

4. FEATURES :

(1) Display Type	: 320x240 Dots
(2) LCD Type	: STN Blue, Transflective, Negative
(3) Driving Method	: 1/240 Duty, 1/17 Bias
(4) Driver IC	: SED1335F0A/RA8835
(5) Viewing Direction	: 6 O'clock
(6) Interface	: 8080 Series

5. MECHANICAL SPECIFICATIONS :

ITEM	SPECIFICATIONS	UNIT
MODULE SIZE	148.02(W)X120.24(H)X12.00MAX(D)	mm
VIEWING AREA	122.00(W)X92.00(H)	mm
ACTIVE AREA	115.17(W)X86.37(H)	mm
BACKLIGHT	WHITE LED	--
ASSY.TYPE	COB	--
WEIGHT	TBD	--

NOTES :

LCM should be grounded during handling LCM.

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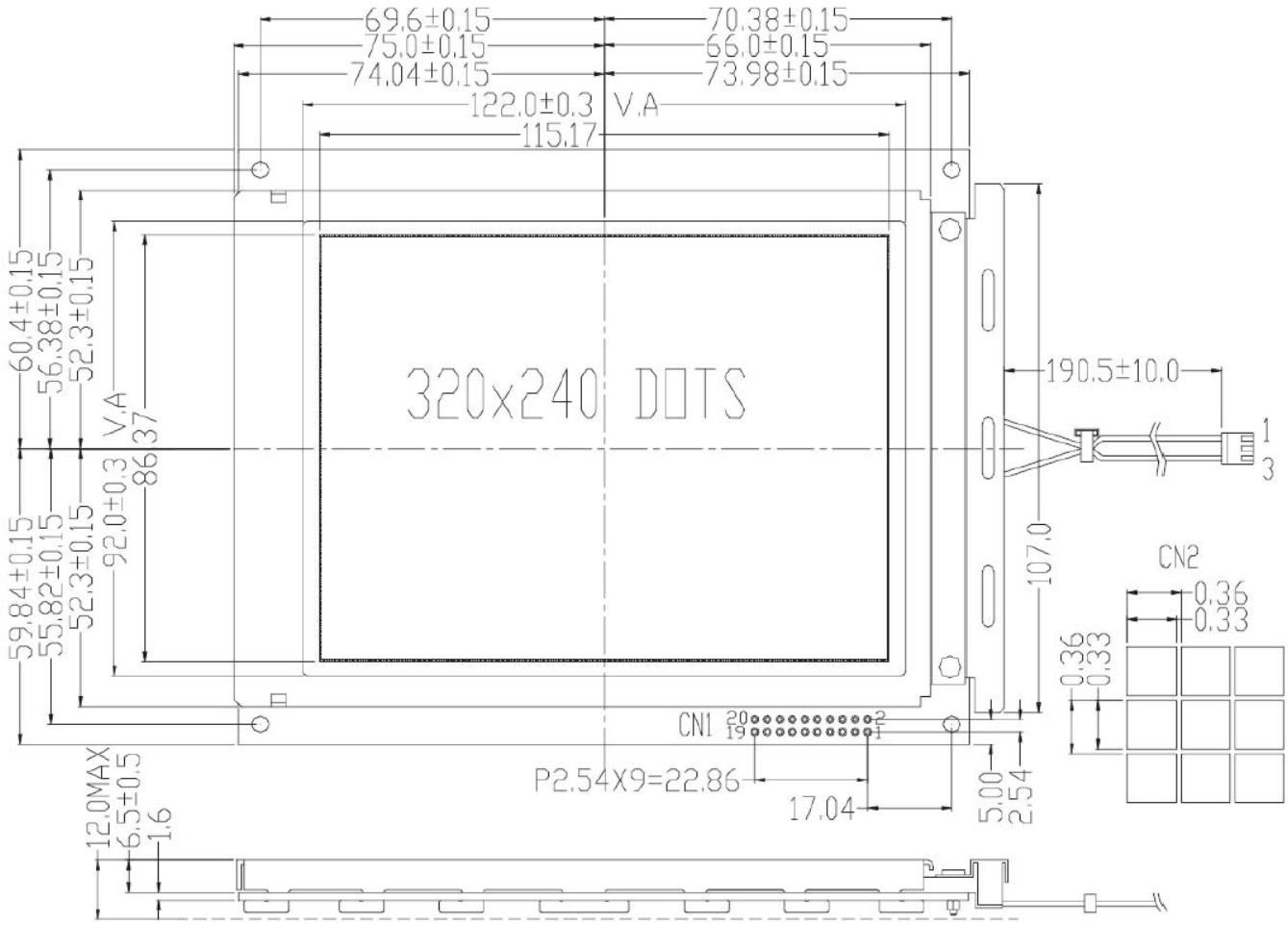
6. OUTLINE DIMENSIONS :



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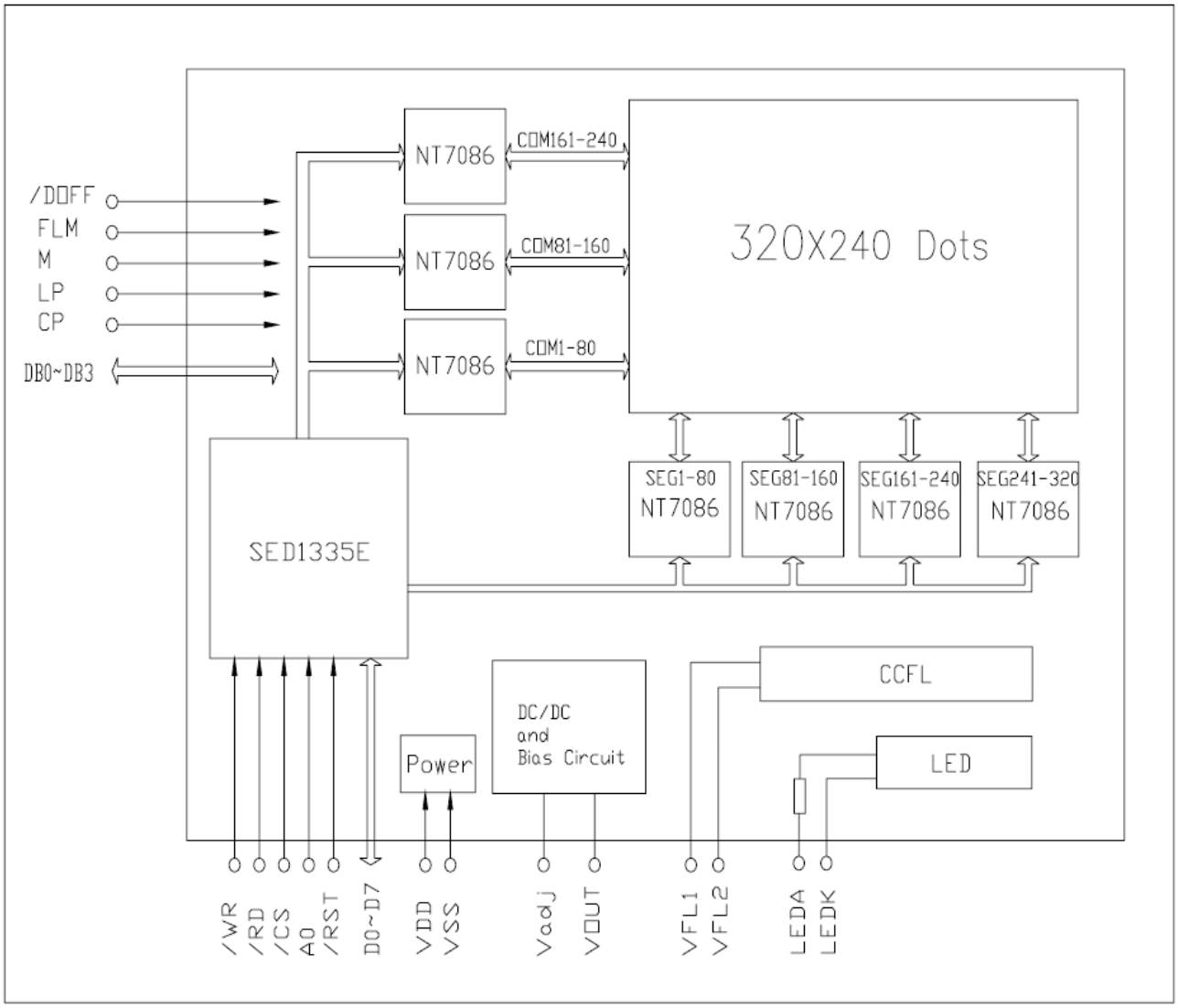
7. BLOCK DIAGRAM :



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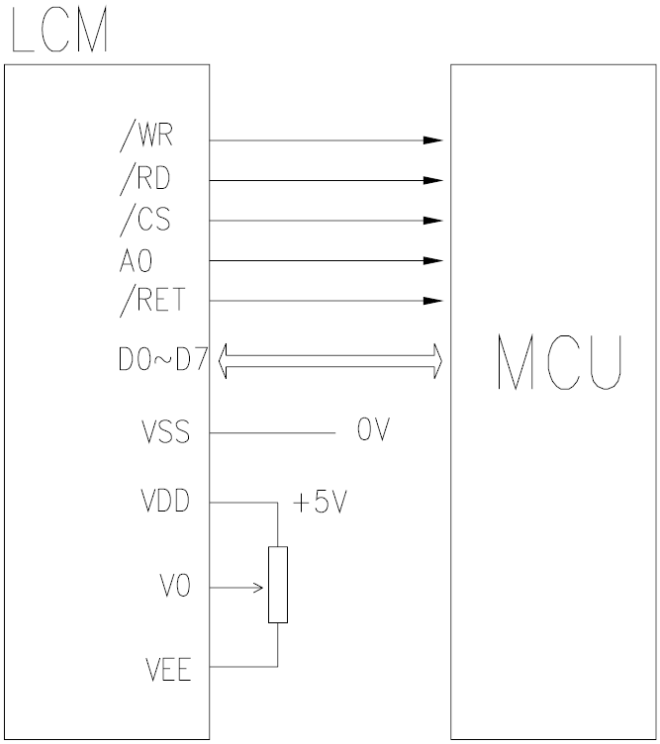
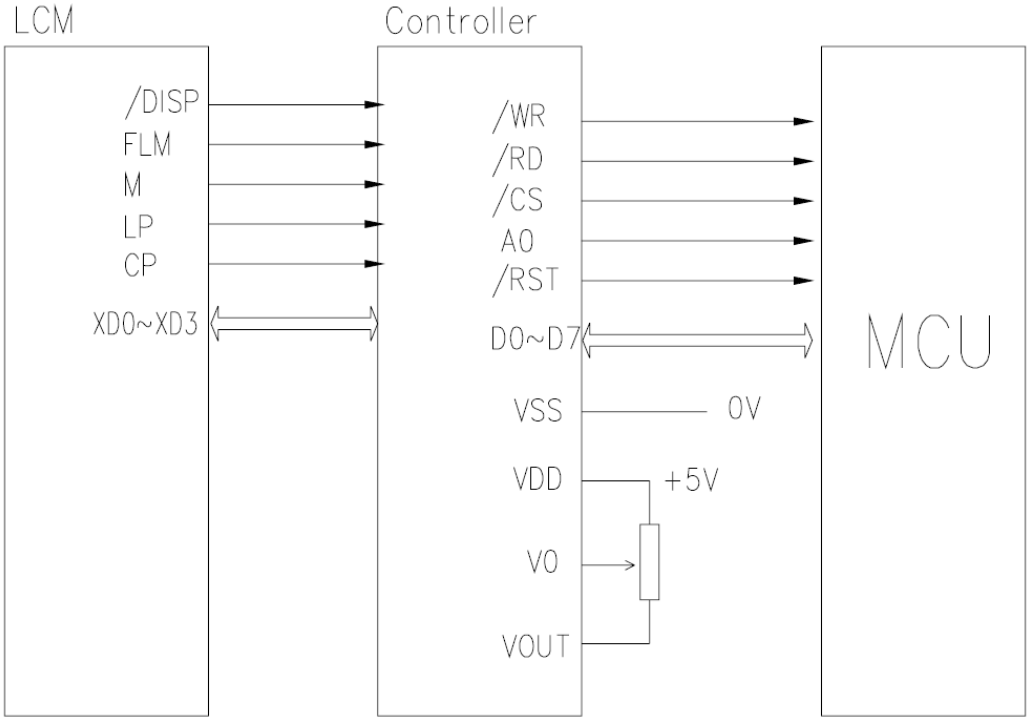
8. APPLICATION CIRCUIT

8-1 Built-in SED1335F/RA8835 Application



8-2 NT7086(NO Controller) Application



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9. ABSOLUTE MAXIMUM RATINGS :

CHARACTERISTICS	SYMBOL	CONDITION	STANDARD VAULE			UNIT
			MIN	TYP	MAX	
Power Supply For Logic	V_{DD}	Ta=25℃	-0.3	-	7.0	V
Input Voltage	V_{IN}	Ta=25℃	-0.3	-	VDD+0.3	V
Operating Temperature	T_{OPR}	---	-10	-	+60	℃
Storage Temperature	T_{STG}	---	-20	-	+70	℃
Storage Humidity	H_D	Ta<40℃	-		90	%RH

10. ELECTRICAL CHARACTERISTICS :

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage (Logic)	VDD-VSS	-	4.5	5.0	5.5	V
Supply Voltage (LCD)	VDD-V0	Ta=+25℃	-	22.4	-	V
Input Signal Voltage	V-IH	“H” Level	0.5VDD	-	VDD	V
	V-IL	“L” Level	VSS	-	0.2VDD	V
Output Signal Voltage	V-OH	“H” Level	2.4	-	-	V
	V-OL	“L” Level	-	-	VSS+0.4	V
Supply Current (Logic)	IDD	VDD=5.0V	-	-	-	uA
Backlight Voltage	V-BL	LED(White)	-	3.0	-	V
Backlight Current	I-BL	LED(White)	-	-	-	mA

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11. OPTICAL CHARACTERISTICS :

ITEM	SYMBOL	CONDITIONS	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Response Time	Tr	-	-	140	-	ms
	Tf	-	-	133	-	ms
Contrast Ratio	Cr	-	-	5.1	-	
Viewing Angle	Θ=90	Cr≥2	41	-	-	deg
	Θ=270		38	-	-	deg
	Θ=0		32	-	-	deg
	Θ=180		19	-	-	deg

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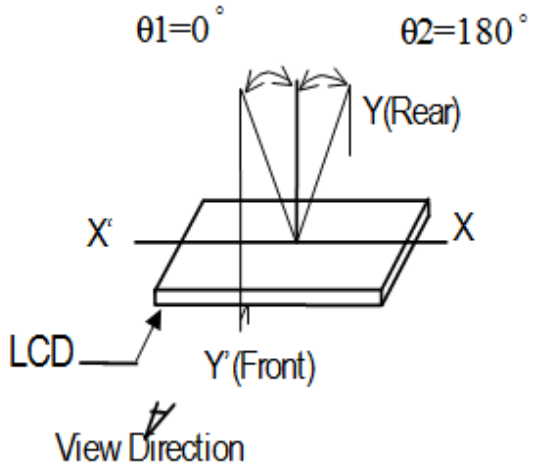
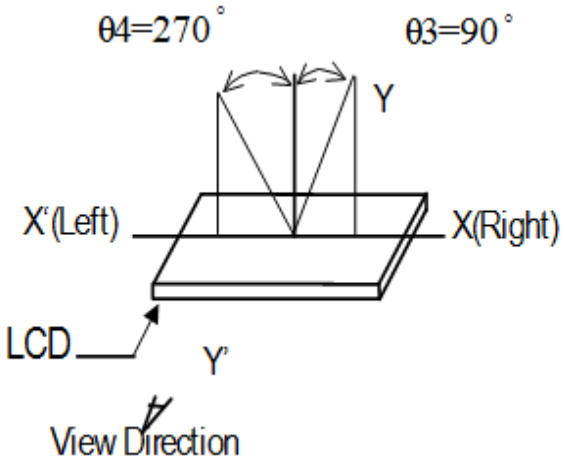
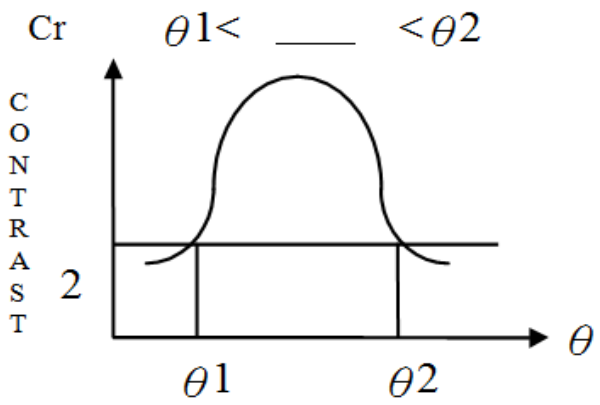
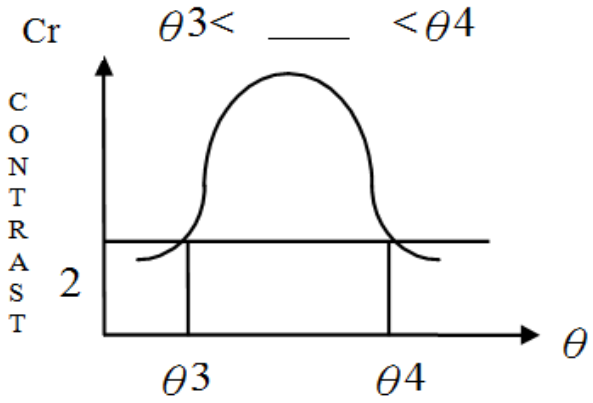
11-1 DEFINITION OF VIEWING ANGLE







Front-Rear Viewing Angle



Right-Left Viewing Angle

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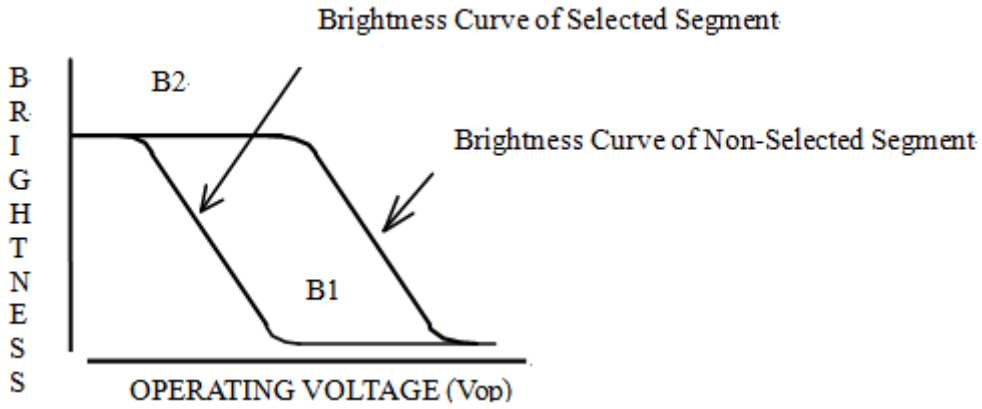
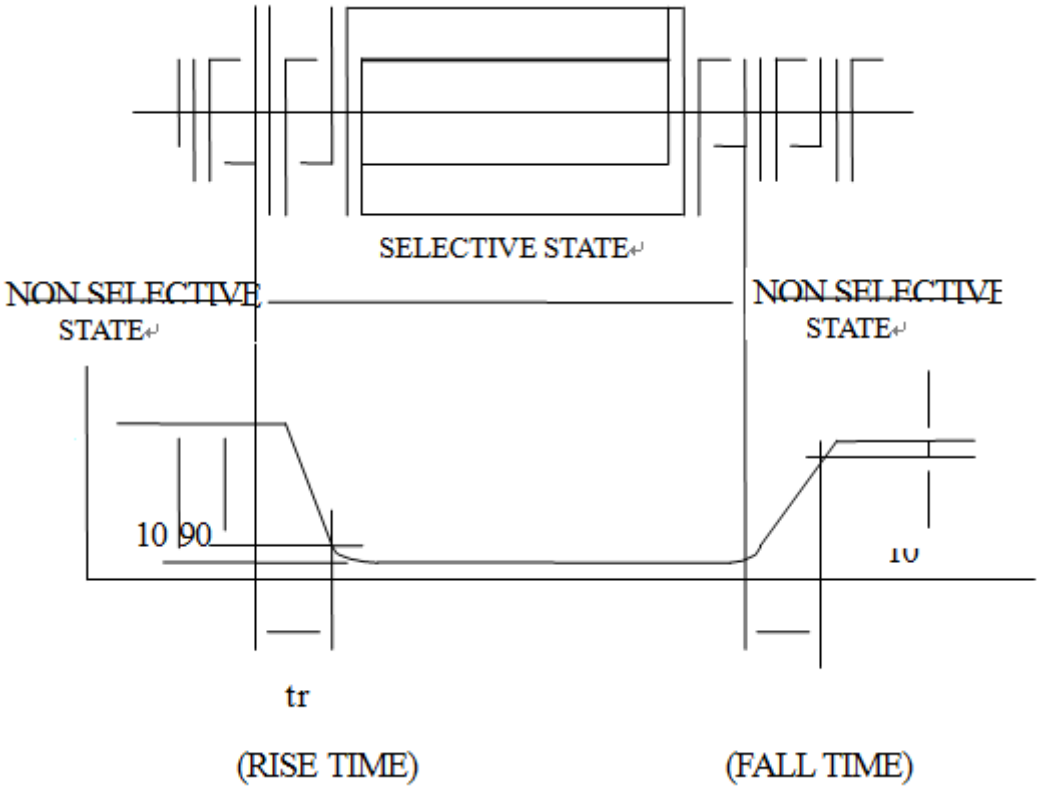
11-2 DEFINITION OF CONTRAST RATIO

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$



11-3 DEFINITION OF RESPONSE TIME



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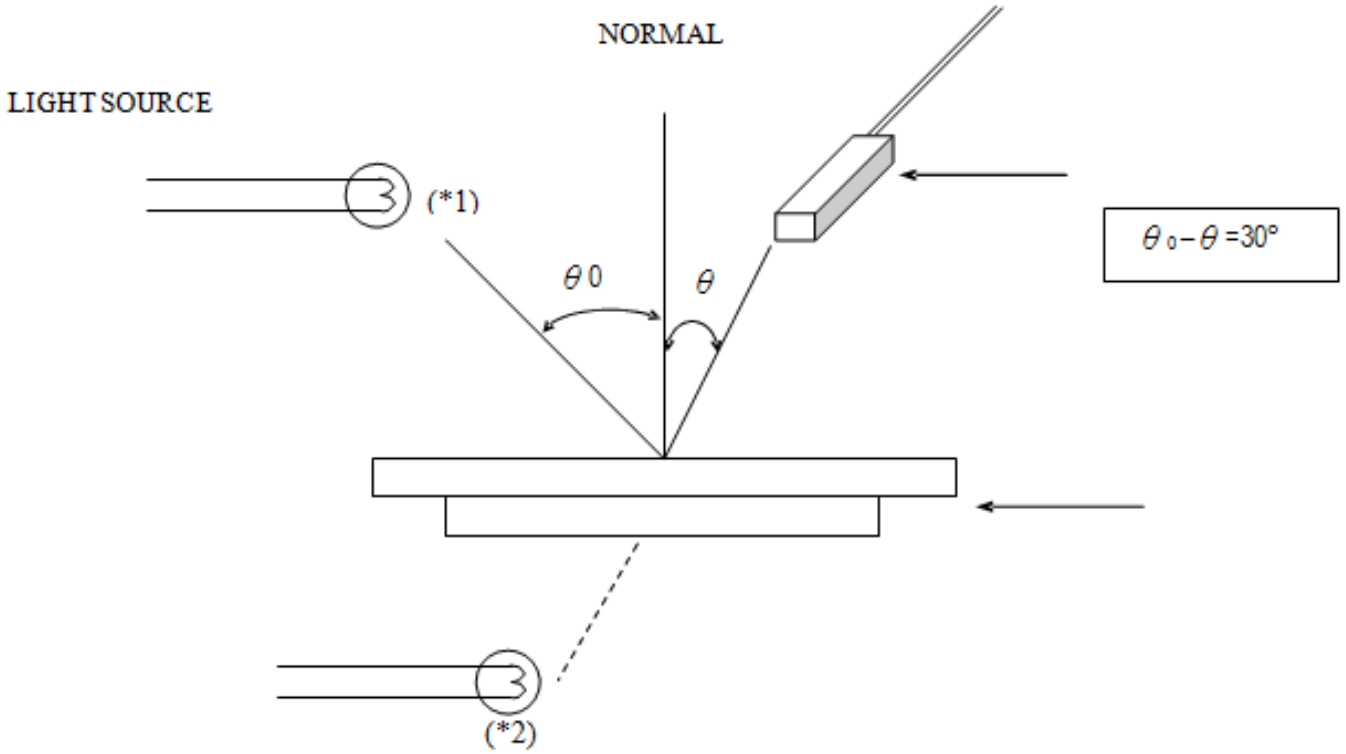
11-4 DEFINITION OF RESPONSE TIME



*1. Light source position for measuring the reflective type of LCD panel.

*2. Light source position for measuring the transflective / transmissive types of LCD panel.

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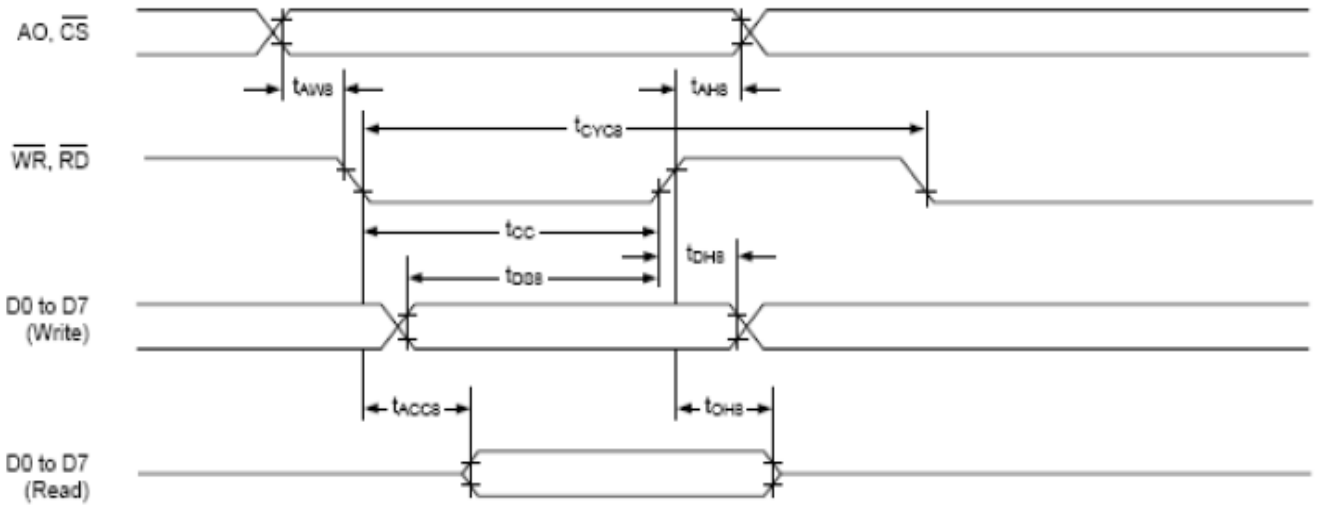
12. TIMING CHARACTERISTICS :

12-1 SED1335F Timing
12-1-1 8080 Interface Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, CS	tAH8	Address hold time	10	—	10	—	ns	CL = 100pF
	tAW8	Address setup time	0	—	0	—	ns	
WR, RD	tCYC8	System cycle time	See note.	—	See note.	—	ns	
	tCC	Strobe pulsewidth	120	—	150	—	ns	
D0 to D7	tDS8	Data setup time	120	—	120	—	ns	
	tDH8	Data hold time	5	—	5	—	ns	
	tACC8	RD access time	—	50	—	80	ns	
	tOH8	Output disable time	10	50	10	55	ns	

Note: For memory control and system control commands:

$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC8} = 4t_C + t_{CC} + 30$

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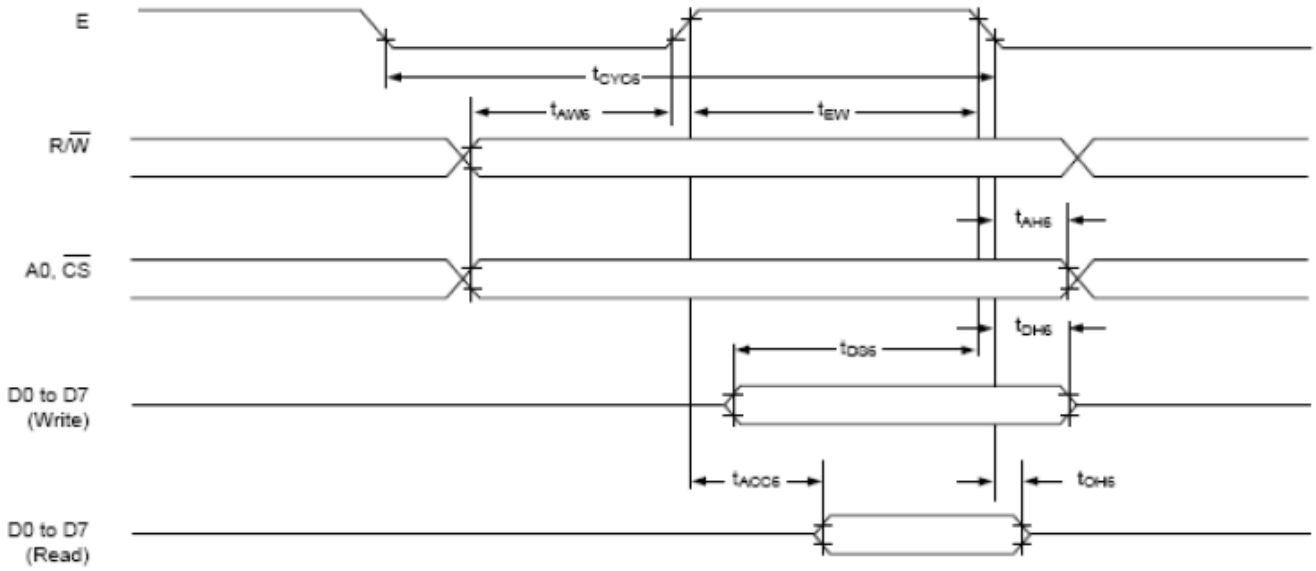
12-1-2 6800 Interface Timing



Note: t_{CYC6} indicates the interval during which CS is LOW and E is HIGH.

Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
A0, $\overline{CS}$, R/$\overline{W}$	tCYC6	System cycle time	See note.	—	See note.	—	ns	CL = 100 pF
	tAW6	Address setup time	0	—	10	—	ns	
	tAH6	Address hold time	0	—	0	—	ns	
D0 to D7	tDS6	Data setup time	100	—	120	—	ns	
	tDH6	Data hold time	0	—	0	—	ns	
	tOH6	Output disable time	10	50	10	75	ns	
	tACC6	Access time	—	85	—	130	ns	
E	tEW	Enable pulsewidth	120	—	150	—	ns	

Note: For memory control and system control commands:

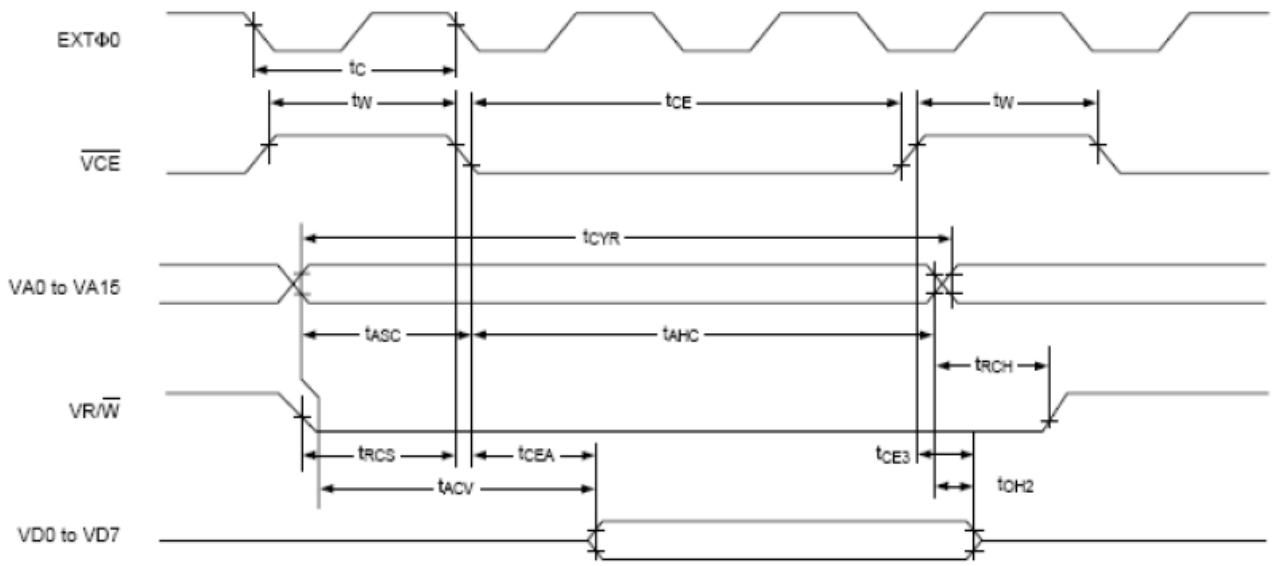
$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$

For all other commands:

$t_{CYC6} = 4t_C + t_{EW} + 30$

Free Datasheet http://www.datasheet4u.com/

12-1-3 Display Memory Read Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
$\overline{VCE}$	tW	$\overline{VCE}$ HIGH-level pulsewidth	tC – 50	—	tC – 50	—	ns	
	tCE	$\overline{VCE}$ LOW-level pulsewidth	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYR	Read cycle time	3tC	—	3tC	—	ns	
	tASC	Address setup time to falling edge of $\overline{VCE}$	tC – 70	—	tC – 100	—	ns	
	tAHC	Address hold time from falling edge of $\overline{VCE}$	2tC – 30	—	2tC – 40	—	ns	
$\overline{VRD}$	tRCS	Read cycle setup time to falling edge of $\overline{VCE}$	tC – 45	—	tC – 60	—	ns	
	tRCH	Read cycle hold time from rising edge of $\overline{VCE}$	0.5tC	—	0.5tC	—	ns	
VD0 to VD7	tACV	Address access time	—	3tC – 100	—	3tC – 115	ns	
	tCEA	$\overline{VCE}$ access time	—	2tC – 80	—	2tC – 90	ns	
	tOH2	Output data hold time	0	—	0	—	ns	
	tCE3	$\overline{VCE}$ to data off time	0	—	0	—	ns	

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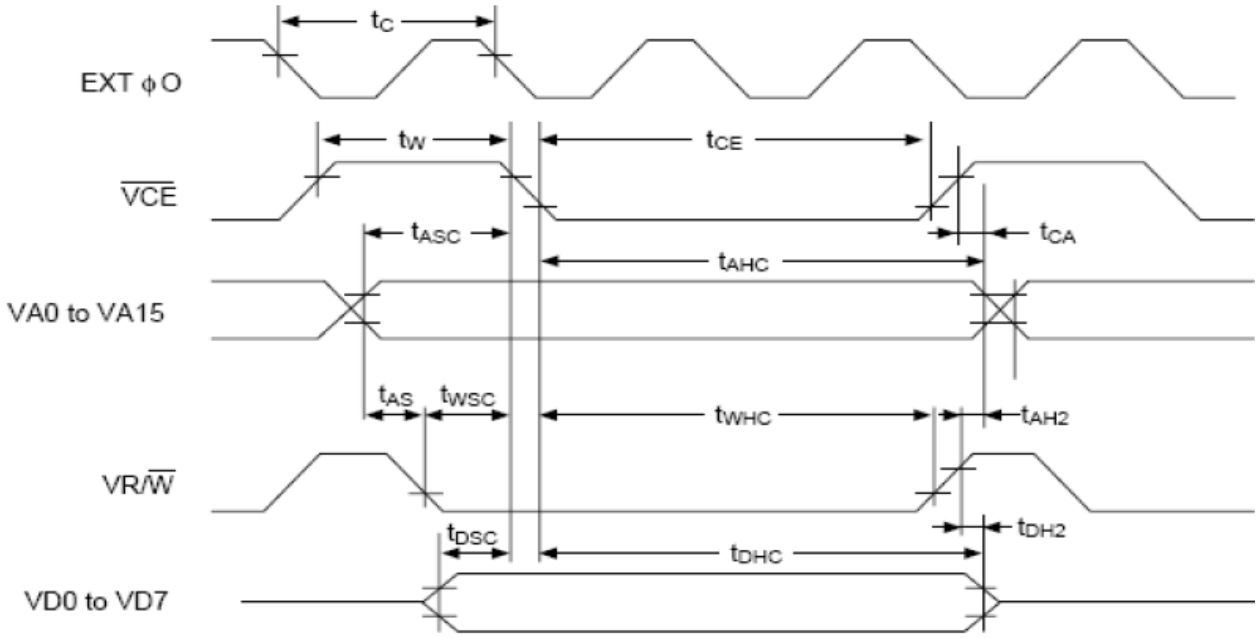
12-1-4 Display Memory Write Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
EXT ϕ0	tC	Clock period	100	—	125	—	ns	CL = 100 pF
VCE	tW	VCE HIGH-level pulsewidth	tC – 50	—	tC – 50	—	ns	
	tCE	VCE LOW-level pulsewidth	2tC – 30	—	2tC – 30	—	ns	
VA0 to VA15	tCYW	Write cycle time	3tC	—	3tC	—	ns	
	tAHC	Address hold time from falling edge of VCE	2tC – 30	—	2tC – 40	—	ns	
	tASC	Address setup time to falling edge of VCE	tC – 70	—	tC – 110	—	ns	
	tCA	Address hold time from rising edge of VCE	0	—	0	—	ns	
	tAS	Address setup time to falling edge of VWR	0	—	0	—	ns	
	tAH2	Address hold time from rising edge of VWR	10	—	10	—	ns	
VWR	tWSC	Write setup time to falling edge of VCE	tC – 80	—	tC – 115	—	ns	
	tWHC	Write hold time from falling edge of VCE	2tC – 20	—	2tC – 20	—	ns	
VD0 to VD7	tDSC	Data input setup time to falling edge of VCE	tC – 85	—	tC – 125	—	ns	
	tDHC	Data input hold time from falling edge of VCE	2tC – 30	—	2tC – 30	—	ns	
	tDH2	Data hold time from rising edge of VWR	5	50	5	50	ns	

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

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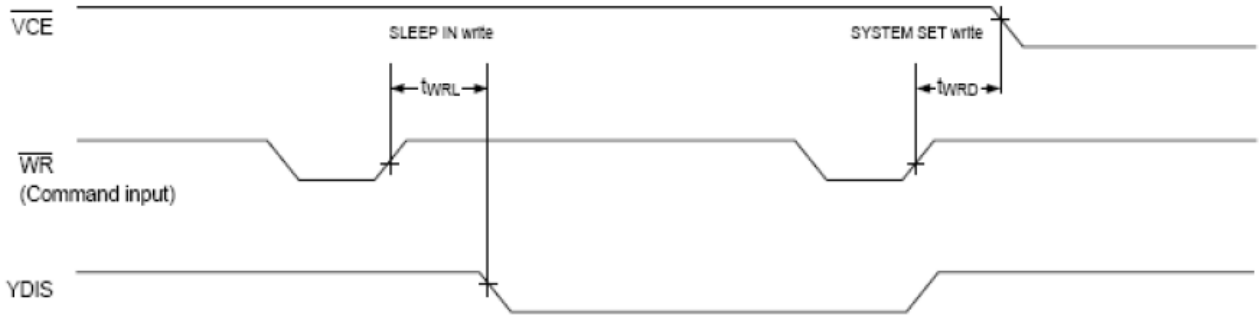
12-1-5 Sleep in Command Timing



Ta = –20 to 75°C

Signal	Symbol	Parameter	VDD = 4.5 to 5.5V		VDD = 2.7 to 4.5V		Unit	Condition
			min	max	min	max		
WR	tWRD	VCE falling-edge delay time	See note 1.	—	See note 1.	—	ns	CL = 100 pF
	tWRL	YDIS falling-edge delay time	—	See note 2.	—	See note 2.	ns	

Notes:

1. $t_{WRD} = 18t_C + t_{OSS} + 40$ (t_{OSS} is the time delay from the sleep state until stable operation)
2. $t_{WRL} = 36t_C \times [TC/R] \times [L/F] + 70$

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13. PIN ASSIGNMENT :

CN1(SED1335/RA8835)

PIN NO.	SYMBOL	I/O	FUNCTION DESCRIPTION
1	VSS	I	Ground
2	VDD	I	Power Supply for Logic(+5.0V)
3	V0	I	Power Supply for LCD Driver
4	/RD	I	Read Signal
5	/WR	I	Write Signal
6	/A0	I	Register Select Signal
7	D0	I/O	Data Bus Line
8	D1	I/O	Data Bus Line
9	D2	I/O	Data Bus Line
10	D3	I/O	Data Bus Line
11	D4	I/O	Data Bus Line
12	D5	I/O	Data Bus Line
13	D6	I/O	Data Bus Line
14	D7	I/O	Data Bus Line
15	/CS	I	Chip Select Signal
16	/RET	I	Reset Signal
17	VEE	O	DC-DC Output Voltage
18	NC	-	No Connection
19	NC	-	No Connection
20	NC	-	No Connection

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CN2

PIN NO.	SYMBOL	I/O	FUNCTION DESCRIPTION
1	K	I	Backlight Cathode Terminal (0V)
2	NC	-	No Connection
3	A	I	Backlight Anode Terminal (+3.0V)

CN3(NT7086)

PIN NO.	SYMBOL	I/O	FUNCTION DESCRIPTION
1	XD0	I	X-Driving Data
2	XD1	I	X-Driving Data
3	XD2	I	X-Driving Data
4	XD3	I	X-Driving Data
5	/DISP	I	Power Down Signal When Display is Blanked
6	FLM	I	Scan Start Pulse
7	M	I	Frame Signal
8	LP	I	Latch Pulse
9	CP	I	X-Driver Data Shift Clock
10	VDD	I	Power Supply for Logic
11	VSS	I	Ground for Logic
12	VEE	O	DC-DC Output Voltage
13	V0	I	Power Supply for LCD Drive
14	NC	-	No Connection

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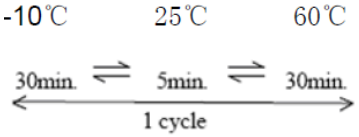
14. RELIABILITY :

ITEM	CONTENT OF TEST	CONDITION	APPLICABLE STANDARD
High Temperature Storage	Endurance test applying the high storage temperature for a long time.	70℃ 200hrs	
Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-20℃ 200hrs	
High Temperature Operation	Endurance test applying the electric stress(voltage& current) and the thermal stress to the element for a long time	60℃ 200hrs	
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	-10℃ 200hrs	
High Temperature Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time	50℃, 90RH 96hrs	MIL-202E-103B JIS-C5023
High Temperature Humidity Operation	Endurance test applying the electric stress(voltage& current) and temperature humidity stress to the element for a long time	50℃, 90RH 96hrs	MIL-202E-103B JIS-C5023
Temperature Cycle	Endurance test applying the low and high temperature cycle. 	-10℃~60℃ 10cycles	
Vibration Test	Endurance test applying the vibration during transportation and using	10-22 Hz->1.5mmp-p 22-500 Hz->1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
Shock Test	Constructional and mechanical endurance test applying the shock during transportation	50G half sign wave 1l msedc 3times of each direction	MIL-202E-213B
Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	MIL-202E-105C
Static Electricity Test	Endurance test applying the electric stress to the terminal	VS=800V, RS=1.5k CS=100Pf 1time	MIL-883B-3015.1

*NOTE : TEST CONDITION

Supply Voltage for Logic System = 3V

Supply Voltage for LCD System = 24.6V

Operating Voltage at 25℃.

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15. PRECAUTION FOR USE :

The following precaution should be followed, since this module contains precise parts.

(1) Do not store module for an extended periods of time under the conditions of high temperature and high humidity.
(2) Avoid using or storing the module in areas that expose it to direct sunlight or ultraviolet rays.
(3) Use protective finger covers when handling the module to avoid scratching or staining the module.
(4) Care should be taken not to expose the module to static electricity, because the module contains C-MOS LSI's.
(5) The LSI is sensitive to light. The user's product should be designed so that LSI is not exposed to any light during operation.
(6) During installation, cover the display area with acrylic protection plates to protect the polarizer plate and LCD cells.
(7) Do not apply any excessive shocks to the module because the module contains sensitive LCD cells. Do not use a module, which has experienced strong mechanical shock.
(8) Care should be taken when the power supply turns on as following.
   (a) Do not apply any input signals before the supplying voltage is applied.
   (b) Do not turn off the power supply while any input signals are applied.

CAUTION

(1) Dangerous. Do not shock glass because glass can break.
(2) If module breaks, do not touch it directly.
(Glass could stick or cut skin)
(3) Do not swallow Liquid Crystal.
(In case of broken LCD panel, do not swallow liquid crystal even if there is no proof that liquid crystal is poisonous)
(4) If liquid crystal is exposed to skin, wash the area thoroughly with alcohol or soap.
(5) When disposing of the product, please observe industrial waste disposal laws in each country and district.
(6) In case of injury, give immediate treatment and consult with a doctor.
(7) This product is constructed precisely. Don't disassemble or modify.

※ Neglecting this mark can cause injury to humans and damage to materials.

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