ILLUMINANT北極光企業有限公司

PRODUCT SPECIFICATION FOR TFT LCM

CUSTOMER:	
MODEL NO:	IG-G120601-6WFLWA
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
北极光 2008.07.22 贺秋芳	北极光 2008.07.22 隆茂生	北极光 2008.07.22 隆茂生

☐ Approval for Specifications Only
■ Approval for Specifications and Sample

Note: 1. Version of Specifications : 3
2. Others: Rohs Compliment

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CONTENTS

RECORDS OF REVISION

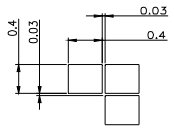
DATE	REVISED NO.	REVISED DESCRIPTIONS
2008.03.20	01	FIRST ISSUE
2008.03.24	02	ADJUST THE BL CONNECT
2008.07.22	03	ADJUST THE TIMES OF BOOSTER

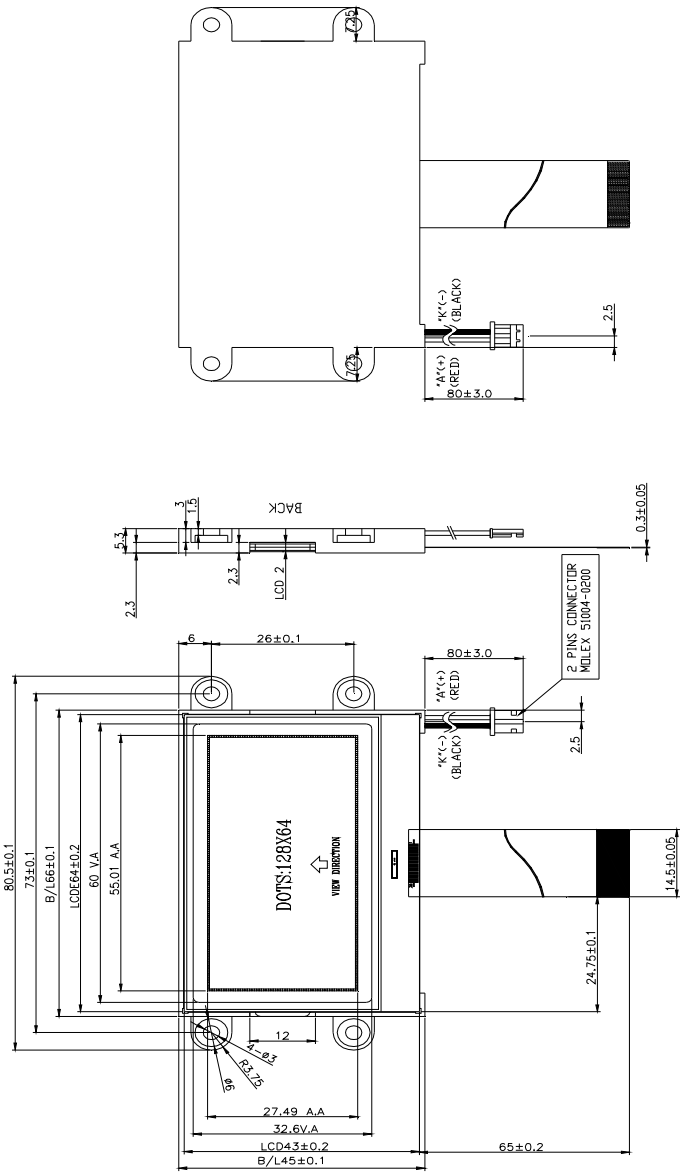
3. MECHANICAL SPECIFICATIONS :

ITEM	STANDARD VALUE	UNIT
Module Dimension	Refer to the outline drawing	mm
View Area	60.00x32.60	mm
Number of Dots	128x64 dots	dots
Dot Size	0.40x0.40	mm
Dot Pitch	0.43x0.43	mm
LCD Type	FSTN / Transflective / Positive	-
Viewing Direction	6H	-
Duty	1/65	-
Bias	1/9	-
Driver	NT7538	-
Approx. Weight	TBD	g
Backlight Color	WHITE	

4. OUTLINE DIMENSIONS :

NO	PIN	NO	PIN
1	CS1	15	VSS
2	/RES	16	VOUT
3	A0	17	CAP3+
4	WR	18	CAP1-
5	RD	19	CAP1+
6	D0	20	CAP2+
7	D1	21	CAP2-
8	D2	22	V1
9	D3	23	V2
10	D4	24	V3
11	D5	25	V4
12	D6	26	V0
13	D7	27	VR
14	VDD	28	IRS





北極光企業有限公司 ILLUMINANT	REVISION	1	IG-G120601A-6WFLW	
	CONTENT			DATE
TOLERANCE	DRAWING	he	DATE 20080310	TITLE
0~15 ±0.2 / 16~60 ±0.2 / UNIT mm	CHECK		DATE	TYPE ASSEMBLY
61~150 ±0.2 / 151~ / SCALE None	APPROVE		DATE	PAGE 1 OF 1

NOTE:
1 DISPLAY TYPE: FSTN
2 POLARIZER MODE: TRANSFLECTIVE/POSITIVE
3 VIEWING DIRECTION: 6:00
4 DRIVE METHOD: 1/65 DUTY, 1/9 BIAS
5 OPERATING VOLTAGE: 8.0 V
6 OPERATING TEMP.: -20 ~+ 70
7 STORAGE TEMP.: -30 ~+ 80
8 IC:NT7538
9 BACK LIGHT: LED (White)
10 BRIGHTNESS OF BLU: >6 cd/m2(WITH LCD)
(Vfm=3.2V(type),Ifm=90mA(max.))

5. ABSOLUTE MAXIMUM RATINGS :

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
Supply Voltage for Logic	V_{DD}-V_{SS}	-0.3	-	+3.6	V	Ta=25℃
Supply Voltage for LCD	V_{LCD}	-0.3	-	+14.2	V	Ta=25℃
Input Voltage	V_I	-0.4	-	V_{DD}+0.3	V	Ta=25℃
Operating Temperature	T_{OP}	-20	-	+70	℃	-
Storage Temperature	T_{ST}	-30	-	+80	℃	-

*NOTE : BASED ON VSS=0V.

6. ELECTRICAL CHARACTERISTICS :

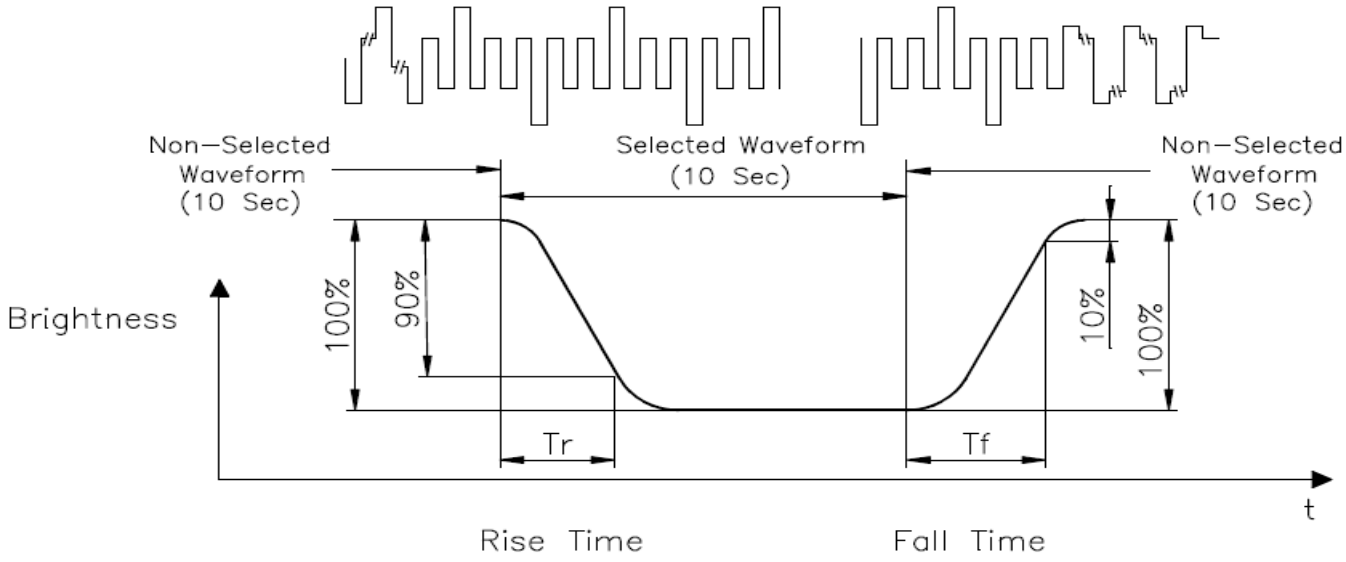
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage for Logic	V_{DD}-V_{SS}	25℃	-	3.0	-	V
Supply Voltage for LCD	V_{LCD}	25℃	-	8.0	-	V
Input High Voltage	V_{IH}	25℃	0.80V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	25℃	V_{SS}	-	0.20V_{DD}	V
Supply Current	I_{DD}	-		TBD		mA

7. OPTICAL CHARACTERISTICS :

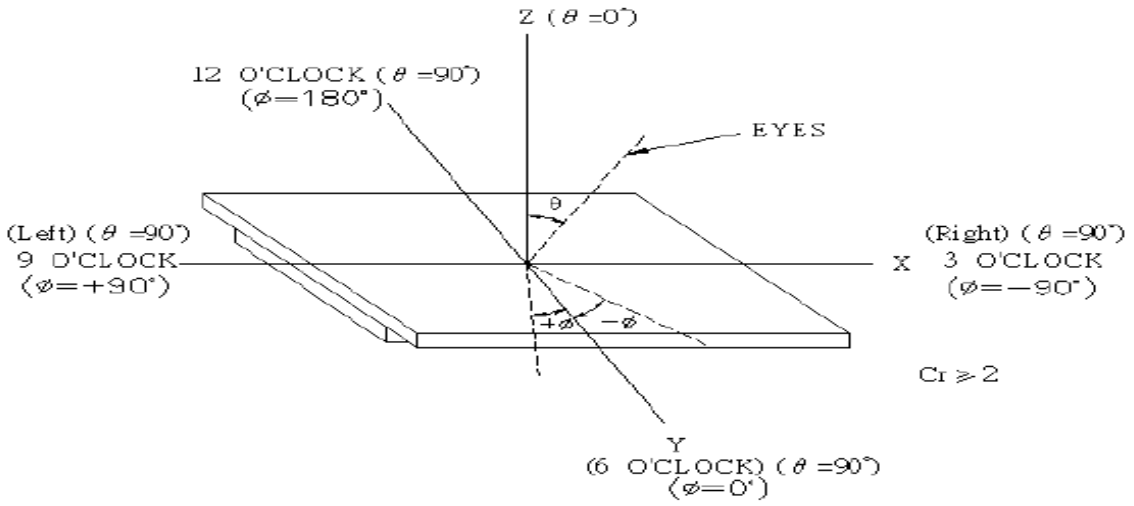
ITEM		SYMBOL	CONDITION		STANDARD VALUE			UNIT
					MIN	TYP	MAX	
Viewing Angle		θ_X	Cr≥2	θ_Y=0?	-30	-	30	Deg.
		θ_Y		θ_X=0?	-15	-	30	
Contrast Ratio		Cr	θ_X=0? θ_Y=0?		-	4	-	
Response Time	Turn On	Ton	θ_X=0? θ_Y=0?		-	250	300	ms
	Turn Off	Toff			-	250	350	

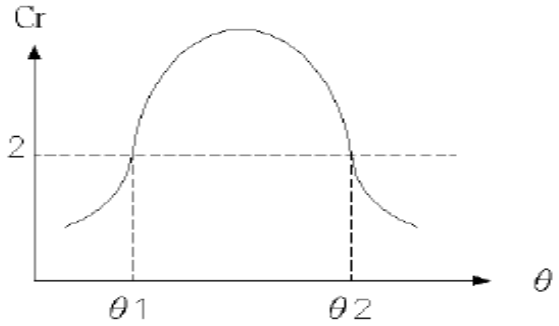
7-1 OPTICAL DEFINITIONS

*Response Time (Tr and Tf)

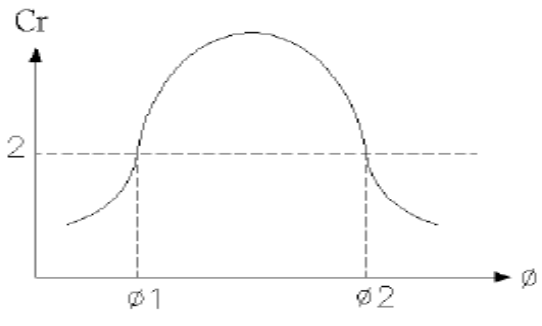


* Viewing Angle (θ)



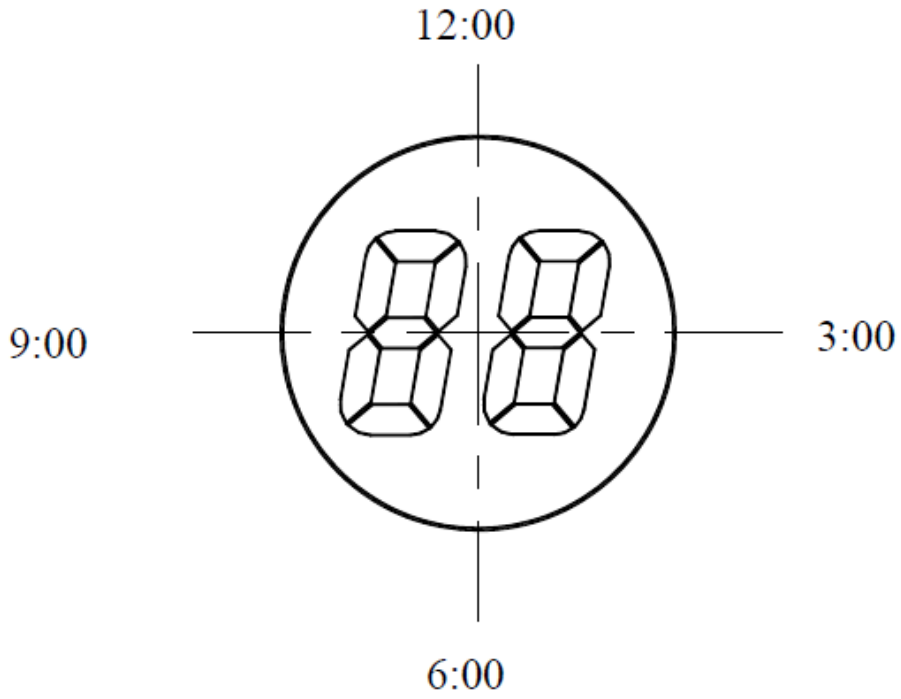


Front−Rear Viewing Angle

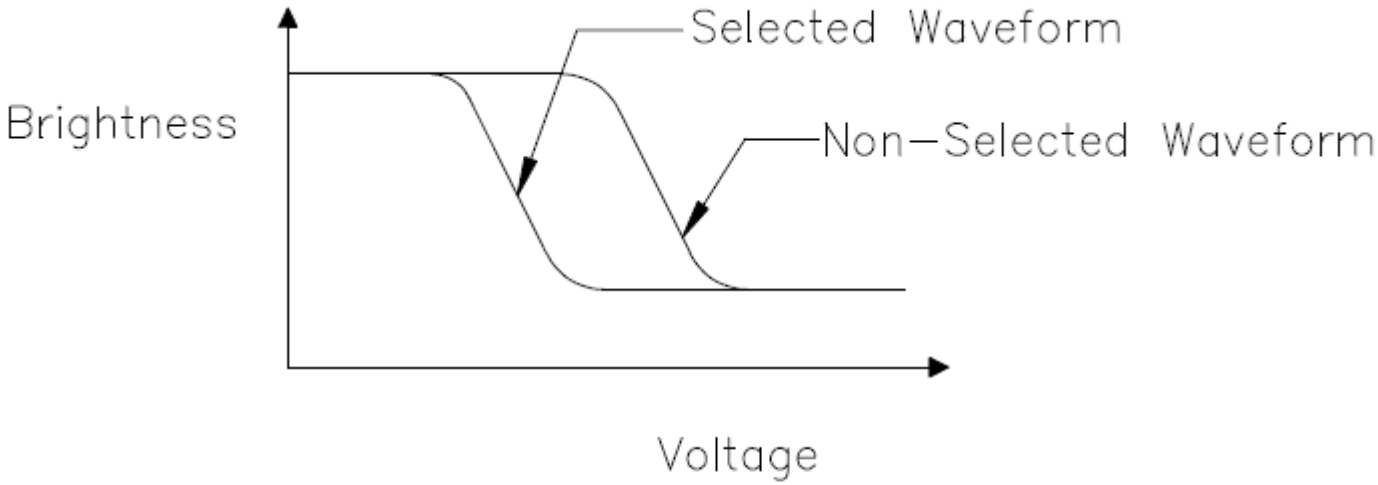


Right−Left Viewing Angle

* Definition of Viewing Direction



* Definition of Contrast Ratio (Cr)



$$\text{Contrast Ratio} = \frac{\text{Brightness of Non-Selected Waveform}}{\text{Brightness of Selected Waveform}}$$

8. INTERFACE :

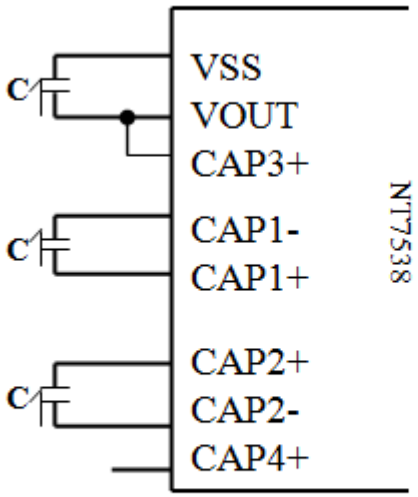
NO	SYMBOL	I/O	FUNCTION
1	/CS1	I	Chip Select Input : L Lever Active
2	/RESET	I	Reset Input Pin
3	A0	I	Control Data or Display Data Selection
4	WR	I	Write Signal
5	RD	I	Read Signal
6	DB0	I/O	Data Bus
7	DB1	I/O	Data Bus
8	DB2	I/O	Data Bus
9	DB3	I/O	Data Bus
10	DB4	I/O	Data Bus
11	DB5	I/O	Data Bus
12	DB6	I/O	Data Bus
13	DB7	I/O	Data Bus
14	VDD	P	Power Supply for Logic
15	VSS	P	Signal Ground (GND)
16	VOUT	P	Voltage Converter Out Pin
17	CAP3+	I	Capacitor 3+ connected to the internal voltage converter
18	CAP1-	I	Capacitor 1- connected to the internal voltage converter
19	CAP1+	I	Capacitor 1+ connected to the internal voltage converter
20	CAP2+	I	Capacitor 2+ connected to the internal voltage converter
21	CAP2-	I	Capacitor 2- connected to the internal voltage converter
22	V1	P	LCD Driver Power Supply Voltages
23	V2	P	LCD Driver Power Supply Voltages
24	V3	P	LCD Driver Power Supply Voltages
25	V4	P	LCD Driver Power Supply Voltages
26	V0	P	LCD Driver Power Supply Voltages
27	VR	P	Voltage Adjustment Pin
28	IRS	P	The Terminal Select the Resistors for the V0 Voltage Level Adjustment

9. INSTRUCTION TABLE :

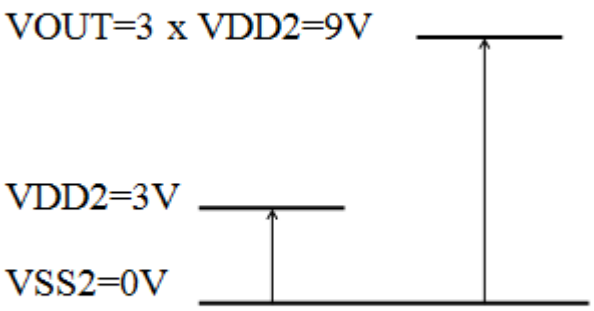
Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h To 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h To B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h To 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10) Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12) Read_Modify_Write	0	1	0	1	1	1	0	0	0	0	0	Eoh	Increments column address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read_Modify_Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15) Common Output Mode Select	0	1	0	1	1	0	0	0 1	.	.	.	Coh To CFh	Select COM output scan direction : invalid data
(16) Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h To 2Fh	Select the power circuit operation mode
(17) V0 Voltage Regulator internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h To 27h	Select internal resistor ratio Rb/Ra mode
(18) Electronic Volume mode set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	.	.	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(19) Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1:ON
Set Static indicator Register	0	1	0	.	.	.	.	.	.	Mode		XX	Sets the flash mode
(20) Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22) Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23) Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24) Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25) Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26) Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27) N-Line inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	.	.	.	Number of Line					XX	Sets the number of line used for N-Line inversion
(28) N-Line inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line inversion
(29) DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30) Test Command	0	1	0	1	1	1	1	.	.	.	.	F1h to FFh	IC test command. Do not use
(31) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

10. RECOMMEND POWER SUPPLY CIRCUIT :



3x step-up voltage circuit



3x step-up voltage relationships

11. BACKLIGHT :

11.1 STANDARD LAMP STYLES (EDGE LIGHTING TYPE)

The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

11.2 THE MAIN ADVANTAGES OF THE LED BACKLIGHT ARE AS FOLLOWING

The brightness of the backlight can simply be adjusted by a resistor or a potentiometer.

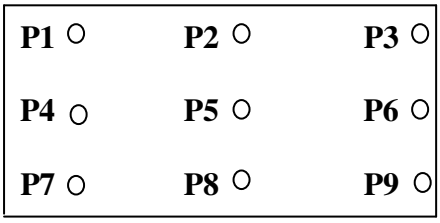
11.3 DATA ABOUT LED BACKLIGHT

ITEM	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply for LED BACKLIGHT	VLED	-	-	3.2	-	V
Power supply current for BL	ILED	VLED=3.2V	-	90	120	mA
Uniformity	-	If ILED =90	70%	-	-	-
Luminous color	-	White				

NOTE:

1.Backlight Only
2.Average Luminous Intensity of P1-P9
3.Uniformity = Min(P1~P9)/Max(P1~P9) * 100%>80%

11.4 MEASURED METHOD



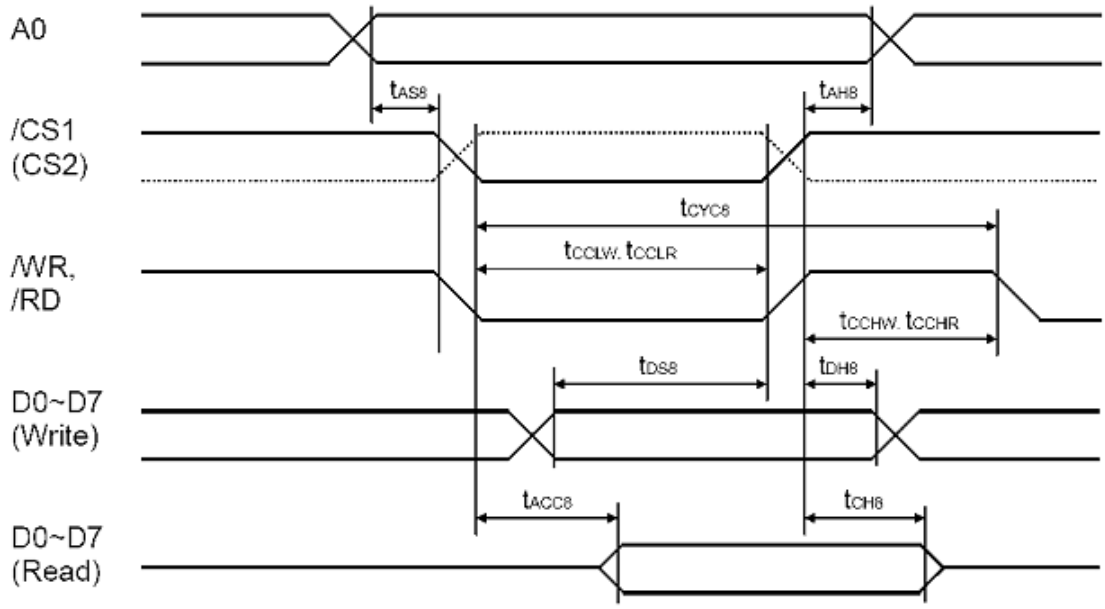
(Effective spatial Distribution)

Hole Diameter±1ø ; 1 to 9per Position Measured Luminous

12. TIMING CHARACTERISTICS :

12.1 PARALLEL BUS TIMING CHARACTERISTICS (FOR 8080MCU)

* System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0	-	-	ns	A0
T_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	240	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	/RD
T_{DS8}	Data setup time	40	-	-	ns	D0~D7
T_{DH8}	Data hold time	0	-	-	ns	
t_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{CH8}	Output disable time	5	-	50	ns	

* System Buses Read/Write Characteristics (for 8080 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH8}	Address hold time	0	-	-	ns	A0
t_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	400	-	-	ns	
t_{CCLW}	Control low pulse width (write)	150	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	150	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	120	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	120	-	-	ns	/RD
t_{DS8}	Data setup time	80	-	-	ns	D0~D7
t_{DH8}	Data hold time	0	-	-	ns	
t_{ACC8}	/RD access time	-	-	240	ns	D0~D7, CL = 100pF
t_{CH8}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (tr,tf) is specified at 15ns or less.
(tr+tf) < (t_{CYC8} - t_{CCLW} -t_{CCHW}) for write, (tr+tf) < (t_{CYC8} - t_{CCLR} -t_{CCHR}) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.