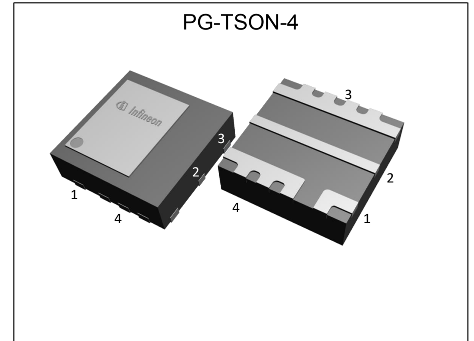
CoolGaN™ Transistor 100 V G3



Features

- Enhancement mode power transistor - normally OFF switch
- No reverse recovery charge
- Reverse conduction capability
- Low gate charge, low output charge
- Qualified according to JEDEC for target applications

Potential applications

- Telecom AC/DC Synchronous Rectifiers
- Telecom DC/DC Synchronous Rectifiers
- Robotics
- Battery powered tool
- e-Mobility, UAVs
- Wireless charging
- ClassD Audio

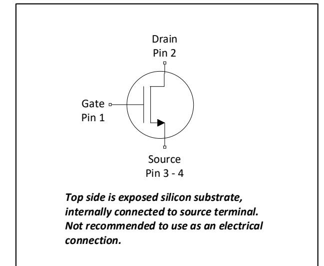


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Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	11	mΩ
I_D	24	A
Q_{oss}	14	nC
Q_G	3.4	nC
Q_{rr}	0	nC

Type / Ordering Code	Package	Marking	Related Links
IGB110S10S1	PG-TSON-4	BA1	-

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1 Maximum ratings

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	V_{GS}=0 V
Pulsed drain-source voltage[1]	$V_{DS,\ pulse}$	-	-	120	V	V_{GS}=0 V, 1 h total time
Continuous drain current	I_D	- -	- -	24 10	A	V_{GS}=5 V, T_C=25 °C V_{GS}=5 V, T_A=25 °C, R_{THJA}=50 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	- -	- -	80 40	A	T_j=25 °C T_j=150 °C
Gate-source voltage	V_{GS}	-4 -6.5	5 -	5.5 6.5	V	Continuous Pulsed
Power dissipation	P_{tot}	- -	- -	15 2.5	W	T_C=25 °C T_A=25 °C, R_{THJA}=50 °C/W
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating temperature	T_j	-40	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	$R_{thJC(top)}$	-	1.4	1.7	°C/W	-
Thermal resistance, junction - case, bottom	$R_{thJC(bottom)}$	-	5.6	8.4	°C/W	-
Device on 1 layer PCB	R_{thJA}	-	71	80	°C/W	1s0p
Device on 4 layer PCB	R_{thJA}	-	50	-	°C/W	2s2p with vias

[1] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation
[2] Device on 4-layer FR4 PCB, vertical in still air.
[3] Pulse current limited by transfer characteristic. See diagram 6.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage[1]	$V_{GS(th)}$	1.2	2.0	2.9	V	V_{DS}=V_{GS}, I_D=3 mA, measured within 5 ms after a pre-bias at V_{GS}=5 V, V_{DS}=0 V for at least 5 ms
Drain-source leakage current	I_{DSS}	- -	0.1 20	10 250	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	- - - -	7.6 0.01 53 15	- - - -	µA	V_{GS}=5 V, T_j=25 °C V_{GS}=-4 V, T_j=25 °C V_{GS}=5 V, T_j=125 °C V_{GS}=-4 V, T_j=125 °C
Drain-source on-state resistance[2]	$R_{DS(on)}$	-	8	11	mΩ	V_{GS}=5 V, I_D=10 A
Gate resistance[3]	R_G	-	1.2	-	Ω	-

Table 5 Dynamic characteristics[3]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	390	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance	C_{oss}	-	160	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	2.7	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz

Table 6 Gate charge characteristics[4]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.1	-	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Gate charge at threshold	$Q_{g(th)}$	-	0.8	-	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Gate to drain charge[3]	Q_{gd}	-	0.7	-	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Switching charge	Q_{sw}	-	1.0	-	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Gate charge total[3]	Q_g	-	3.4	-	nC	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Gate plateau voltage	$V_{plateau}$	-	2.7	-	V	V_{DD}=50 V, I_D=10 A, V_{GS}=0 to 5 V
Output charge[3]	Q_{oss}	-	14	-	nC	V_{DD}=50 V, V_{GS}=0 V

[1] When tested without the specified V_{GS} pre-bias, $V_{GS(th)}$ will typically be 0.7 V lower than the threshold voltage measured under the specified conditions.
[2] $R_{DS(ON)}$ is measured without prior drain bias or switching stress. An upcoming application note will provide detailed information about dynamic $R_{DS(ON)}$ and recommendations for *in situ* measurement in target application conditions.
[3] Defined by design. Not subject to production test.
[4] See "Gate charge waveforms" for parameter definition

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Table 7 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	4	A	T_C=25 °C
Pulsed current, reverse	$I_{S,pulse}$	-	-	80	A	T_C=25 °C
Source-Drain reverse voltage	V_{SD}	-	2.5	3.4	V	V_{GS}=0 V, I_{Sp}ulse=10 A, T_j=25 °C
Reverse recovery charge[1)]	Q_{rr}	-	0	-	nC	V_R=50 V, $I_{S,pulse}$=10 A, $di_{S,pulse}/dt$=100 A/µs

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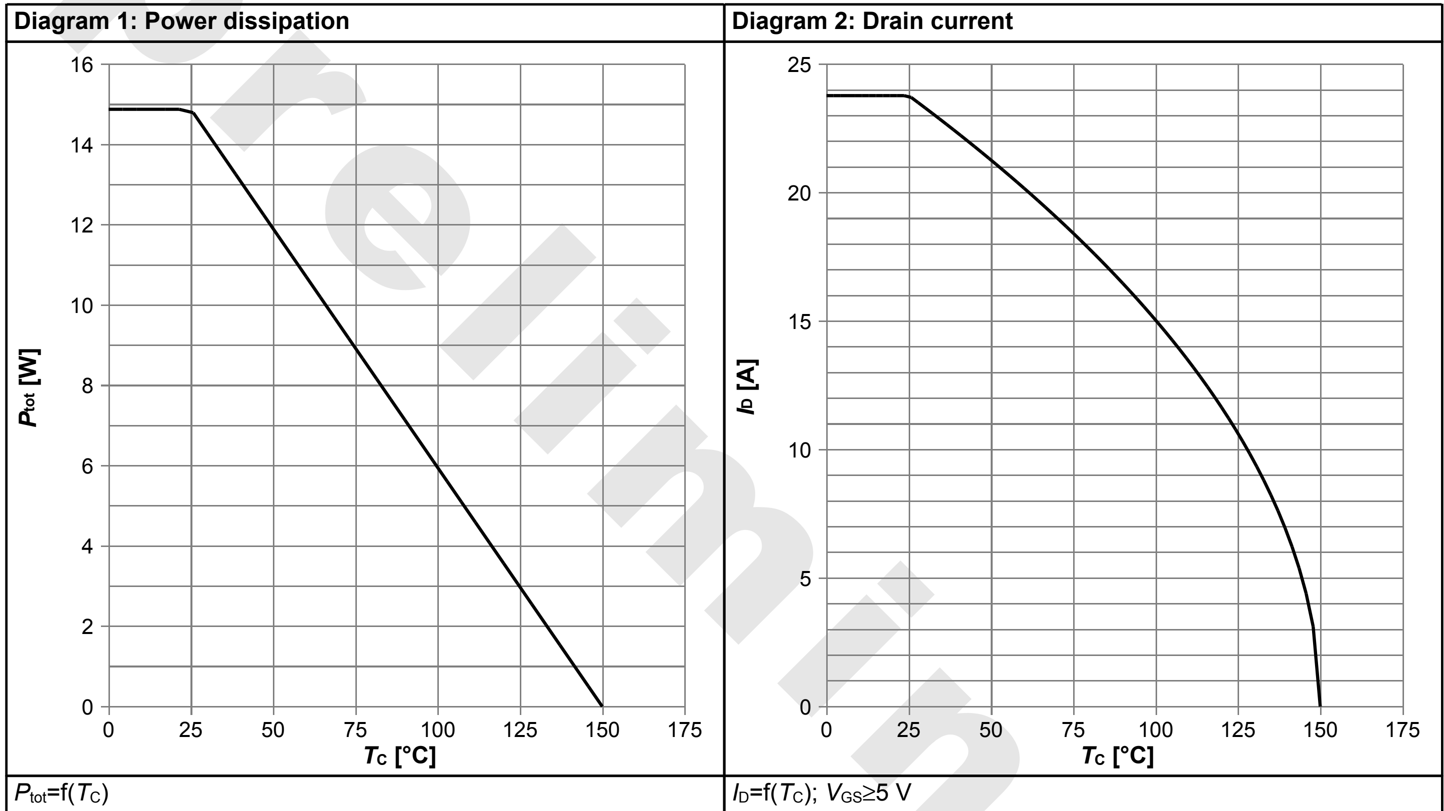
[1)] Defined by design. Not subject to production test.

4 Electrical characteristics diagrams



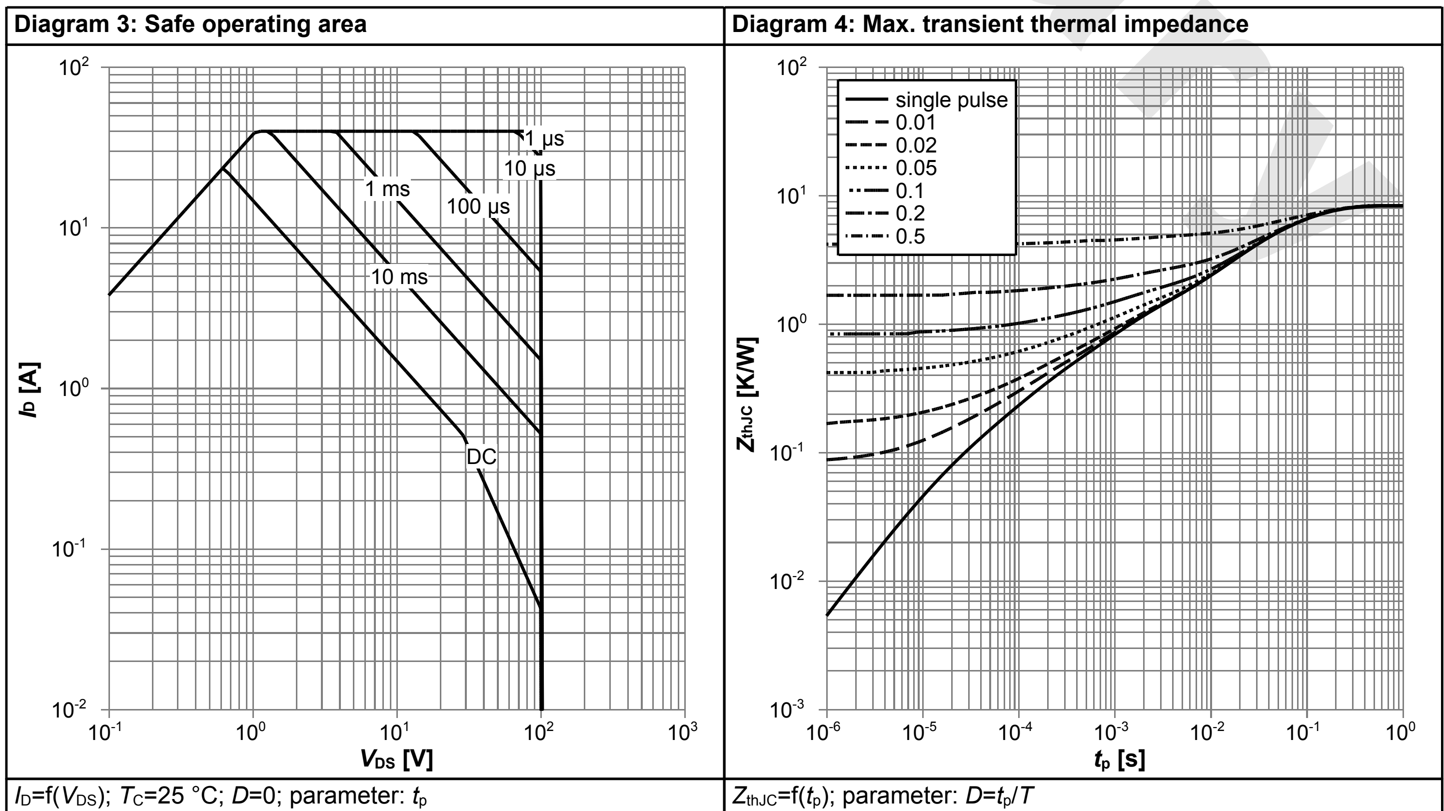


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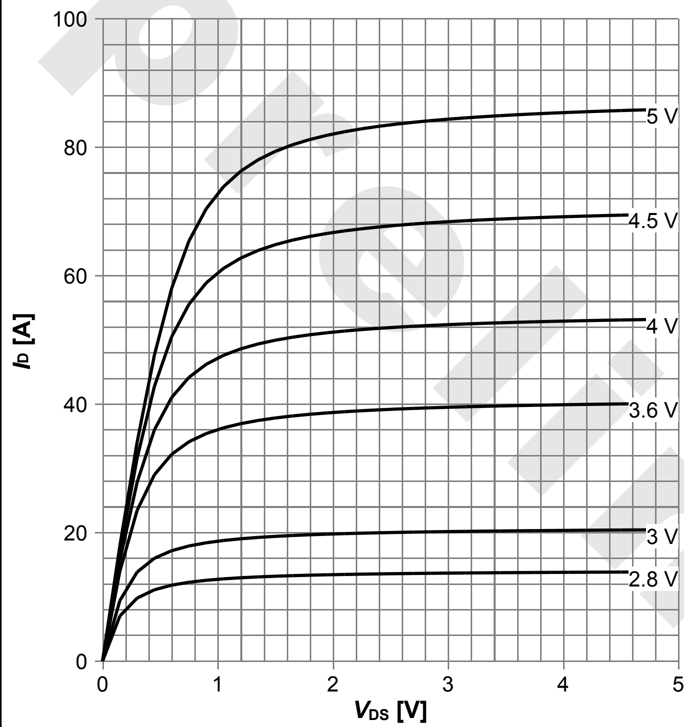
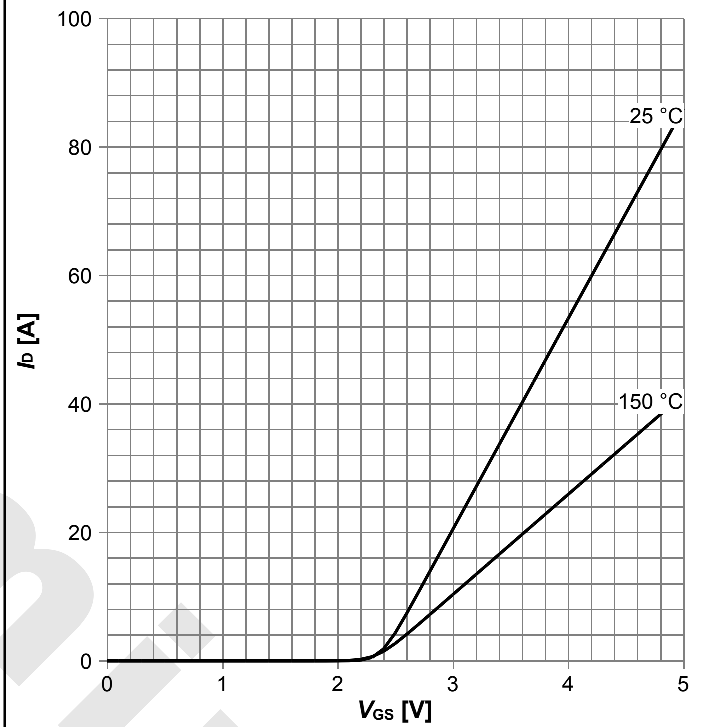
Diagram 5: Typ. output characteristics	Diagram 6: Typ. transfer characteristics
	
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}	I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

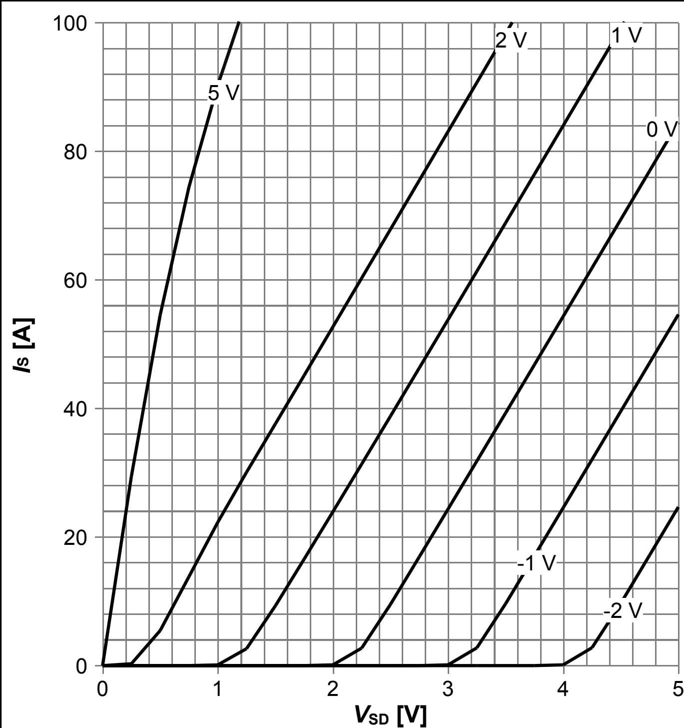
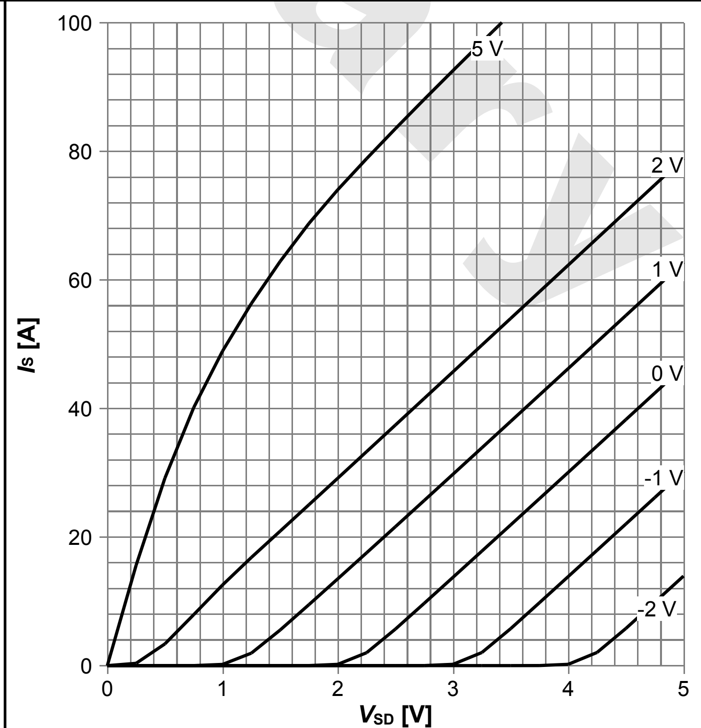
Diagram 7: Typ. reverse output characteristics	Diagram 8: Typ. reverse output characteristics
	
I_F=f(V_{SD}), T_j=25 °C; parameter: V_{GS}	I_F=f(V_{SD}), T_j=125 °C; parameter: V_{GS}

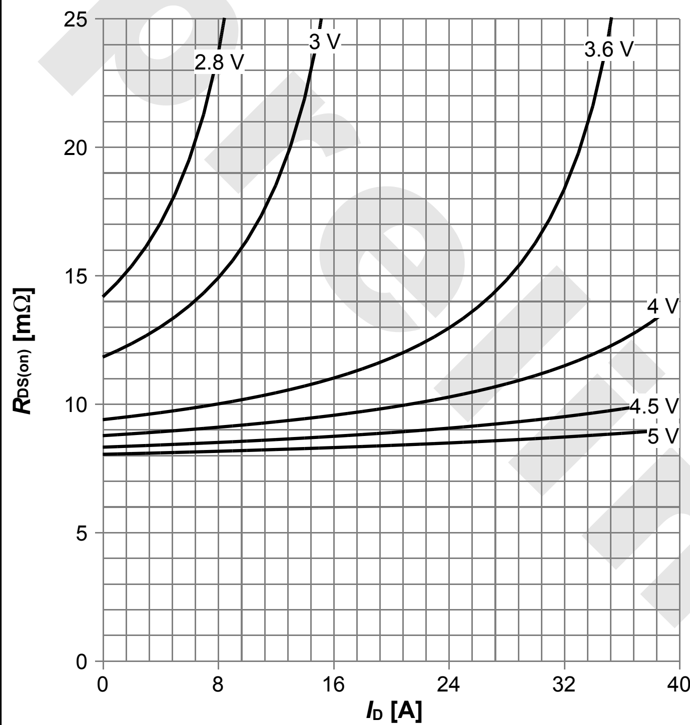
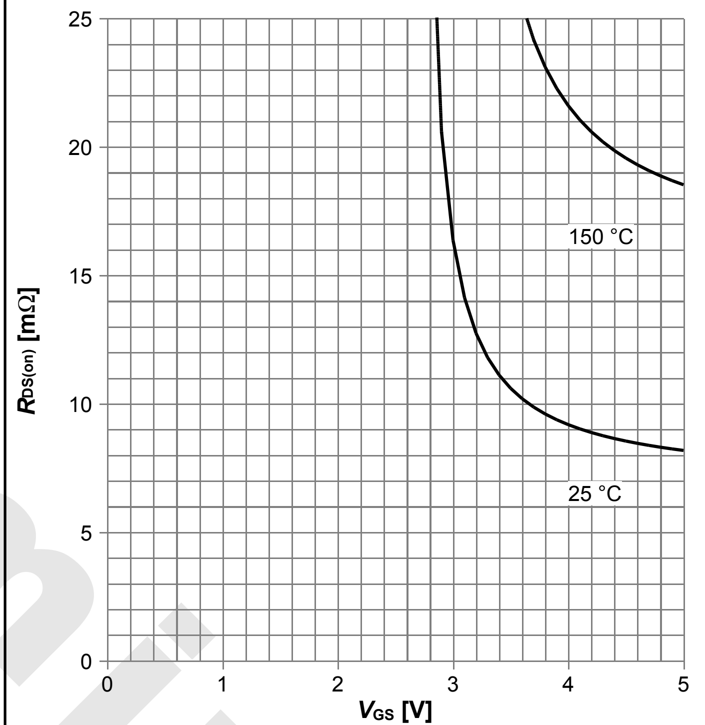
Diagram 9: Typ. drain-source on resistance	Diagram 10: Typ. drain-source on resistance
	
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(V_{GS}), I_D=10 A; parameter: T_j

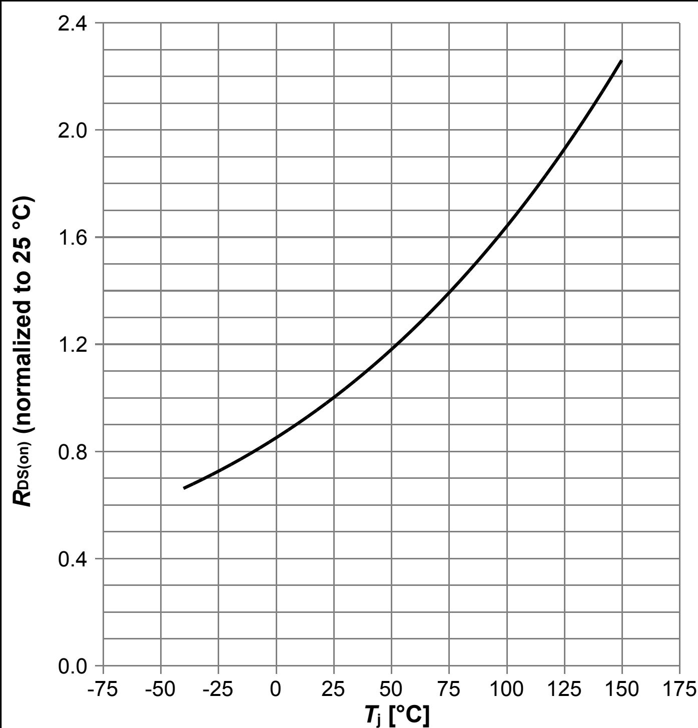
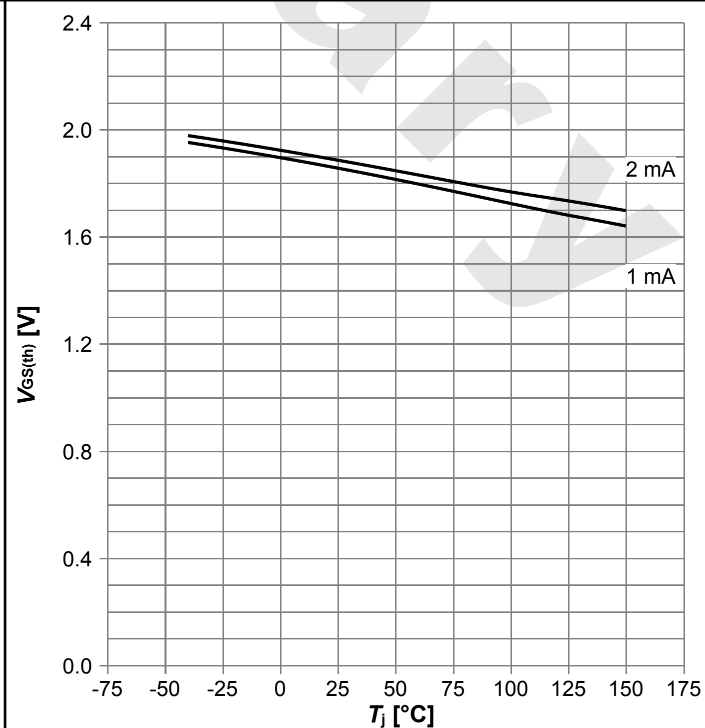
Diagram 11: Normalized drain-source on resistance	Diagram 12: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=10 A, V_{GS}=5 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

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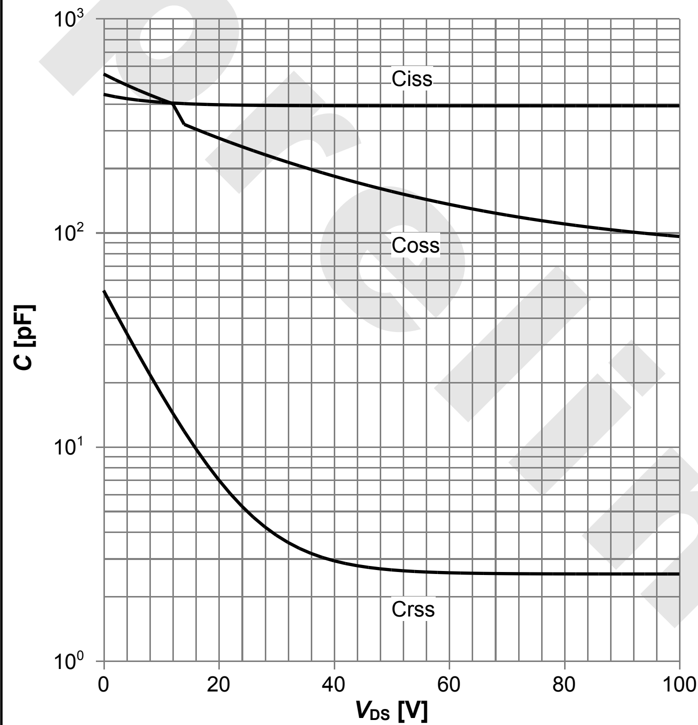
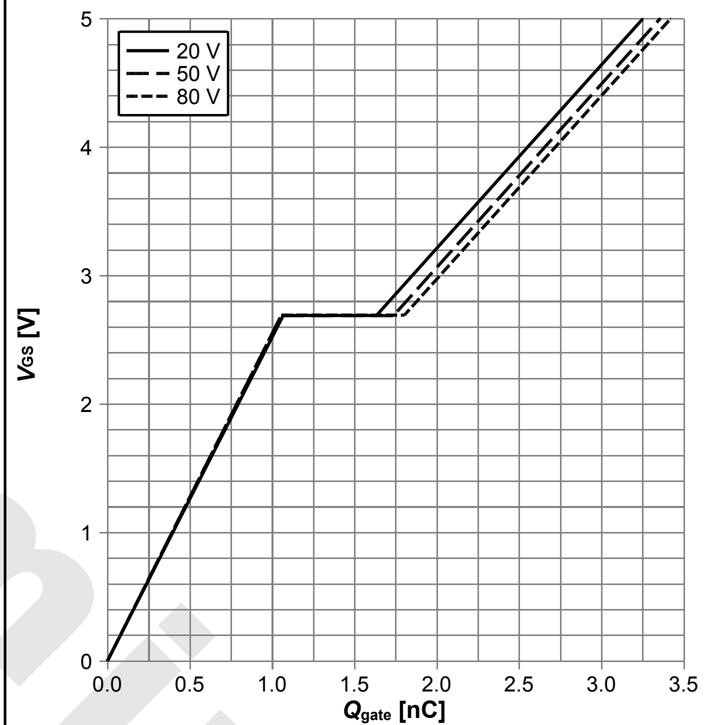
Diagram 13: Typ. capacitances



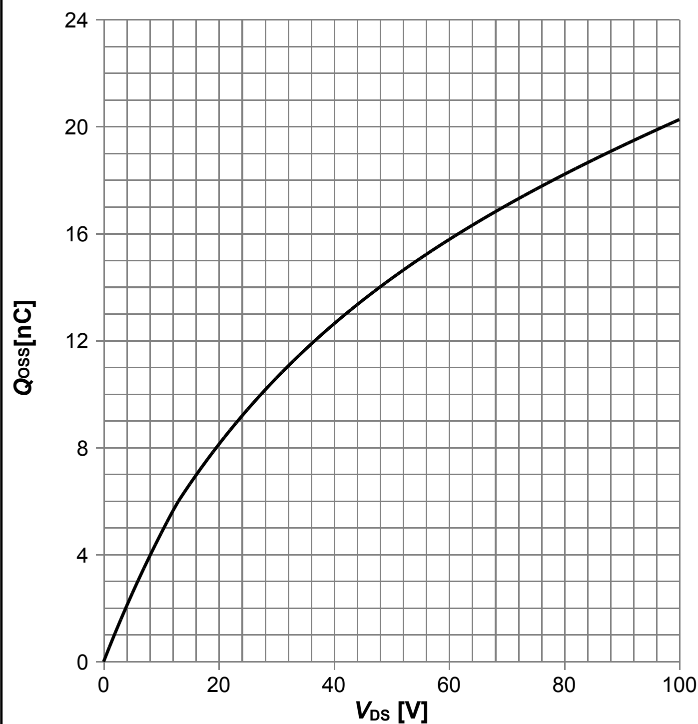
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 14: Typ. gate charge



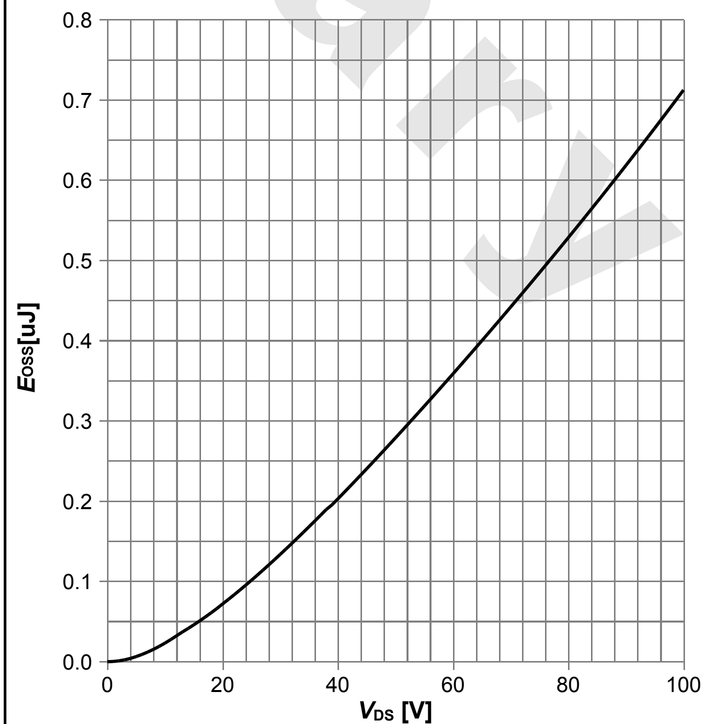
V_{GS}=f(Q_{gate}), I_D=10 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Typ output charge



Q_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 16: Typ output energy



E_{oss}=f(V_{DS}), V_{GS}=0 V

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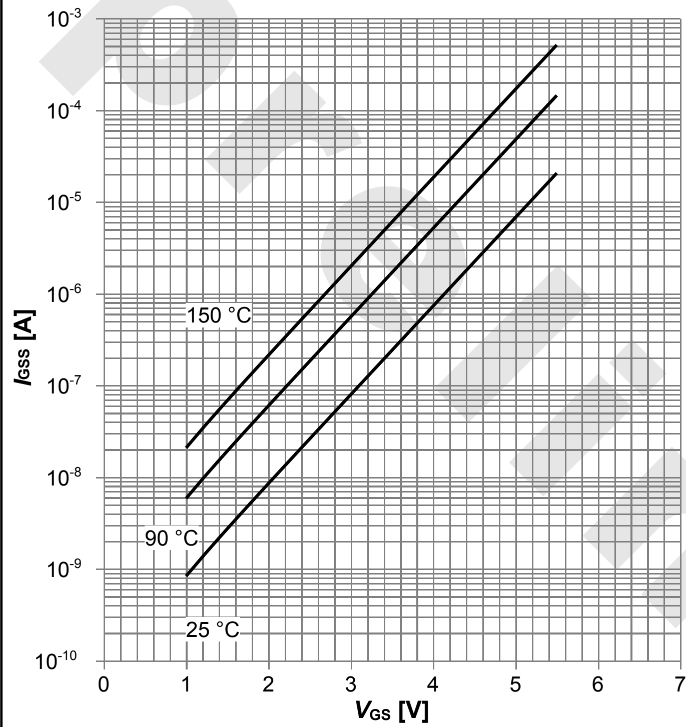
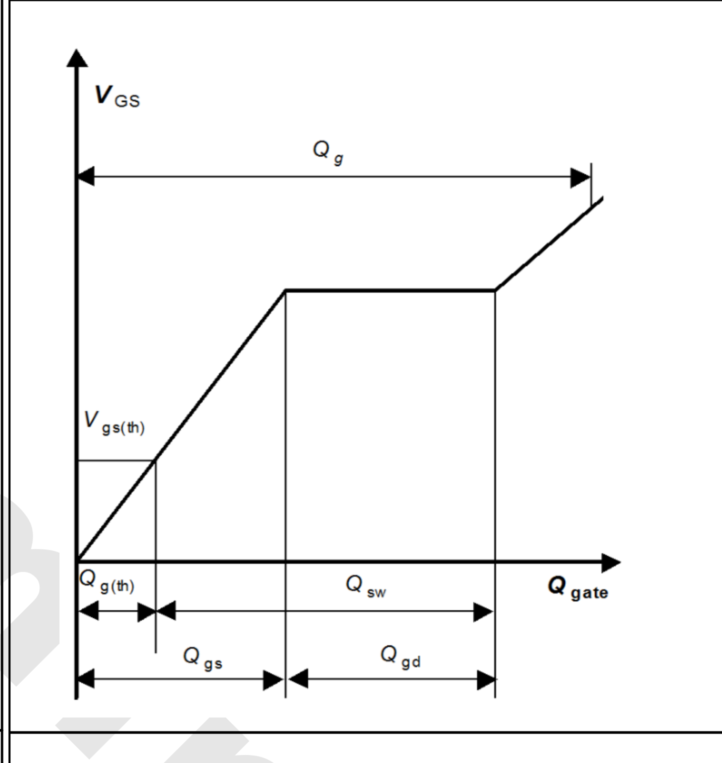
Diagram 17: Typ gate-source leakage current	Diagram Gate charge waveforms
	
I_{GSS}=f(V_{GS}), V_{DS}=0 V; parameter: T_j	

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5 Package Outlines

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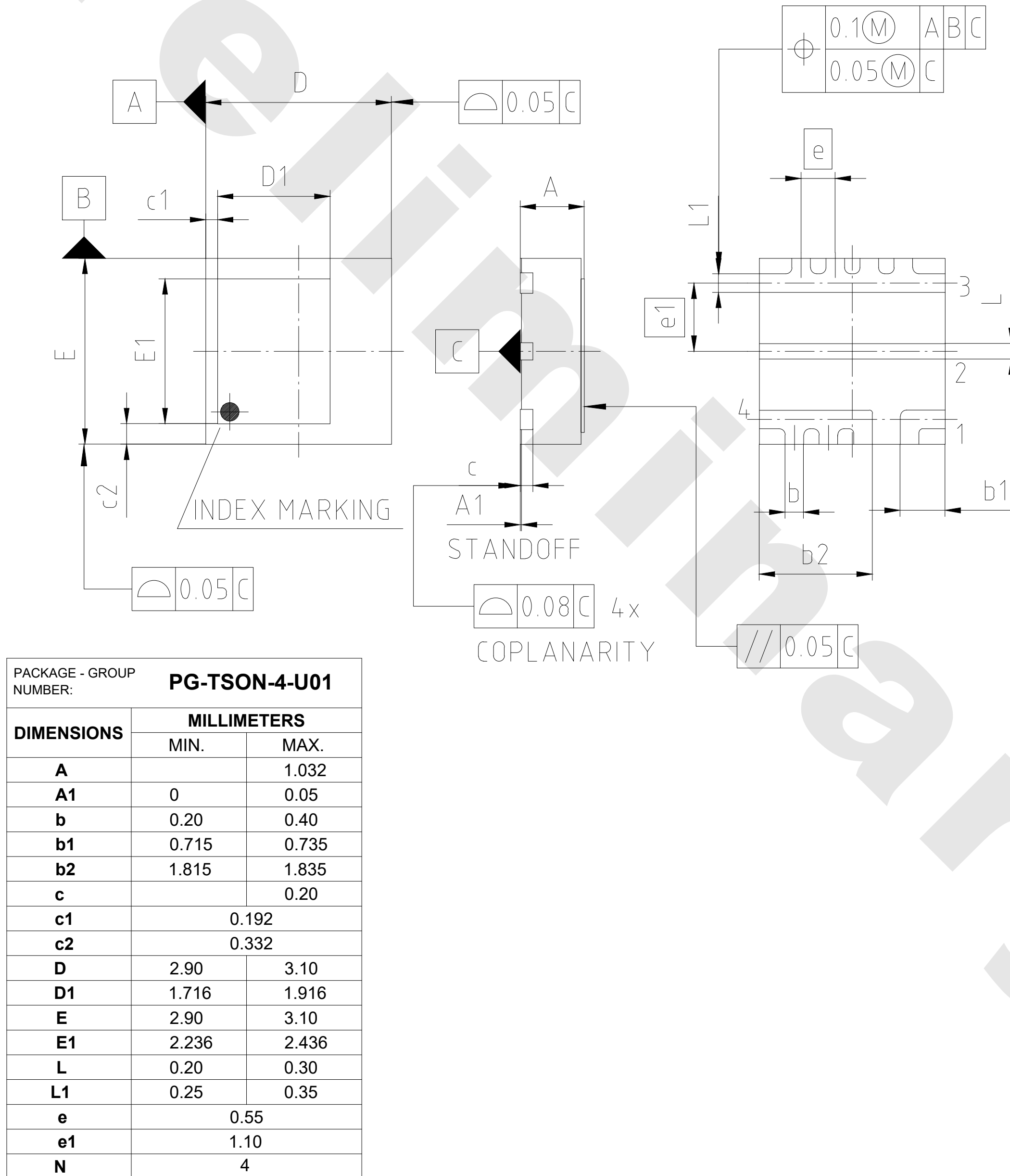

PACKAGE - GROUP NUMBER:	PG-TSON-4-U01	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A		1.032
A1	0	0.05
b	0.20	0.40
b1	0.715	0.735
b2	1.815	1.835
c		0.20
c1	0.192	
c2	0.332	
D	2.90	3.10
D1	1.716	1.916
E	2.90	3.10
E1	2.236	2.436
L	0.20	0.30
L1	0.25	0.35
e	0.55	
e1	1.10	
N	4	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-TSON-4, dimensions in mm

Revision History

IGB110S10S1		
Revision: 2024-05-20, Rev. 0.9		
Previous Revision		
Revision	Date	Subjects (major changes since last revision)
0.9	-	Release of preliminary version

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