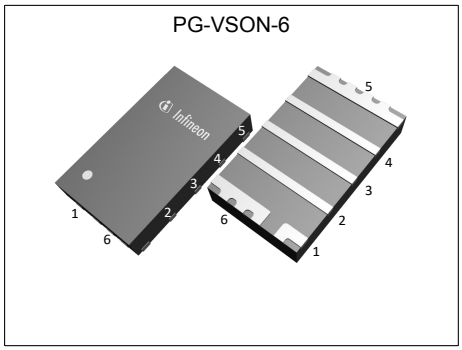
CoolGaN™ Transistor 100 V G3

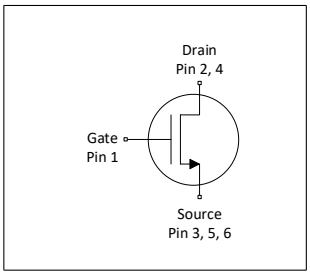


Features

- Enhancement mode power transistor - normally OFF switch
- No reverse recovery charge
- Reverse conduction capability
- Low gate charge, low output charge
- Qualified according to JEDEC for target applications

Potential applications

- Telecom AC/DC Synchronous Rectifiers
- Telecom DC/DC Synchronous Rectifiers
- Robotics
- Battery powered tool
- e-Mobility, UAVs
- Wireless charging
- ClassD Audio



RoHS

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	3.3	mΩ
I_D	75	A
Q_{oss}	49	nC
Q_G	11	nC
Q_{rr}	0	nC

Type / Ordering Code	Package	Marking	Related Links
IGC033S101	PG-VSON-6	33SA1	-

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1 Maximum ratings

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain-source voltage	V_{DS}	-	-	100	V	V_{GS}=0 V
Pulsed drain-source voltage[1)]	$V_{DS,\ pulse}$	-	-	120	V	V_{GS}=0 V, 1 h total time
Continuous drain current	I_D	- -	- -	75 20	A	V_{GS}=5 V, T_C=25 °C V_{GS}=5 V, T_A=25 °C, R_{THJA}=38 °C/W[2)]
Pulsed drain current[3)]	$I_{D,pulse}$	- -	- -	240 100	A	T_j=25 °C T_j=150 °C
Gate-source voltage	V_{GS}	-4 -6.5	5 -	5.5 6.5	V	Continuous Pulsed
Power dissipation	P_{tot}	- -	- -	45 3.3	W	T_C=25 °C T_A=25 °C, R_{THJA}=38 °C/W
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating temperature	T_j	-40	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, top	$R_{thJC(top)}$	-	15	22	°C/W	-
Thermal resistance, junction - case, bottom	$R_{thJC(bottom)}$	-	1.9	2.8	°C/W	-
Device on 1 layer PCB	R_{thJA}	-	60	70	°C/W	1s0p
Device on 4 layer PCB	R_{thJA}	-	38	-	°C/W	2s2p with vias

[1)] Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation

[2)] Device on 4-layer FR4 PCB, vertical in still air.

[3)] Pulse current limited by transfer characteristic. See diagram 6.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage[1]	$V_{GS(th)}$	1.2	2.0	2.9	V	V_{DS}=V_{GS}, I_D=8 mA, measured within 10 ms after a pre-bias at V_{GS}=5 V, V_{DS}=0 V for at least 5 ms
Drain-source leakage current	I_{DSS}	- -	0.2 20	20 250	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	- - - -	23 0.01 130 15	550 1.1 2200 100	µA	V_{GS}=5 V, T_j=25 °C V_{GS}=-4 V, T_j=25 °C V_{GS}=5 V, T_j=125 °C V_{GS}=-4 V, T_j=125 °C
Drain-source on-state resistance[2]	$R_{DS(on)}$	-	2.4	3.3	mΩ	V_{GS}=5 V, I_D=20 A
Gate resistance[3]	R_G	-	0.5	-	Ω	-

Table 5 Dynamic characteristics[3]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1100	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance	C_{oss}	-	630	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	8.6	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz

Table 6 Gate charge characteristics[4]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3.0	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 5 V
Gate charge at threshold	$Q_{g(th)}$	-	2.3	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 5 V
Gate to drain charge[3]	Q_{gd}	-	3.4	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 5 V
Switching charge	Q_{sw}	-	4.0	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 5 V
Gate charge total[3]	Q_g	-	11.0	-	nC	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 5 V
Gate plateau voltage	$V_{plateau}$	-	2.6	-	V	V_{DD}=50 V, I_D=20 A, V_{GS}=0 to 5 V
Output charge[3]	Q_{oss}	-	49	-	nC	V_{DD}=50 V, V_{GS}=0 V

[1] When tested without the specified V_{GS} pre-bias, $V_{GS(th)}$ will typically be 0.7 V lower than the threshold voltage measured under the specified conditions.
[2] $R_{DS(ON)}$ is measured without prior drain bias or switching stress. An upcoming application note will provide detailed information about dynamic $R_{DS(ON)}$ and recommendations for *in situ* measurement in target application conditions.
[3] Defined by design. Not subject to production test.
[4] See ″Gate charge waveforms″ for parameter definition

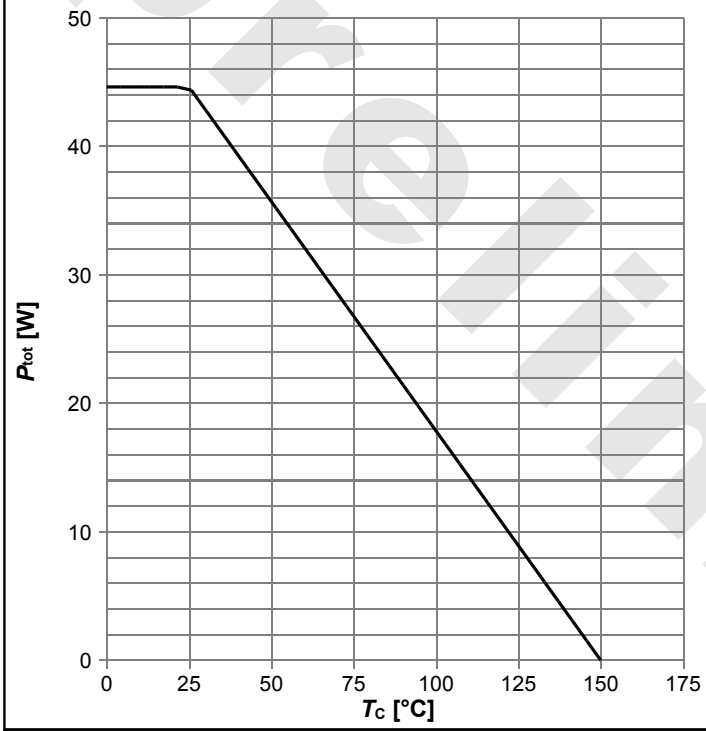
Table 7 Reverse operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse continuous current	I_S	-	-	13	A	T_C=25 °C
Pulsed current, reverse	$I_{S,pulse}$	-	-	100	A	T_C=25 °C
Source-Drain reverse voltage	V_{SD}	-	2.6	3.4	V	V_{GS}=0 V, $I_{S,}$pulse=20 A, T_j=25 °C
Reverse recovery charge[1)]	Q_{rr}	-	-	-	nC	V_R=50 V, $I_{S,pulse}$=20 A, di_S,pulse/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

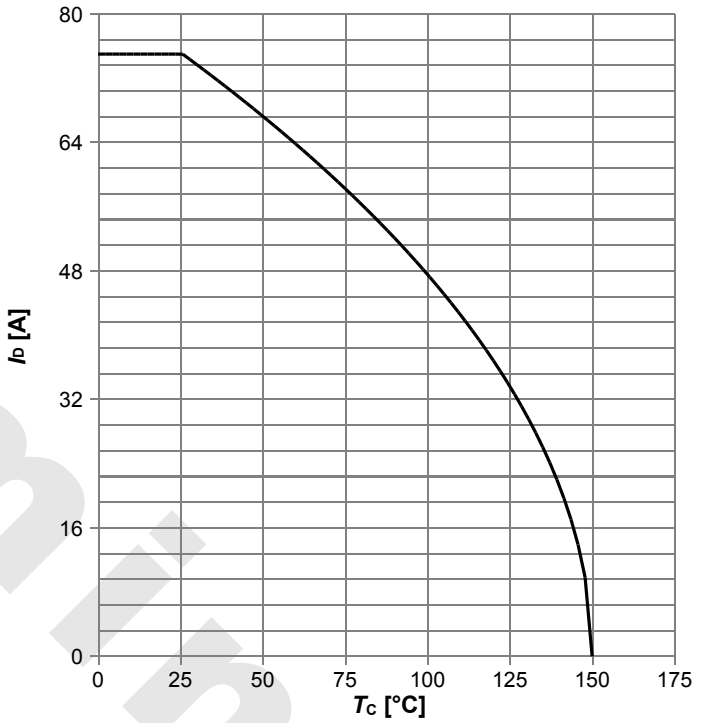
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



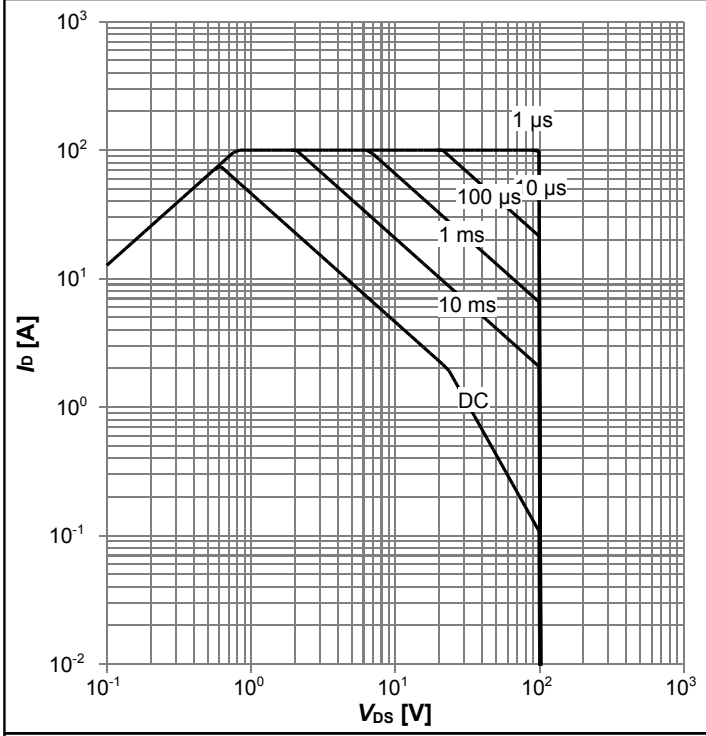
$P_{tot}=f(T_C)$

Diagram 2: Drain current



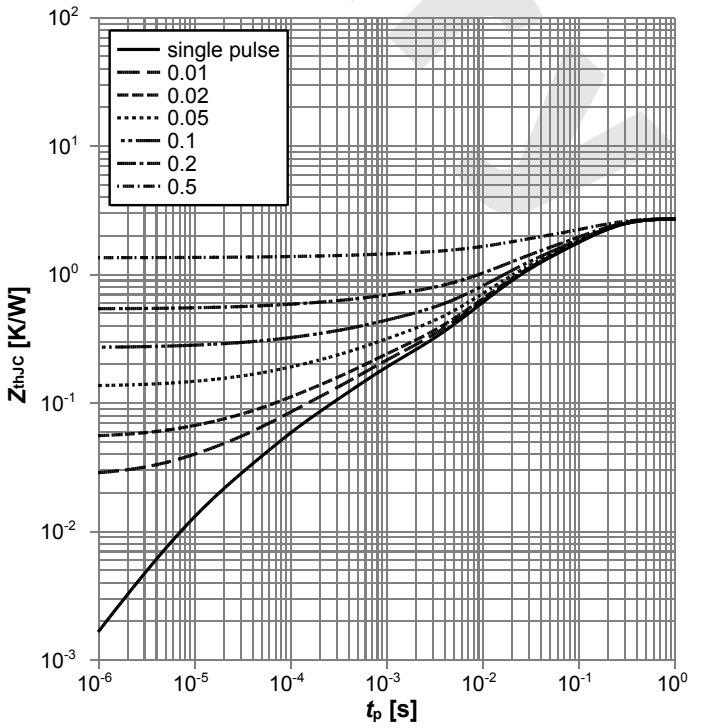
$I_D=f(T_C)$; $V_{GS}\geq 5$ V

Diagram 3: Safe operating area



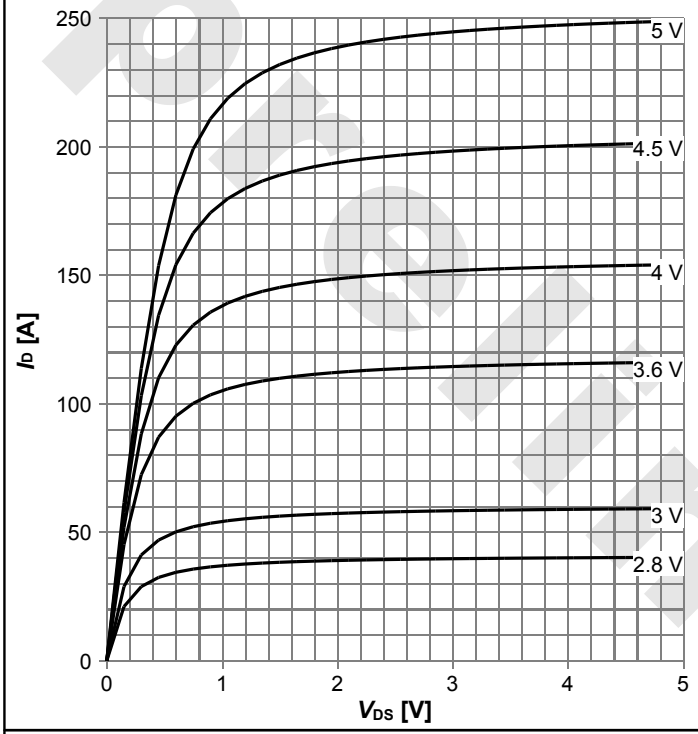
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



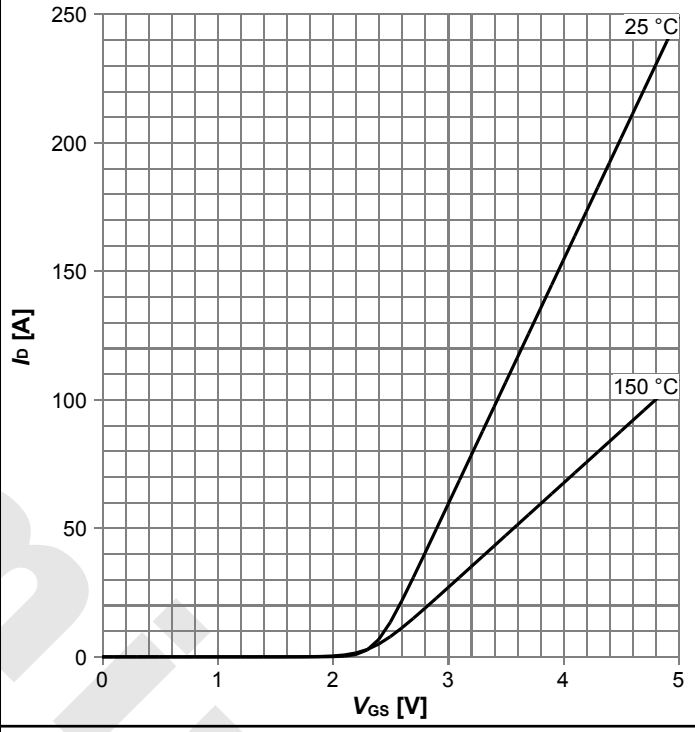
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



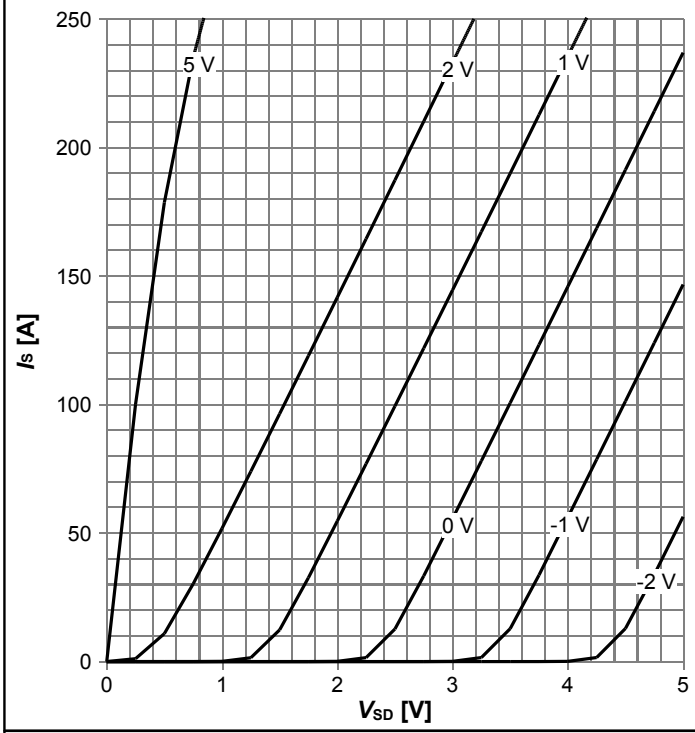
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. transfer characteristics



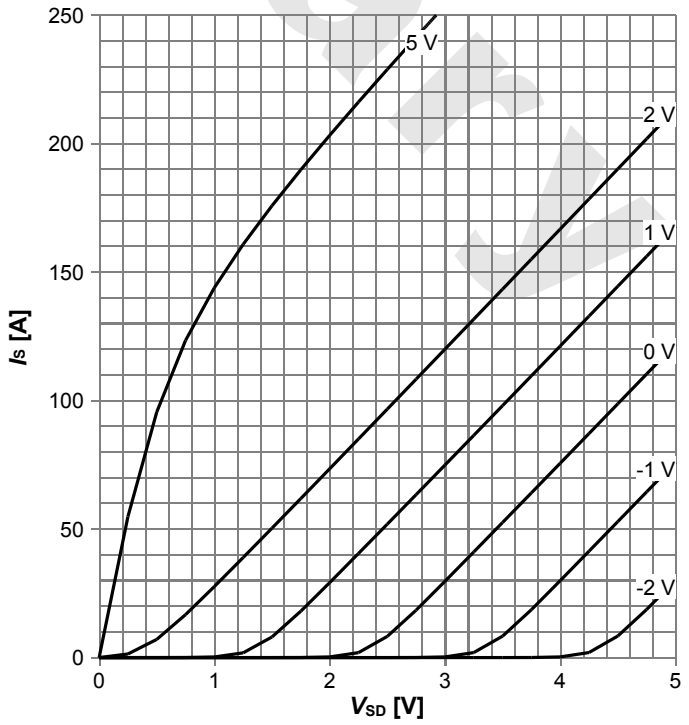
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 7: Typ. reverse output characteristics



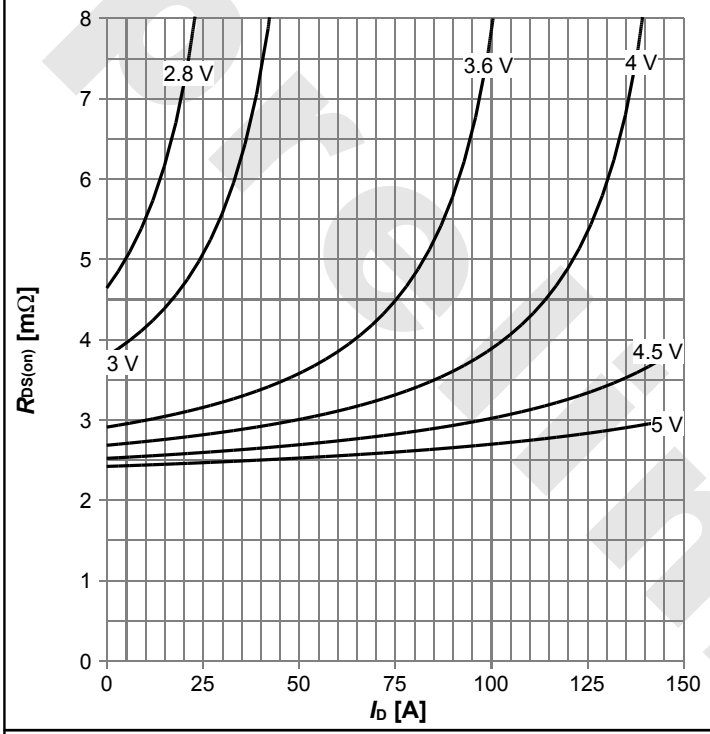
$I_F=f(V_{SD})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 8: Typ. reverse output characteristics



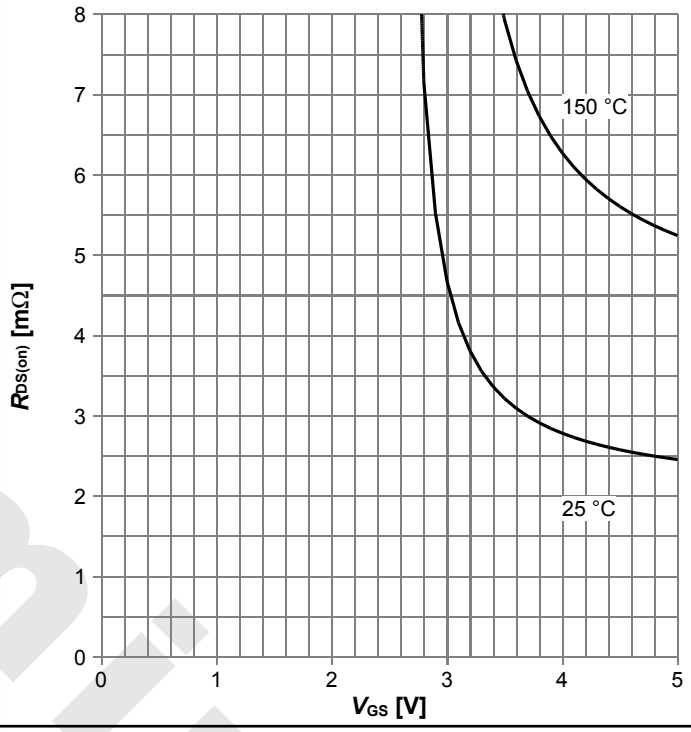
$I_F=f(V_{SD})$, $T_j=125$ °C; parameter: V_{GS}

Diagram 9: Typ. drain-source on resistance



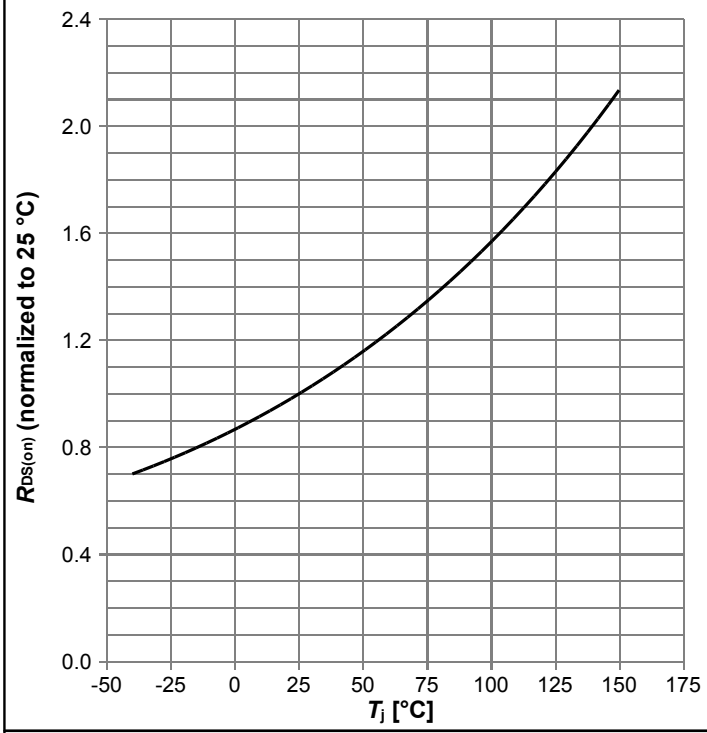
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 10: Typ. drain-source on resistance



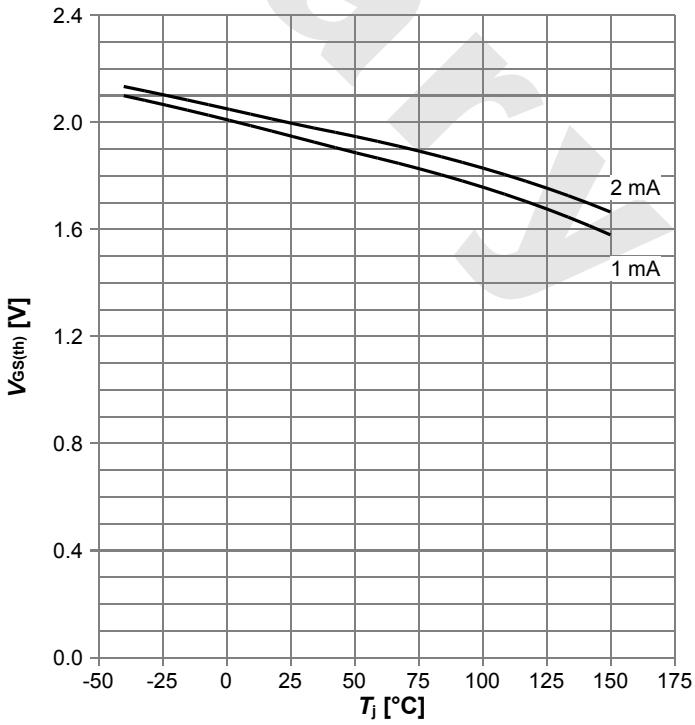
$R_{DS(on)}$=f(V_{GS}), I_D=20 A; parameter: T_j

Diagram 11: Normalized drain-source on resistance



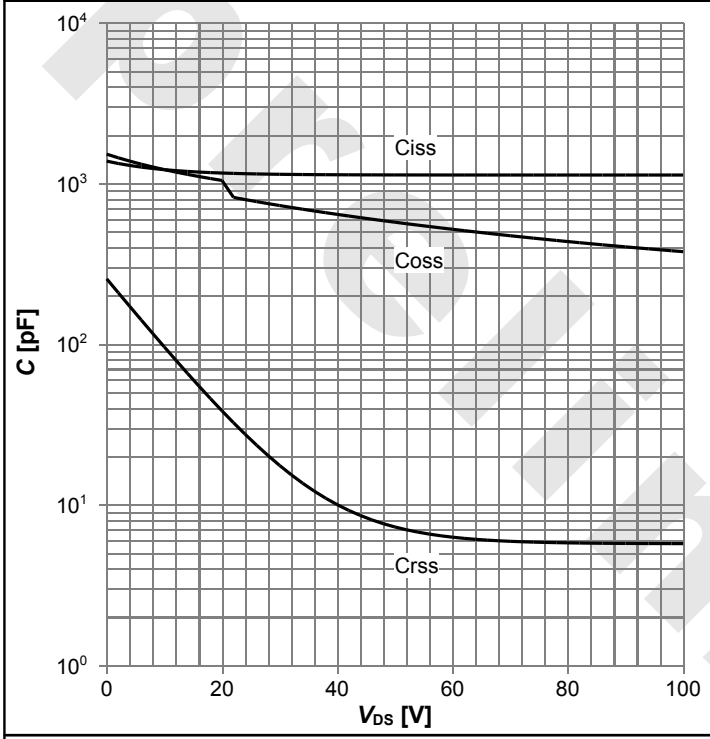
$R_{DS(on)}$=f(T_j), I_D=20 A, V_{GS}=5 V

Diagram 12: Typ. gate threshold voltage



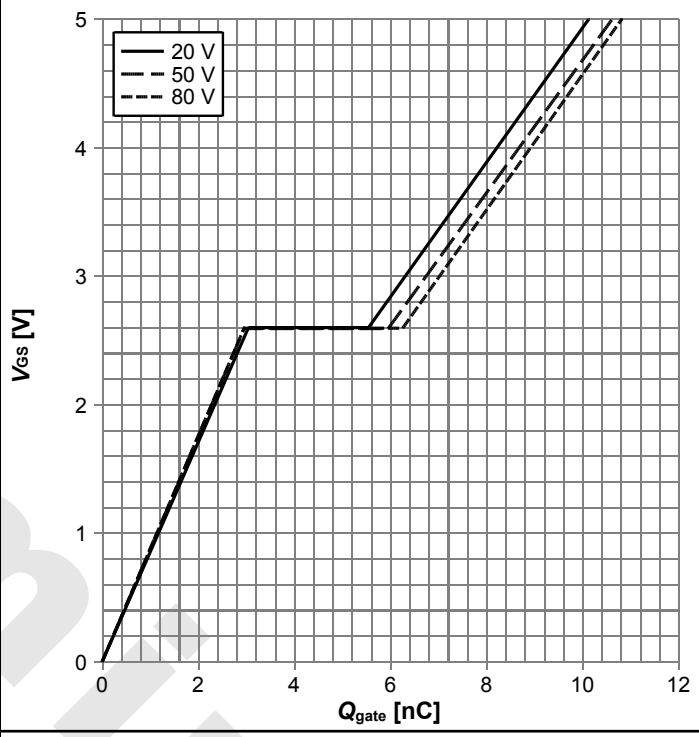
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 13: Typ. capacitances



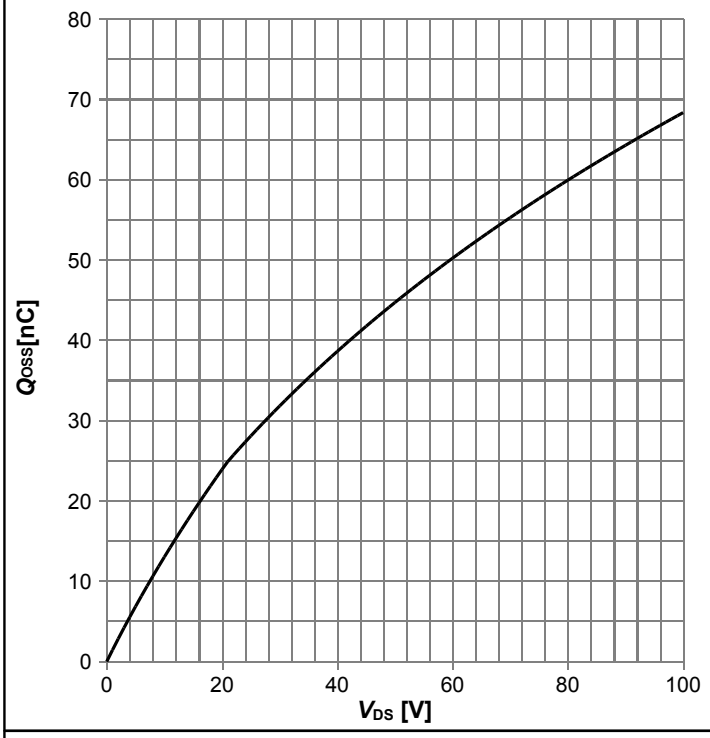
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 14: Typ. gate charge



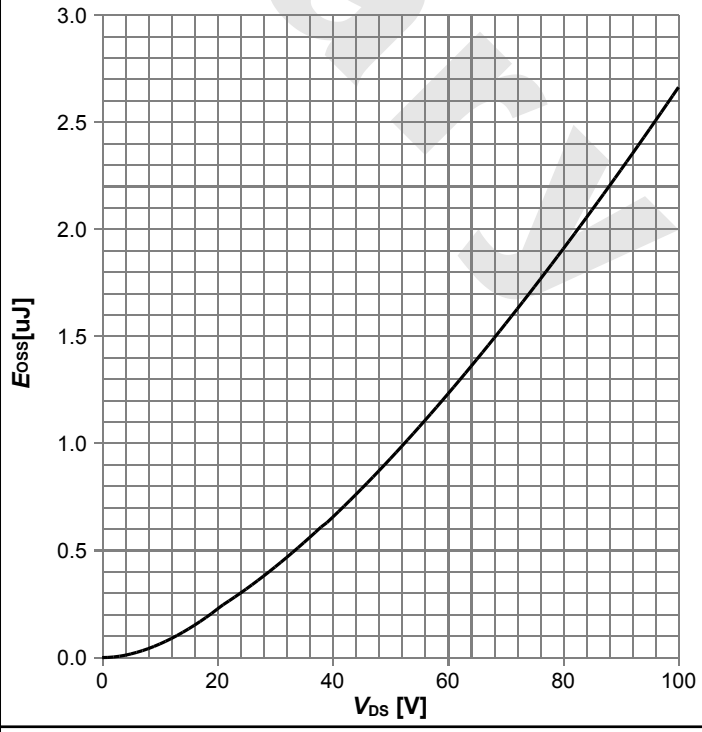
V_{GS}=f(Q_{gate}), I_D=20 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Typ output charge



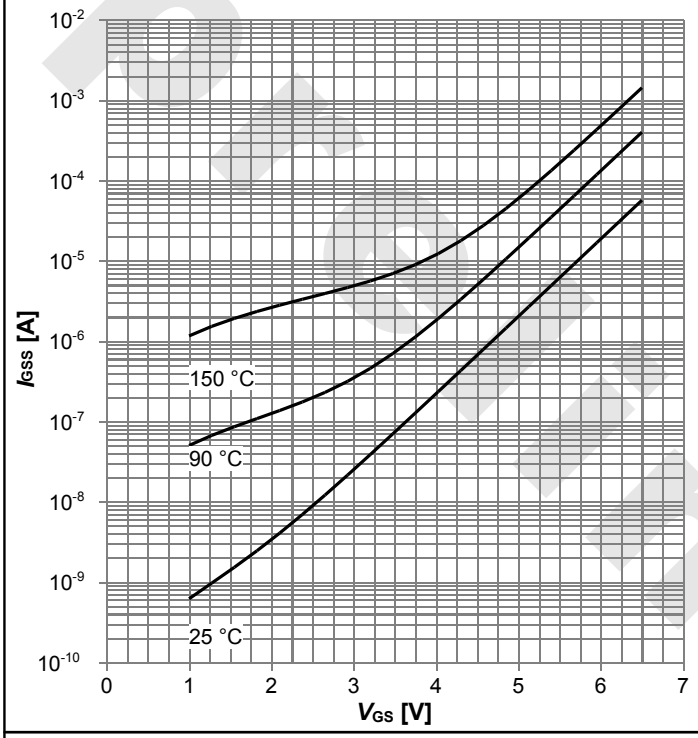
Q_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 16: Typ output energy



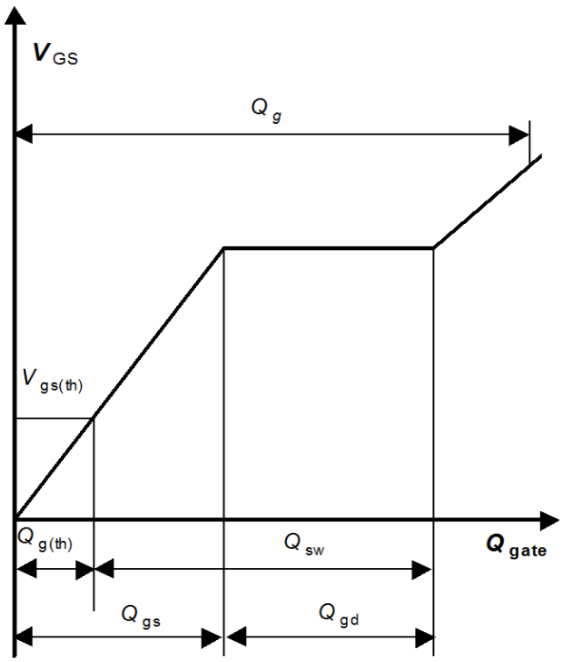
E_{oss}=f(V_{DS}), V_{GS}=0 V

Diagram 17: Typ gate-source leakage current

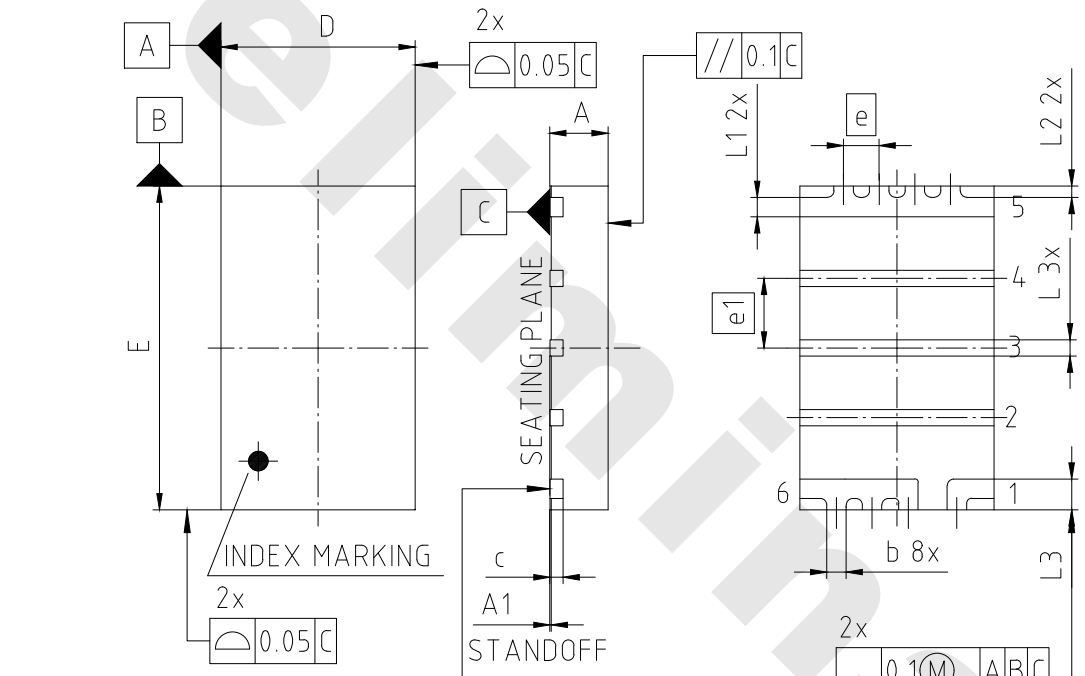


I_{GSS}=f(V_{GS}), V_{DS}=0 V; parameter: T_j

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-VSON-6-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A		1.00
A1		0.05
b	0.20	0.40
c		0.20
D	2.90	3.10
E	4.90	5.10
L	0.20	0.30
L1	0.25	0.35
L2	0.125	0.225
L3	0.425	0.525
e	0.55	
e1	1.075	
N	6	

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-6, dimensions in mm

Revision History

IGC033S101

Revision: 2024-05-20, Rev. 0.9

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.9	-	Release of preliminary version

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