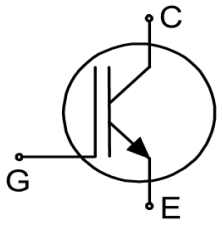
EDT2 IGBT Chip for Automotive Applications

IGBT

Quality Requirement Category: Automotive

Features

- 750V trench + field stop technology
- Low $V_{CE(sat)}$
- Low switching losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling
- Solderable / sinterable front-side pads



Applications

- Drives

Description

Recommended for power modules

Product Validation

Technology qualified for automotive applications. Ready for validation for automotive applications according to AEC Q100/101 or AQG324

Key Performance Parameters

Chip Type	V_{CE}	I_{Cn}	Die Size	Package
IGC77T75E12RDA	750V	170A	77.44mm^2	Sawn on foil

Table of Contents

1 Parameters and characteristics

Table 1 Mechanical Parameters

Raster size		8.800 x 8.800	mm^2
Area total		77.44	
Emitter pad size		See chip drawing	
Gate pad size		See chip drawing	
Silicon thickness		70	µm
Wafer size		300	mm
Maximum possible chips per wafer		794	
Passivation frontside		Photoimide	
Pad metal		NiP/Pd	
Backside metal		NiP/Pd	
Die bond		Soft solder or sinter	
Reject ink dot size		Inkless	
Storage environment (<6 months)	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C	

Table 2 Maximum Ratings

Parameter		Symbol	Value	Unit
Collector-emitter voltage	25°C ≤ T_{vj} ≤ 175°C	V_{CES}	750	V
	T_{vj} = -40°C [1/2]		700	
DC collector current, limited by $T_{vj\,max}$		I_C	- [1]	A
Pulsed collector current, t_p limited by $T_{vj\,max}$ [1]		$I_{C,puls}$	510	A
Gate-emitter voltage		V_{GE}	±20	V
Operating junction temperature		$T_{vj,op}$	-40 ... +175	°C
Short circuit data [1/3/4/5] V_{GE}≤15V, V_{CC}≤450V, T_{vj}≤175°C		t_{sc}	3	µs
Reverse bias safe operating area (RBSOA) [1]		$I_{C,max}$ = 340A, $V_{CE,max}$ = V_{CES}, -40°C ≤ $T_{vj,op}$ ≤ 175°C		

Table 3 Static Characteristics (Tested on Wafer), T_{vj}=25°C

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter saturation voltage	V_{CEsat}	V_{GE}=15V, I_C=51A	-	1.0	1.15	V
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C=2.4mA, V_{GE}=V_{CE}	5.0	5.8	6.5	
Zero gate voltage collector current	I_{CES}	V_{CE}=750V, V_{GE}=0V	-	-	100	µA
Gate-emitter leakage current	I_{GES}	V_{CE}=0V, V_{GE}=20V	-	-	600	nA
Integrated gate resistor	r_G		-	2.7	-	Ω

Table 4 Electrical Characteristics[1]

Parameter		Symbol	Conditions	Value			Unit
				min.	typ.	max.	
Collector-emitter saturation voltage	T_{vj}=25°C	V_{CEsat}	V_{GE}=15V, I_C=170A	-	1.25	1.45	V
	T_{vj}=175°C			-	1.4	-	
Input capacitance		C_{ies}	V_{CE}=25V, V_{GE}=0V, f=100kHz T_{vj}=25°C	-	19100	-	pF
Output capacitance		C_{oes}		-	320	-	
Reverse transfer capacitance		C_{res}		-	90	-	
Gate charge		Q_G	V_{CE}=450V, I_C =170A V_{GE}=-8V...+15V	-	1080	-	nC

[1] Not subject to production test - verified by design/characterization.

[2] V_{CES} increases linearly between -40°C and 25°C.

[3] Depending on thermal properties of assembly.

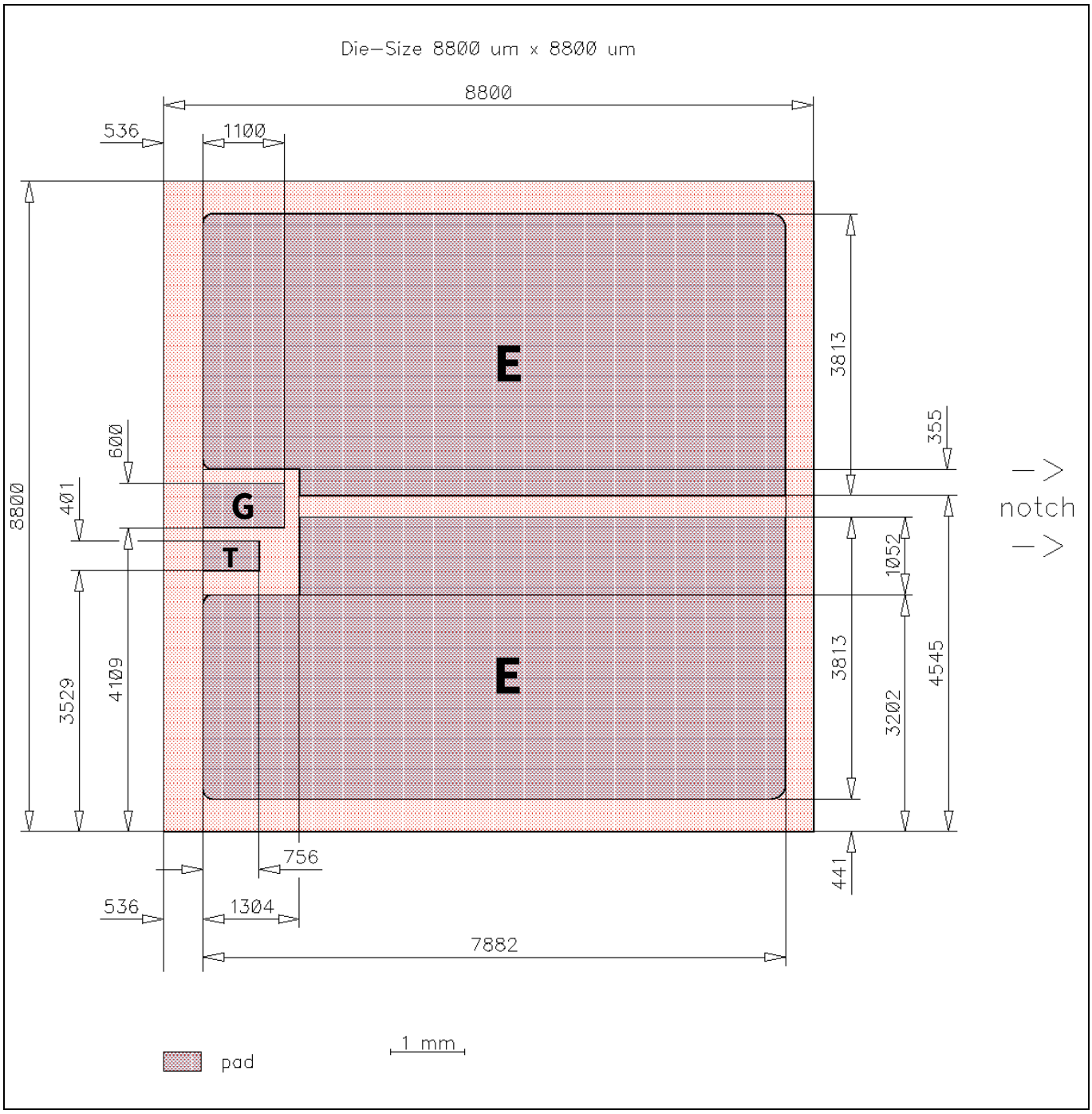
[4] Allowed number of short circuits: <1000; time between short circuits: >1s.

[5] Depending on electrical design of assembly.

2 Further Electrical Characteristics

Note: Switching characteristics and thermal properties are dependent on module design and mounting technology and can therefore not be specified for a bare die.

3 Chip Drawing



Key

- E = Emitter
- G = Gate
- T = Test pad, do not contact

4 Bare Die Product Specifics

Note: Test coverage at wafer level cannot cover the full range of customer application conditions. Therefore it is the responsibility of the customer to test all performance characteristics, which are relevant for their specific application, at the package level, including RBSOA and SCSOA.

Description

- AQL 0.1 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Document version	Date of release	Description of changes
V1.0	2019-08-05	Initial Datasheet
V1.01	2019-11-29	Datasheet update with additional parameters: - V_{CES} @ T_{vj}=-40°C - I_{CES} @ V_{CE}=750V - V_{CEsat} @ T_{vj}=175°C - C_{oes} - Q_G
V1.02	2020-03-18	Update of notes in Chapter 4.
V1.03	2021-08-05	Condition of chip capacitances is changed from f = 1MHz to 100kHz. The C_{res} value is modified with measurement result at f = 100kHz.

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