

## CoolGaN™ Gen2

### 650 V CoolGaN™ enhancement-mode Power Transistor

Infineon's CoolGaN™ is a highly efficient GaN (gallium nitride) transistor technology for power conversion in the voltage range up to 650 V. With extensive experience on the semiconductor market, Infineon's GaN technology brought the e-mode concept to maturity with end-to-end production in high volumes. The pioneering quality ensures the highest standards and offers the most reliable and performing solution among all GaN HEMTs on the market.

### Features

- Enhancement mode transistor - Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- ESD (HBM/CDM) JEDEC standards

### Benefits

- Improves system efficiency
- Improves power density
- Enables highest operating frequency
- System cost reduction savings
- Reduces EMI

### Potential applications

Industrial, telecom, datacenter SMPS, charger and adapter based on half-bridge topologies (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC).

### Product validation

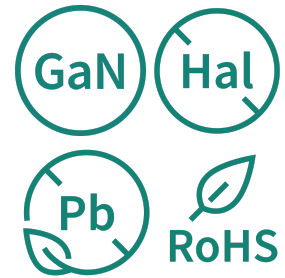
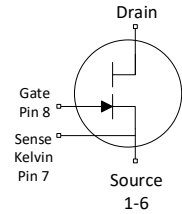
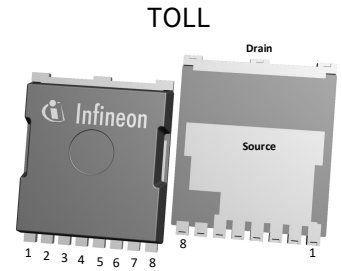
Fully qualified according to JEDEC for Industrial Applications

*Please note: Target Datasheet to change without further notice*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$	42	mΩ
$Q_{g,typ}$	11.0	nC
$I_{D,pulse}$	90	A
$Q_{oss @ 400 V}$	58	nC
$Q_{rr}$	0	nC

Type/Ordering Code	Package	Marking	Related Links
IGT65R035D2	PG-HSOF-8	65R035D2	see Appendix A





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Datasheet

## 1 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	$V_{GS} = 0\text{ V}$ , derating recommendation acc. JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	20	mA	$V_{GS} = 0\text{ V}$ , $V_{DS,trans} = 900\text{ V}$
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1 % duty cycle, <1 $\mu\text{s}$ , 1 M pulses
Drain source voltage, pulsed	$V_{DS,pulse}$ $V_{DS,pulsed}$	-	-	750 650	V	$T_j = 25\text{ °C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$ $T_j = 125\text{ °C}$ ; $V_{GS} \leq 0\text{ V}$ ; cumulated stress time $\leq 1\text{ h}$
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$ ; turn on $I_{D,pulse} = 44\text{ A}$ ; $T_j = 105\text{ °C}$ ; $f \leq 100\text{ kHz}$ , $t \leq 100\text{ sec.}$ (10 million pulses)
Continuous current, drain source <sup>1)</sup>	$I_D$	-	-	49	A	$T_c = 25\text{ °C}$ ; $T_j = T_{j,max}$
Pulsed current, drain source	$I_{D,pulse}$	-90 -45	-	90 45	A	$T_j = 25\text{ °C}$ ; $I_G = 42\text{ mA}$ ; See Diagram 3, 5 $T_j = 125\text{ °C}$ ; $I_G = 42\text{ mA}$ ; See Diagram 4, 6
Gate current, continuous <sup>2)</sup>	$I_{G,avg}$	-	-	32	mA	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; See Table 9
Gate current, pulsed <sup>2)</sup>	$I_{G,pulsed}$	-3.2	-	3.2	A	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; $t_{PULSE} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; See Table 9
Gate source voltage, continuous <sup>2)</sup>	$V_{GS}$	-10	-	-	V	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; See Diagram 12
Gate source voltage, pulsed <sup>2)</sup>	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$ ; $t_{PULSE} = 50\text{ ns}$ , $f = 100\text{ kHz}$ ; open drain
Power dissipation	$P_{tot}$	-	-	162	W	$T_c = 25\text{ °C}$
Operating junction temperature	$T_j$	-55	-	150	°C	-
Storage temperature	$T_{stg}$	-55	-	150	°C	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	$dv/dt$	-	-	200	V/ns	-

1) Limited by  $T_{j,max}$ . Maximum Duty Cycle  $D = 0.75$

2) We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.77	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	86	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	-	62	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm <sup>2</sup> (one layer, 70 μm thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{sold}$	-	-	260	°C	MSL1

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless specified otherwise

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 -	1.2 1	1.6 -	V	$I_{DS}=4.2\text{ mA}$ ; $V_{DS}=10\text{ V}$ ; $T_j=25\text{ °C}$ $I_{DS}=4.2\text{ mA}$ ; $V_{DS}=10\text{ V}$ ; $T_j=150\text{ °C}$
Gate-Source reverse clamping voltage	$V_{GS,clamp}$	-	-	-8	V	$I_{GS}=-1\text{ mA}$
Drain-Source leakage current	$I_{DSS}$	-	1.6 32	160 -	$\mu\text{A}$	$V_{DS}=650\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=650\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=150\text{ °C}$
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.035 0.075	0.042 -	$\Omega$	$I_G=42\text{ mA}$ ; $I_D=13\text{ A}$ ; $T_j=25\text{ °C}$ $I_G=42\text{ mA}$ ; $I_D=13\text{ A}$ ; $T_j=150\text{ °C}$
Gate resistance	$R_{G,int}$	-	tbd	-	$\Omega$	LCR impedance measurement; $f=f_{res}$ , open drain;

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	530	-	pF	$V_{GS}=0\text{ V}$ ; $V_{DS}=400\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	85	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=400\text{ V}$ , $f=1\text{ MHz}$
Reverse Transfer capacitance	$C_{rss}$	-	1.02	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=400\text{ V}$ , $f=1\text{ MHz}$
Effective output capacitance, energy related <sup>3)</sup>	$C_{o(er)}$	-	tbd	-	pF	$V_{DS}=0\text{ to }400\text{ V}$
Effective output capacitance, time related <sup>4)</sup>	$C_{o(tr)}$	-	tbd	-	pF	$V_{GS}=0\text{ V}$ ; $V_{DS}=0\text{ to }400\text{ V}$ ; $I_D=const$
Output charge	$Q_{oss}$	-	58	-	nC	$V_{DS}=0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	tbd	-	ns	$I_D=13\text{ A}$ ; $R_{ON}=3.3\text{ Ohm}$ ; $R_{OFF}=3.3\text{ Ohm}$ ; $R_{SS}=220\text{ Ohm}$ ; $C_C=5.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8
Turn-off delay time	$t_{d(off)}$	-	tbd	-	ns	$I_D=13\text{ A}$ ; $R_{ON}=3.3\text{ Ohm}$ ; $R_{OFF}=3.3\text{ Ohm}$ ; $R_{SS}=220\text{ Ohm}$ ; $C_C=5.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8
Rise time	$t_r$	-	tbd	-	ns	$I_D=13\text{ A}$ ; $R_{ON}=3.3\text{ Ohm}$ ; $R_{OFF}=3.3\text{ Ohm}$ ; $R_{SS}=220\text{ Ohm}$ ; $C_C=5.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8
Fall time	$t_f$	-	tbd	-	ns	$I_D=13\text{ A}$ ; $R_{ON}=3.3\text{ Ohm}$ ; $R_{OFF}=3.3\text{ Ohm}$ ; $R_{SS}=220\text{ Ohm}$ ; $C_C=5.3\text{ nF}$ ; $V_{DRV}=12\text{ V}$ ; see Table 8

3)  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

4)  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400 V

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate charge	$Q_G$	-	11	-	nC	$V_{GS}=0$ to 3 V; $V_{DS}=400$ V, $I_D=13$ A

**Table 7 Reverse conduction characteristics**

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	$V_{SD}$	-	2.2	2.5	V	$V_{GS}=0$ V; $I_{SD}=13$ A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	90	A	$I_G=42$ mA
Reverse recovery charge <sup>5)</sup>	$Q_{rr}$	-	0	-	nC	$I_{SD}=13$ A; $V_{DS}=400$ V

5) Excluding  $Q_{oss}$

## 4 Electrical characteristics diagrams

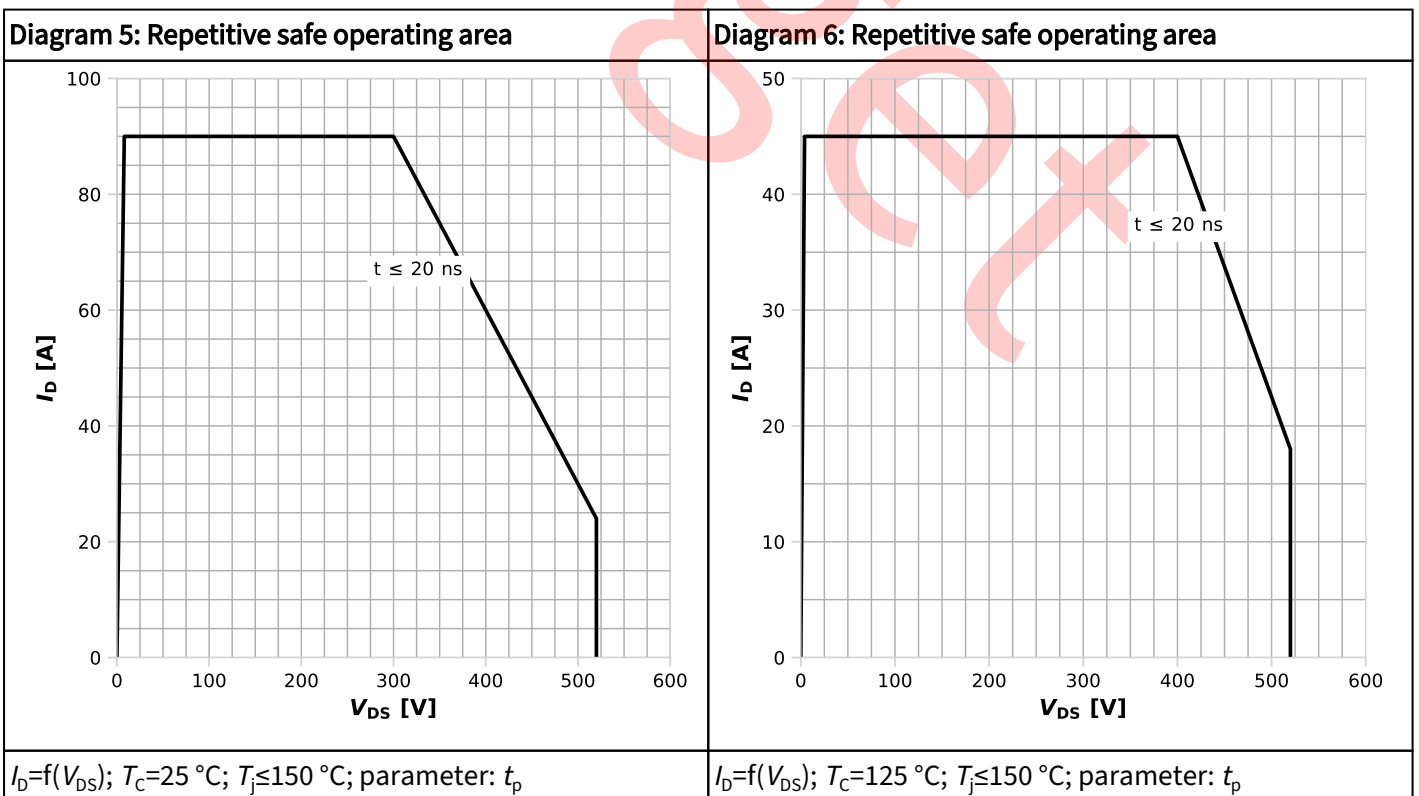
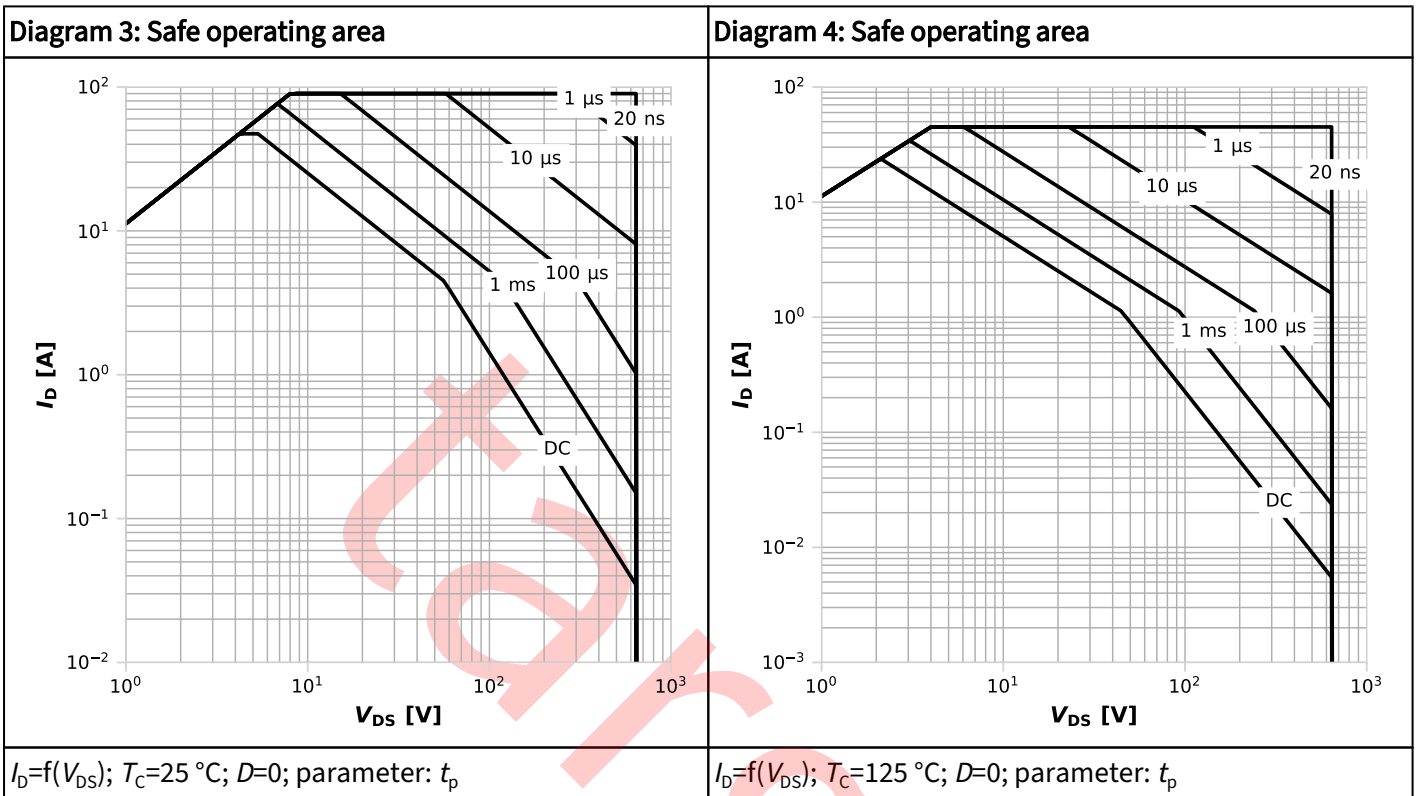
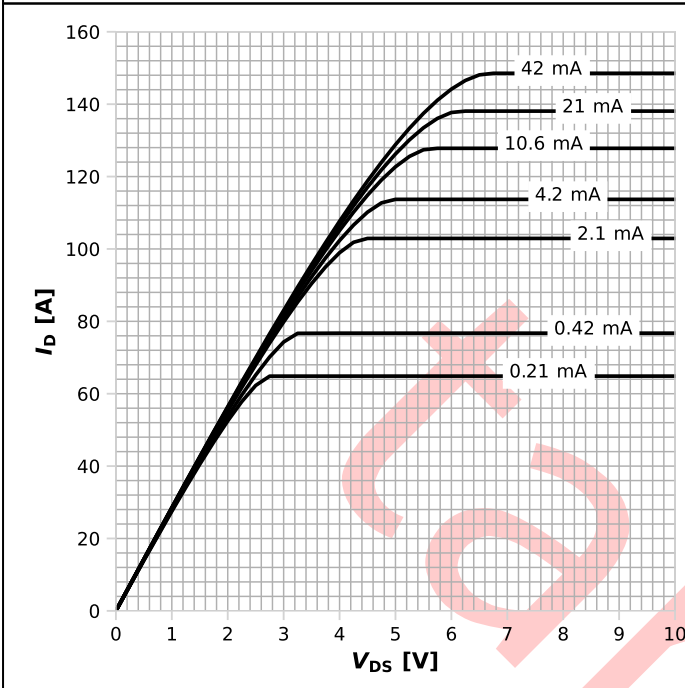
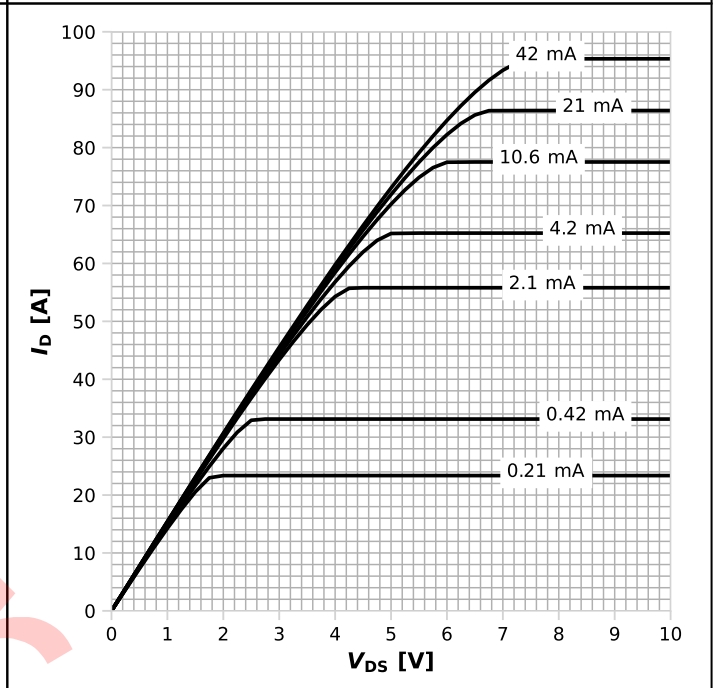


Diagram 7: Typ. output characteristics



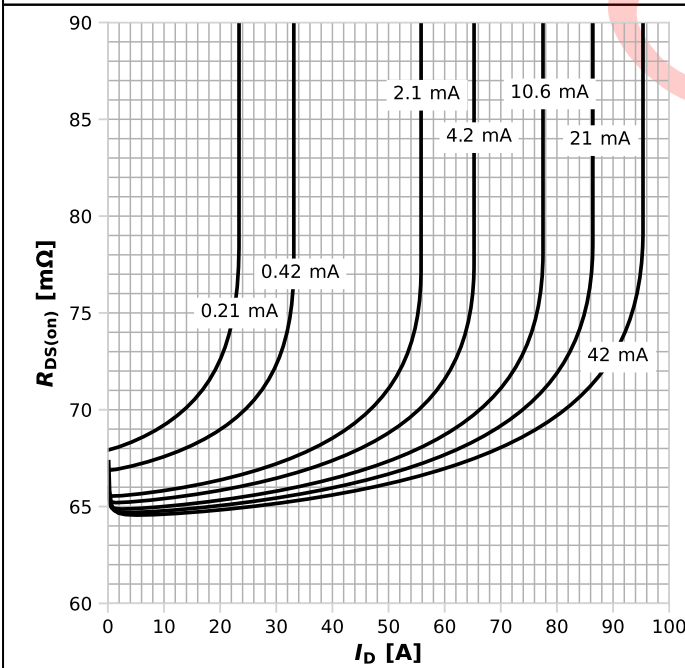
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } I_{GS}$

Diagram 8: Typ. output characteristics



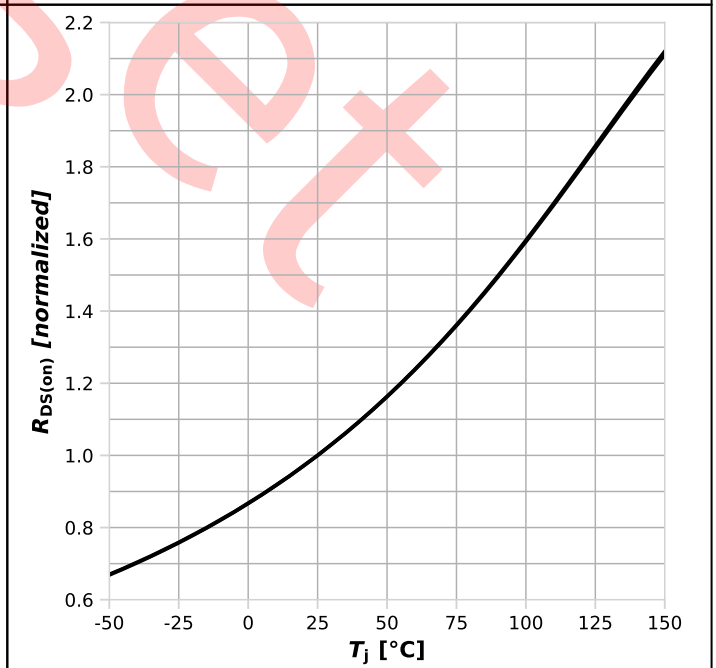
$I_D = f(V_{DS}); T_j = 125\text{ °C}; \text{parameter: } I_{GS}$

Diagram 9: Typ. Drain-source on-state resistance



$R_{DS(on)} = f(I_D); T_j = 125\text{ °C}; \text{parameter: } I_{GS}$

Diagram 10: Drain-source on-state resistance



$R_{DS(on)} = f(T_j); I_D = 13\text{ A}$



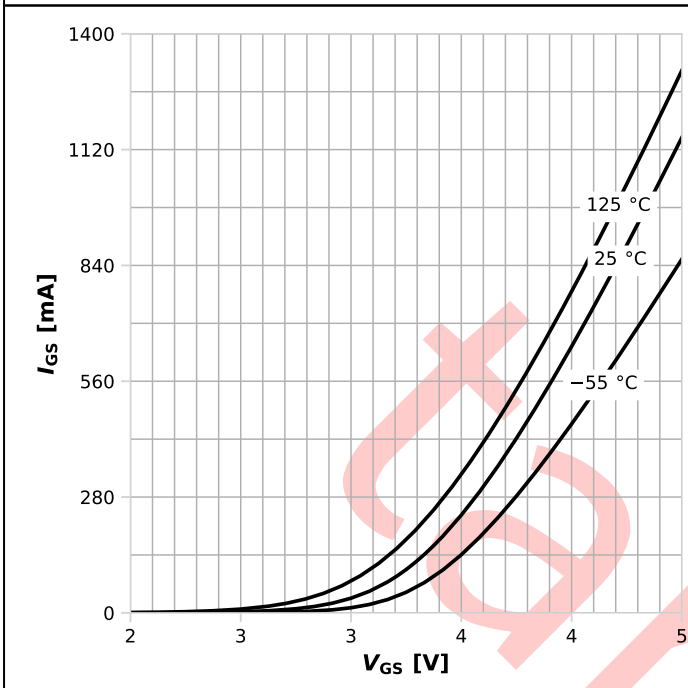
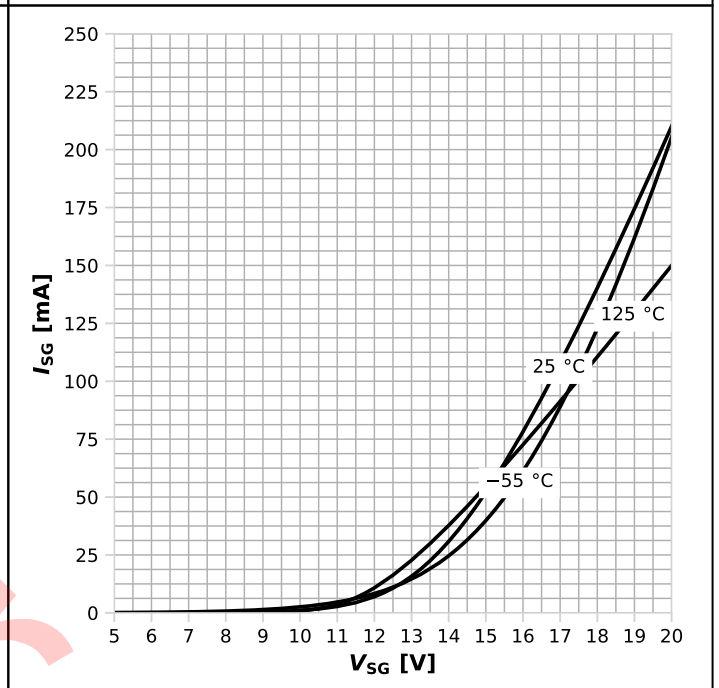
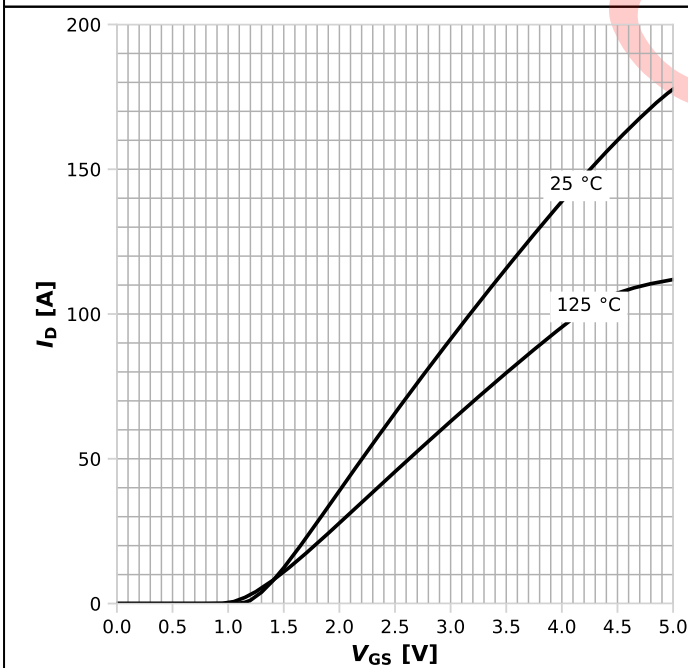
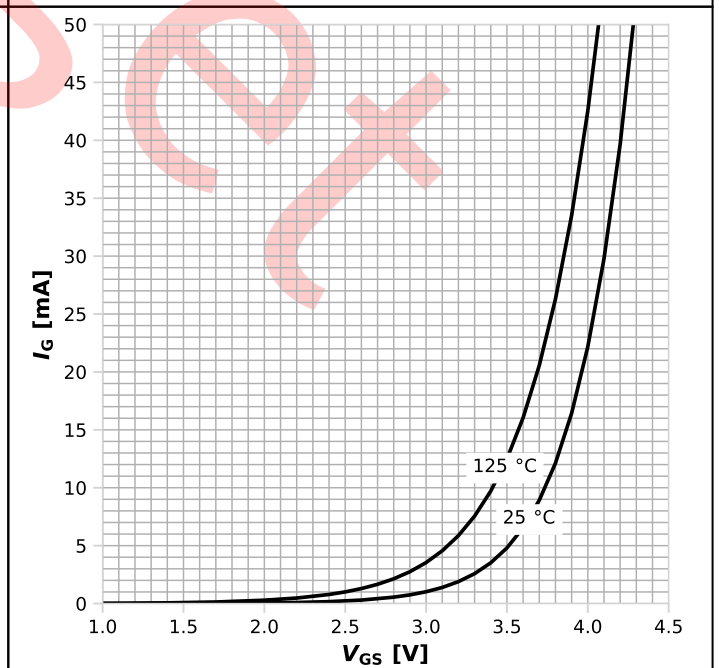
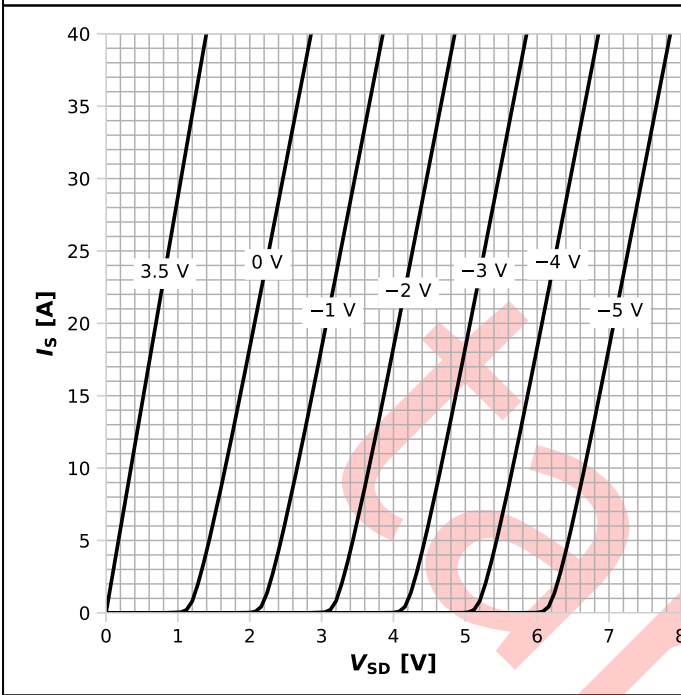
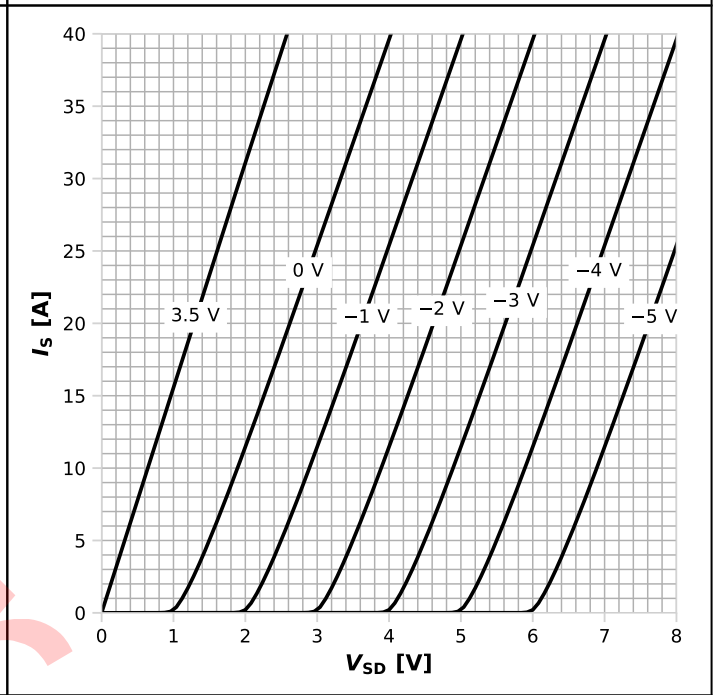
**Diagram 11: Typ. gate characteristics forward**

 $I_{GS}=f(V_{GS})$ ; open drain; parameter:  $T_j$ 
**Diagram 12: Typ. gate characteristics reverse**

 $I_{SG}=f(V_{SG})$ ; parameter:  $T_j$ 
**Diagram 13: Typ. transfer characteristics**

 $I_D=f(V_{GS})$ ;  $V_{DS}=8V$ ; parameter:  $T_j$ 
**Diagram 14: Typ. transfer gate current characteristic**

 $I_G=f(V_{GS})$ ;  $V_{DS}=8V$ ; parameter:  $T_j$

Diagram 15: Typ. channel reverse characteristics



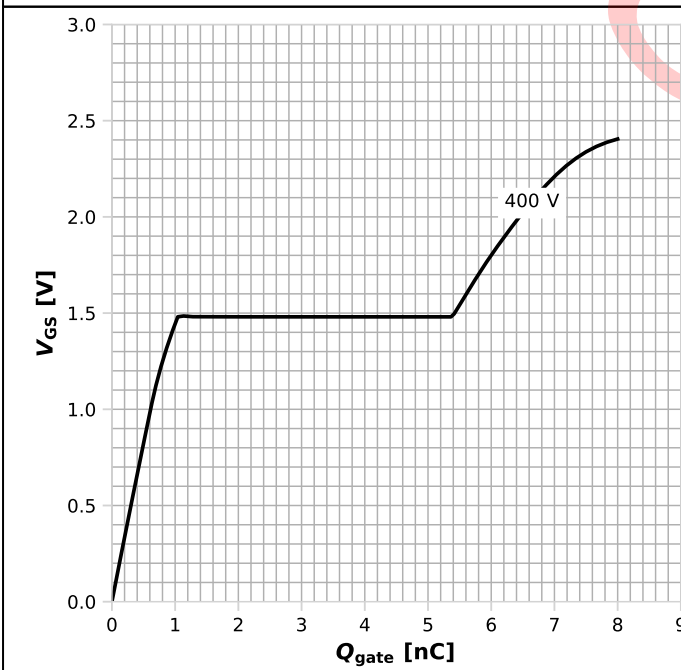
$I_s = f(V_{SD}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 16: Typ. channel reverse characteristics



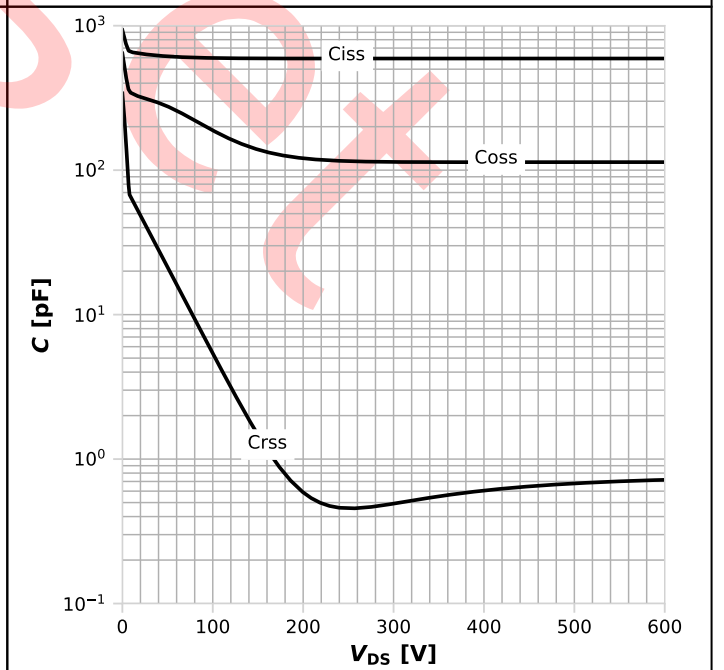
$I_s = f(V_{SD}); T_j = 125\text{ °C};$  parameter:  $V_{GS}$

Diagram 17 Typ. gate charge



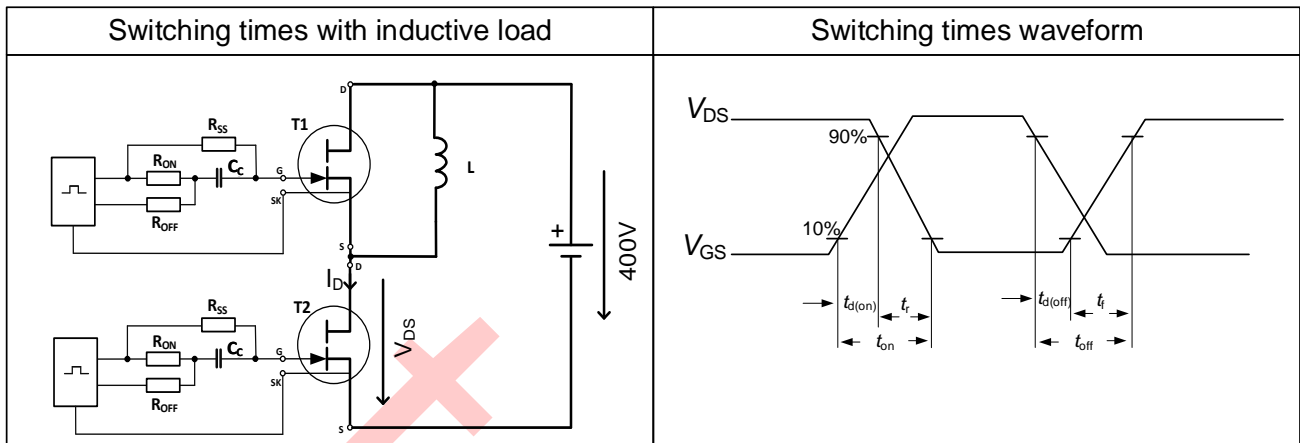
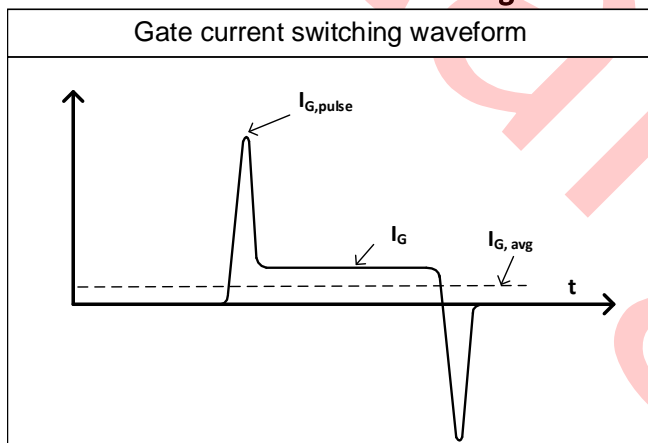
$V_{GS} = f(Q_{gate}); I_D = 13\text{ A pulsed};$  parameter:  $V_{DD}$

Diagram 18: Typ. capacitances

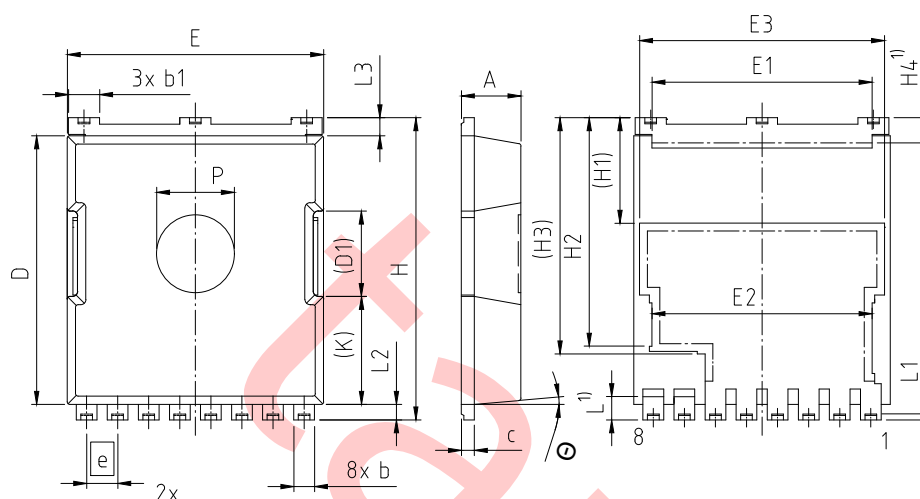


$C = f(V_{DS}); V_{GS} = 0\text{ V}$

## 5 Test Circuits

**Table 8 Reverse Channel Characteristics Test**

**Table 9 Gate current switching waveform**


## 6 Package Outlines

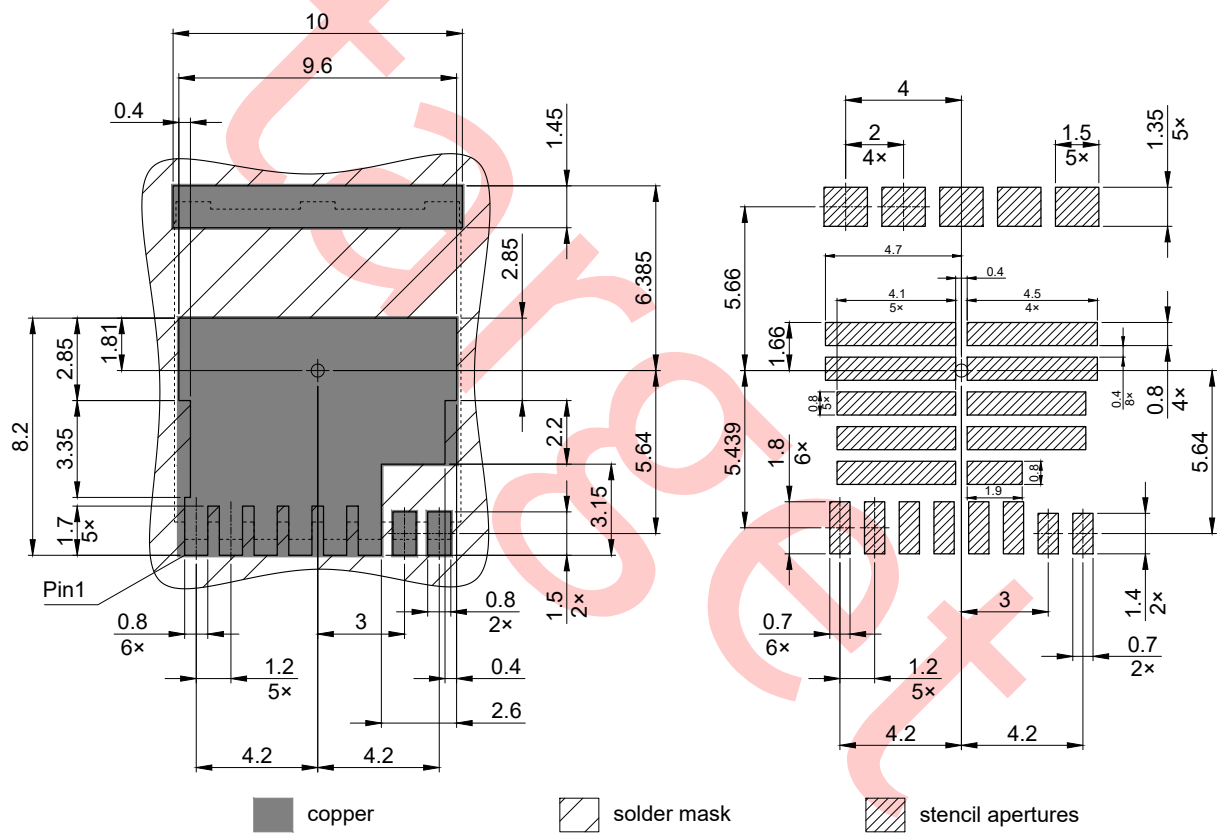


PACKAGE - GROUP NUMBER: PG-HSOF-8-U04		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	1.10	1.30
c	0.40	0.60
D	10.275	10.575
D1	(3.20)	(3.40)
E	9.70	10.10
E1	8.40	8.60
E2	8.40	8.60
E3	9.36	9.56
e	1.20	
H	11.475	11.875
H1	(3.98)	(4.18)
H2	8.73	8.93
H3	(9.03)	(9.23)
H4	0.88	1.08
N	8	
K	(4.07)	(4.27)
L	0.80	1.00
L1	0.13	0.33
L2	0.50	0.70
L3	0.60	0.80
P	2.90	3.10
Θ	3.5°	6.5°

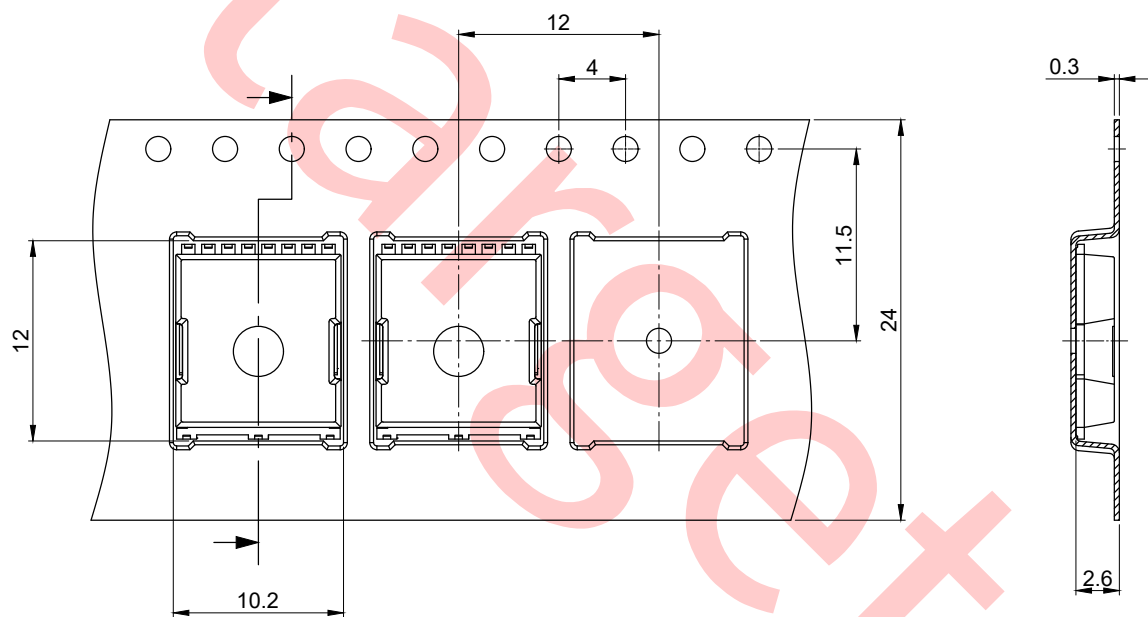
## NOTES:

1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED

Figure 1 Outline PG-HSOF-8, dimensions in mm



**Figure 2 Outline PG-HSOF-8, dimensions in mm**



All dimensions are in units mm  
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊥]

**Figure 3** Outline PG-HSOF-8, dimensions in mm

## 7 Appendix A

**Table 10**    **Related Links**

- [IFX CoolGaN™ GaN 650 V webpage](#)
- [IFX CoolGaN™ GaN 650 V reliability white paper](#)
- [IFX CoolGaN™ GaN 650 V gate driver application note](#)
- [IFX CoolGaN™ GaN 650 V applications information](#)

Datasheet

## Revision History

IGT65R035D2

### Revision 2024-04-15, Rev. 0.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.1	2024-04-15	Release of target

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