
Triple DC to DC Converter Control IC for CCD Image sensor

DESCRIPTION

IK3301 is to be used as power supply control IC for the system that is based on CCD image sensor. IK3301 supplies all the voltages that are needed to operate CCD image sensor, 15V, 5V and -8V, with excellently controlled ripple voltage. The typical power efficiency of this device is 80% at a standard load current. Due to the high power efficiency, the heat dissipation is suppressed, which can be fatal to the image quality of CCD sensor. Excellent voltage ripple and suppressed heat dissipation will be very beneficial for the CCD system that needs high image quality.

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FEATURES

- Built-in 3-Channel Voltage Output Option : 15V / 5.0V / -8V, 12V / 3.3V / -8V
- PWM Method
- High Power Efficiency (80%)
- Low Heat Dissipation
- 9~18V Wide Operating Voltage
- Very Low Ripple Voltage Noise (less than 20mV)
- High Driving Current (300mA@Vout 3.3V or 5.0V)
- Small Package Size :16pin MLP (QFN)
- Simple and Low Cost External Circuit
- Built-in Protection Circuit for External Damage

APPLICATION

- B/W CCD Camera System
- Color CCD Camera System
- Other CCD Image Sensor Power Supply

General Description

Figure 1 shows the simplified block diagram of IK3301. The device consists of two highly efficient DC-DC converters, a negative charge pump, clock generator to supply clock signals to each circuit and reference voltage generator.

The 15V supply voltage is generated by UP voltage converter, which utilizes one external inductor, one external capacitor and two external diodes. The internal comparator continuously monitors the output voltage and adjusts it to 15V by controlling PWM (Pulse Width Modulation) circuit. The 5V supply voltage is generated by DOWN voltage converter, which utilizes one external inductor, one PFET switch, one external capacitor and one external diode. The internal comparator continuously monitors the output voltage and adjusts it to 5V by controlling PWM circuit. The -8V supply voltage is generated by negative charge pump. This circuit needs two diodes, two external capacitors, and one external inductor. The user can adjust the output voltages by changing the feedback resistor ratio for all three output voltages.

The reference voltage is generated from internal Band-gap reference circuit and almost constant to the temperature and the power supply voltage. As a result, 15V, 5V, and -8V voltage outputs are also constant to temperature and power supply voltage.

Block Diagram

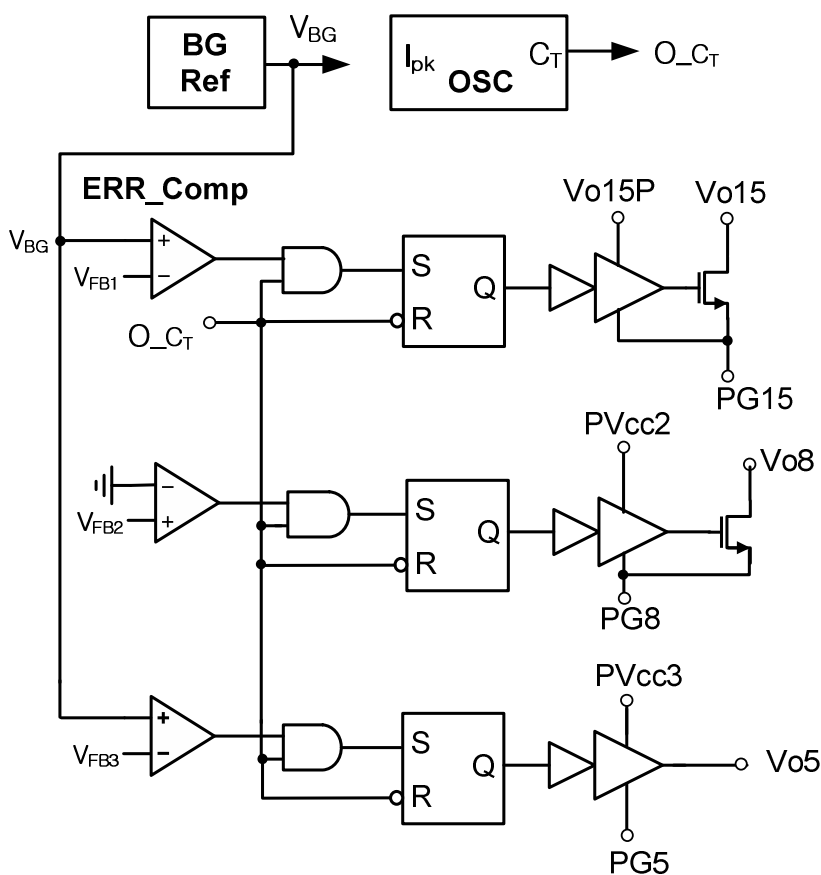


Figure 1. Block Diagram

Pin Description for IK3301 (16-QFN)

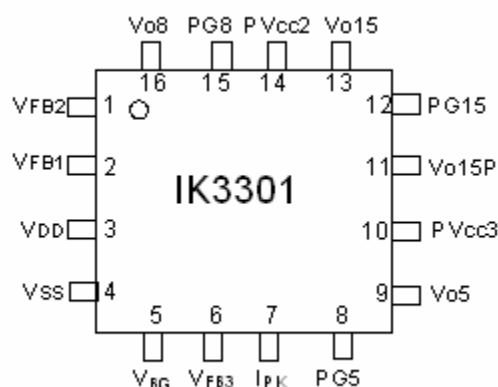


Figure 2. Package Pin-out Diagram

Pin Description

Pin No	Pin Name	I/O, P/G	Description
1	VFB2	I	Feedback Input2
2	VFB1	I	Feedback Input1
3	VDD	P	Analog Signal Block Power Supply (Common supply at the PCB)
4	VSS	G	Analog Signal Block Ground (Common GROUND point at the PCB)
5	BG	O	Bandgap Reference Voltage Output
6	VFB3	I	Feedback Input3
7	IPK	I	Peak Current Sense
8	PG5	G	Power Ground for 5V Generation (Common GROUND point at the PCB)
9	Vo5	O	PWM Output for 5V Output
10	PVcc3	P	Power Block Power Supply for 5V Output (Common supply at the PCB)
11	Vo15P	O	PSIDE PWM Output for 15V Output
12	PG15	G	Power Ground for 15V Generation (Common GROUND point at the PCB)
13	Vo15	O	NSIDE PWM Output for 15V Output
14	PVcc2	P	Power Supply for -8V output (Common supply at the PCB)
15	PG8	G	Power Ground for -8V Generation (Common GROUND point at the PCB)
16	Vo8	O	PWM Output for -8V Output

Absolute Maximum Ratings and Recommend Operating Conditions

Absolute Maximum Ratings		Recommend Operating Conditions	
Power Supply Voltage VDD, PVcc2, PVcc3	-0.5V to +25.0V	Power Supply Voltage VDD, PVcc2, PVcc3	9V to 18V
Voltage on Any Pin with GND = 0V (V _I)	-0.5V to +25.0V	Operating Temperature(T _A)	-40°C to 85°C
Storage Temperature Range (T _S)	-65°C to +150°C		

Electrical Characteristics (V_{DD} = 9V~15V, -40°C < T_A < 85°C, Except as Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{DD}	Power Supply Current	V _{DD} , PV _{CC2} , PV _{CC3} =12.0V	--	10	20	mA
I _{out5}	Output Current of 5V Output	V _{DD} , PV _{CC2} , PV _{CC3} =12.0V	300	--	--	mA
I _{out15}	Output Current of 15V Output	V _{DD} , PV _{CC2} , PV _{CC3} =12.0V	15	--	--	mA
I _{outN8}	Output Current of -8V Output	V _{DD} , PV _{CC2} , PV _{CC3} =12.0V	10	--	--	mA
V _{o5}	5V Output Voltage		4.8	5.0	5.2	V
V _{o15}	15V Output Voltage		14.5	15.0	15.5	V
V _{o8}	-8V Output Voltage		-7.7	-8.0	-8.3	V
V _{o33}	3.3V Output Voltage		3.17	3.3	3.4	V
V _{o12}	12V Output Voltage		11.5	12.0	12.5	V

Electrical Description

The standard external components for standard load are shown in Figure 4.

1. Multi-output Generation(-8V & 5V & 15V)

IK3301 consists of CMOS step-down, step-up, and Voltage-inverting switching regulator, which produces 5V, 15V, and -8V. This device contains an internal temperature compensated bandgap reference, comparator, duty cycle controlled oscillator with cycle-cycle current limit circuit, and high current output switch with logic gates. Three outputs of 5V, 15V, and -8V are adjustable through two external feedback resistors with 2% reference voltage accuracy. The power efficiency depends on the value and the efficiency of external components, the load current and the target ripple voltage. The minimum efficiency of the 5V voltage generator is 80% with the reference circuit shown in Figure 4. The maximum load current of 5V of the reference circuit is 300mA, the maximum ripple voltage is 20mV. To save external components, internal Pch and Nch Power MOS FET are used to generate -8V and 15V. The 5V Pch Power MOS FET is used as external component because of high peak current and package power dissipation.

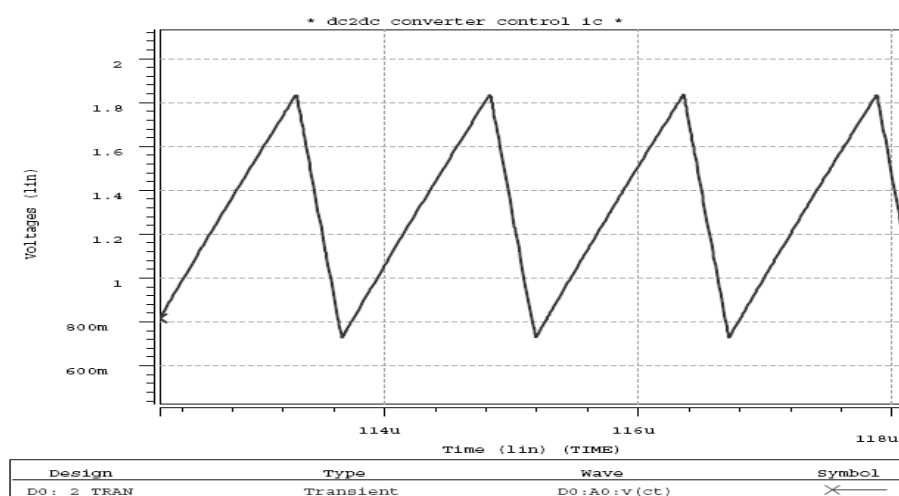
2. Internal BG Reference

IK3301 generates three outputs which are determined by the internal bandgap reference voltage and the ratio of the feedback resistors. Therefore, the output voltages of 15V, 5V, and -8V are also insensitive of the temperature and power supply variations.

3. Internal Oscillator

IK3301 has an internal oscillator which charges and discharges the internal timing capacitor using current sourcing and sinking between an upper and lower predetermined threshold voltage. The upper threshold voltage is 1.8V and the lower threshold voltage is 0.8V. The charging current and discharging current ratio is one to six which will vary depending on running frequency. The oscillator frequency is around 500KHz which is determined by the chosen internal capacitor value and charging & discharging current and oscillator amplitude.

Internal Oscillator



Maximum Output Voltage of the Charge Pump

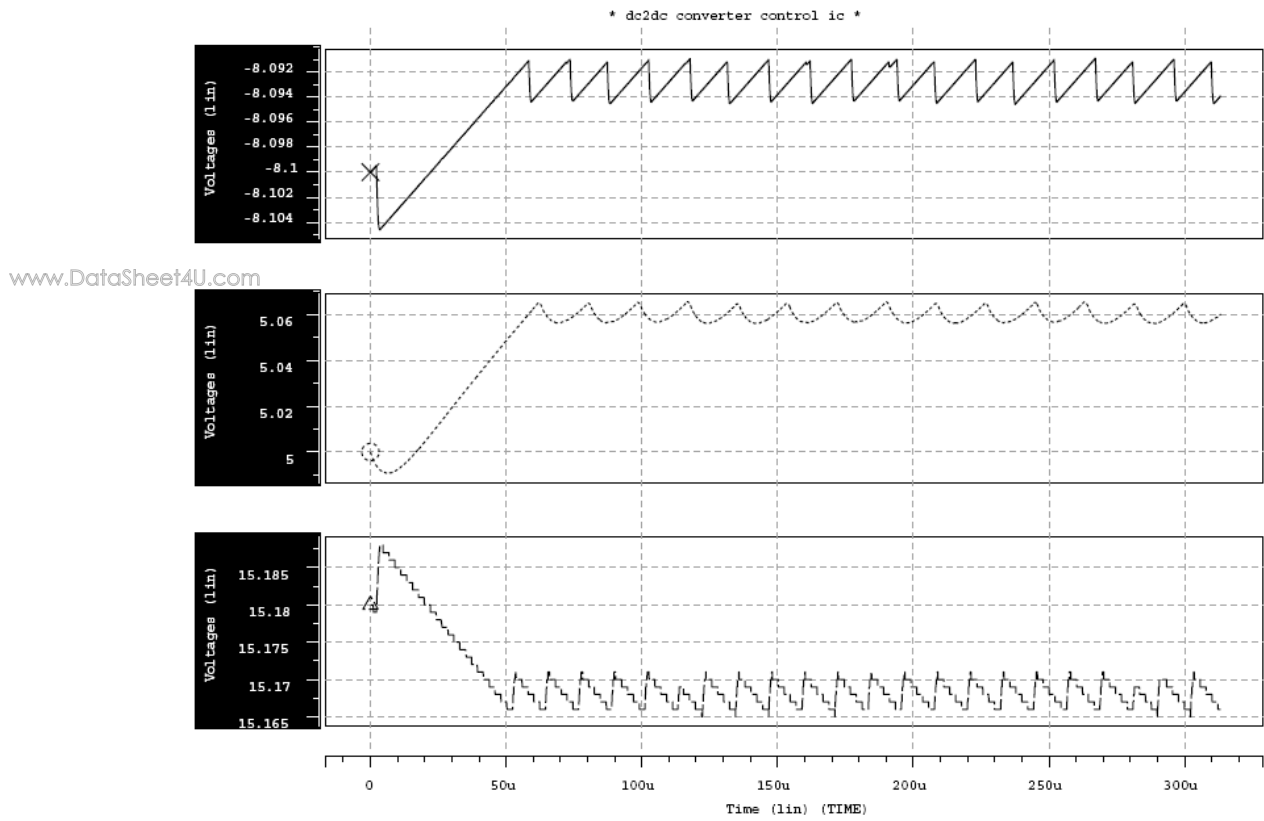


Figure 3. Internal oscillator & Maximum output voltage of the charge pump

Functional Block Diagrams and Application Circuits

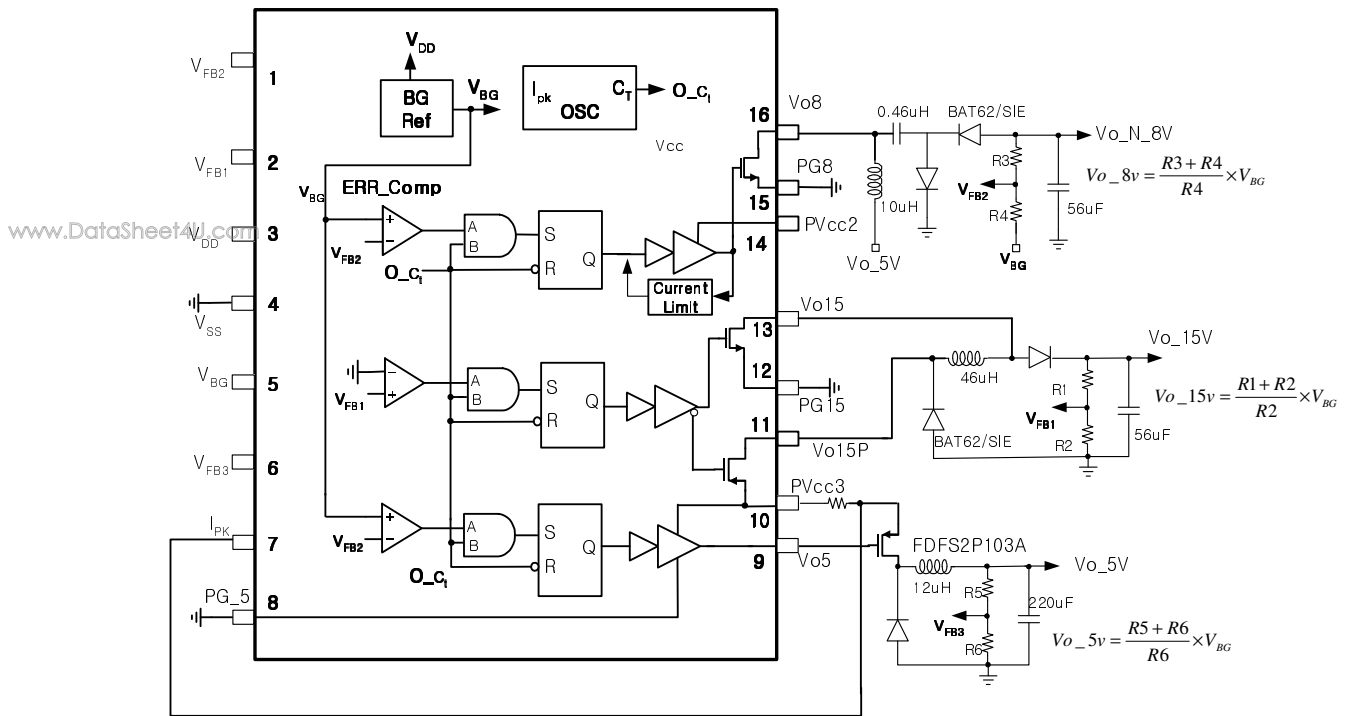


Figure 4. Functional Block Diagrams and Application Circuits

4. Functional Description

In figure 4., during ramping up portion of the cycle, the AND gate input "A" will be high. If the output voltage of switching regulator is below than target voltage, the AND gate input "B" will be high. This condition will set the latch and cause the "Q" output to be high enabling the driver and output switch to be on (for NFET switch case). When the oscillator reaches its upper threshold, Ct will start to discharge and the AND gate input will be low. The logic level is also connected to an inverter whose output produces a logic "high" to the reset input of the latch. This condition will cause "Q" to go low, which disables the driver out output switch.

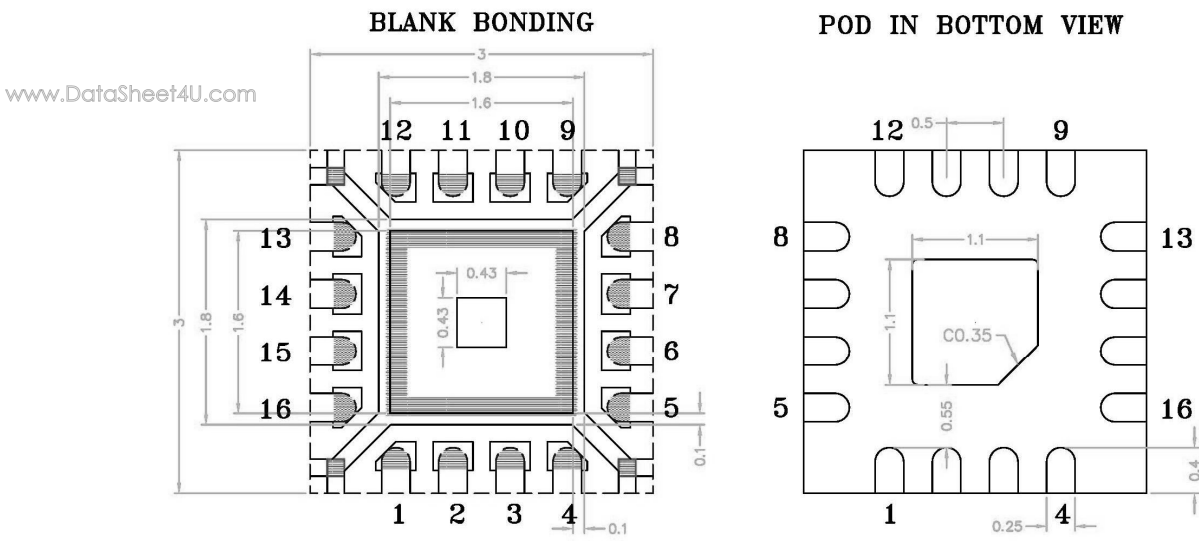
The comparator output can set the latch only during the ramp-up of Ct and can initiate a partial or full on-cycle of output switch conduction. Once the comparator has set the latch, it cannot reset it. The latch will remain set until Ct begins ramping down. Thus the comparator can initiate the output switch conduction, but cannot stop it and the latch is always reset when Ct begins remaining down.

The comparator's output will be "high" when the output voltage of the switching regulator is above target output voltage.

The current limiting is achieved by monitoring the voltage drop across an external sense resistor placed in series with supply and the output switch. The voltage drop developed across this resistor is monitored by the Ipk sense pin. When this voltage becomes greater than presetting offset voltage, the current limit circuit provides an additional current path to charge the timing capacitor Ct, which decreases the time of output switch conduction and reduces the amount of energy stored in the inductor. Operation of switching regulator in an overload or shorted condition will cause a very short but finite time of output conduction.

Package Dimensions (16-QFN)

16L QFN 3X3 /Lead pitch 0.5 mm.
Package thickness 0.9 mm. MAX.
Ag RING



RECOMMEND MIN DIE SIZE 0.43 X 0.43 mm.(17 X 17 MILS)
RECOMMEND MAX DIE SIZE 1.6 X 1.6 mm (63 X 63 mils)

All dimension in mm