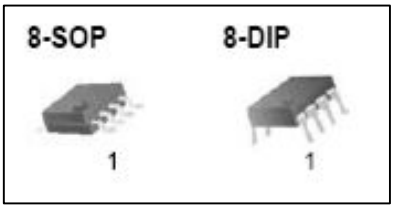
Green Mode PWM Controller

IK3401

Description



The IK3401 is a green mode PWM controller. It is specially designed for DVDP, STB and LCD monitor application.
To minimize standby power consumption, a green-mode function provides off-time modulation to continuously decrease the switching frequency at light-load conditions. Under zero-load conditions, the power supply enters burst-mode. To avoid acoustic noise problem, the minimum PWM frequency set above 20KHz. This green-mode function enables the power supply to easily meet international power conservation requirements. To further reduce power consumption, IK3401 is manufactured by using the HV-CMOS process. This allows the lowest start-up current around 14uA, and the operating current is only 4mA. As a result, large start-up resistance can be used.

The maximum power can be limited constantly, regardless of the line voltage change using power limit function. The switching frequency is programmable or internally fixed to be 65kHz.
IK3401 integrates frequency modulation technique internally. The frequency jittering function helps reduce EMI emission of a power supply with minimum line filters. Also, its built-in synchronized slope compensation achieves stable peak-current-mode control.
IK3401 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open loop or output short-circuit failure occurs. PWM output is disabled till VDD drops below the UVLO lower limit. Then, the controller starts up again. As long as VDD exceeds about 24V, the internal OVP circuit is triggered. For OVP and OTP, the protection mode can be chosen to be latch off or auto recovery.
IK3401 is available in an 8-pin DIP or SOP package.

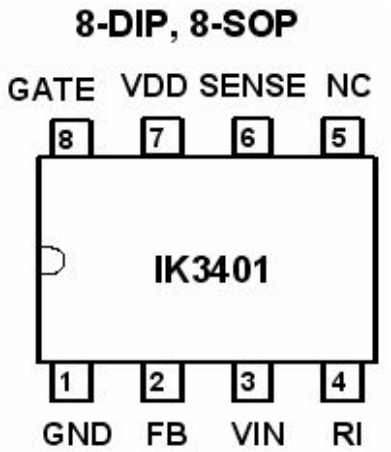
Features

- Green-mode PWM Control
- Low Start-Up Current (Typ. 14uA)
- Low Operating Current (Typ. 4mA)
- Programmable PWM frequency with Frequency Jittering
- Peak-current-mode Control
- Cycle-by-Cycle Current Limiting
- Synchronized Slope Compensation
- Leading-Edge Blanking
- Constant Output Power Limit
- Totem Pole Output with Soft Driving
- VDD Over Voltage Protection (OVP)
- 150°C OTP with Hysteresis
- Internal Latch Circuit (OVP, OTP)
- Internal Open-loop Protection
- VDD Under-voltage Lockout (UVLO)
- GATE Output Maximum Voltage Clamp (18V)

Applications

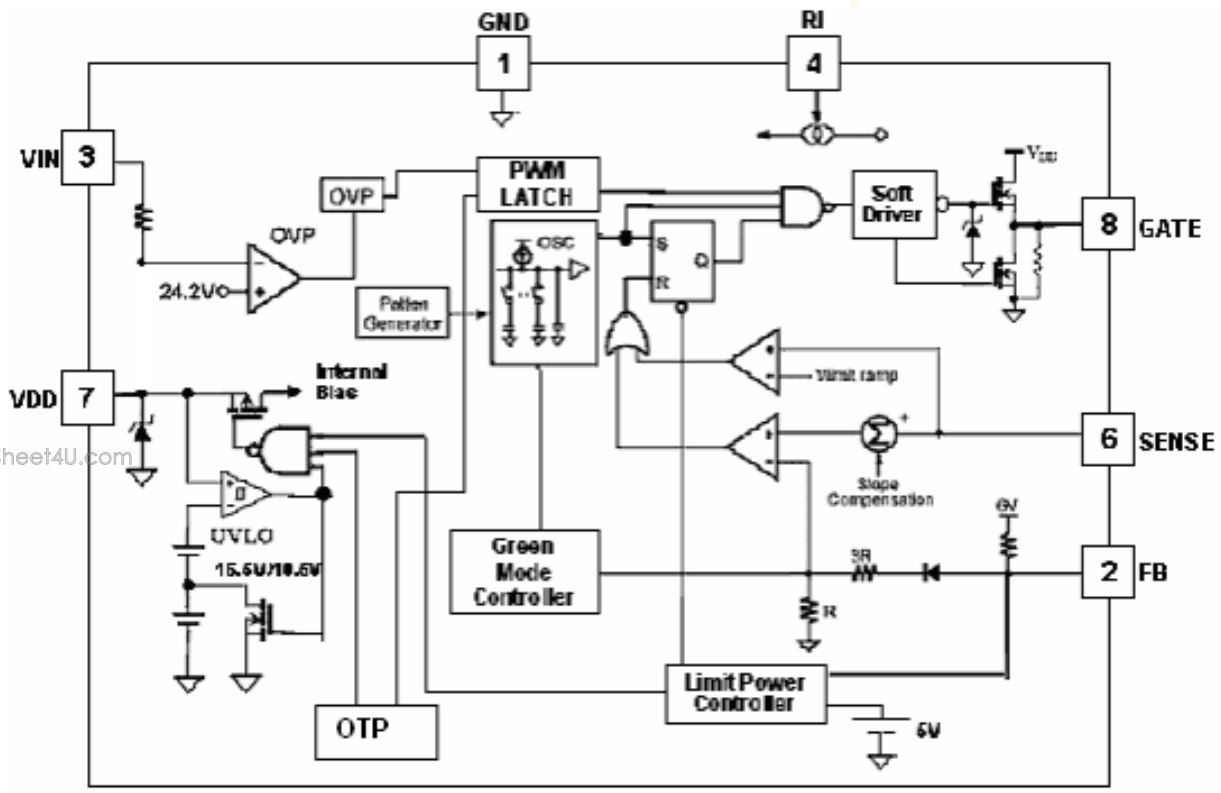
- Notebook Power Adapters
- DVD-P, STB, LCD Monitor Power
- Open-Frame SMPS

Pin Configuration



Pin	Symbol	Pin Description
1	GND	Ground
2	FB	Feedback
3	VIN	Start-up Input
4	RI	Reference Setting
5	NC	-
6	SENSE	Current Sense
7	VDD	IC Power Supply
8	GATE	Gate Drive Output

Block diagram



Absolute Maximum Ratings

(Ta = 25°C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DD}	Supply Voltage		25	V
V_{IN}	Input Terminal		25	V
V_{FB}	Input Voltage to FB Pin		-0.3 to 7V	V
V_{SENSE}	Input Voltage to SENSE Pin		-0.3 to 7V	V
V_{RI}	Input Voltage to RI Pin		-0.3 to 7V	V
P_D	Power Dissipation	at T_A < 50°C DIP SOP	800 400	mW
$R_{\Theta J-A}$	Thermal Resistance	Junction-Air DIP SOP	82.5 141	°C
T_J	Operating Junction Temperature		-40 to 125	°C
T_{STG}	Storage Temperature Range		-50 to 150	°C
T_L	Lead Temperature		260	°C
HBM	ESD Capability, HBM Model		3.0	kV
MM	ESD Capability, MM Model		250	V

Electrical Characteristics

(V_{DD} = 15V, T_A = 25°C, unless noted)

VDD Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OP}	Continuously Operating Voltage				22	V
V_{TH-ON}	Turn-on Threshold Voltage		15.5	16.5	17.5	V
V_{TH-OFF}	Turn-off Voltage		9.5	10.5	11.5	V
I_{DD-ST}	Start-up Current			14	30	uA
I_{DD-OP}	Operating Supply Current	Gate Open		4	5	mA
V_{DD-OVP}	V_{DD} Over Voltage Protection		23.2	24.2	25.2	V
$T_{VDD-OVP}$	V_{DD} OVP Debounce Time			100		usec

RI Section

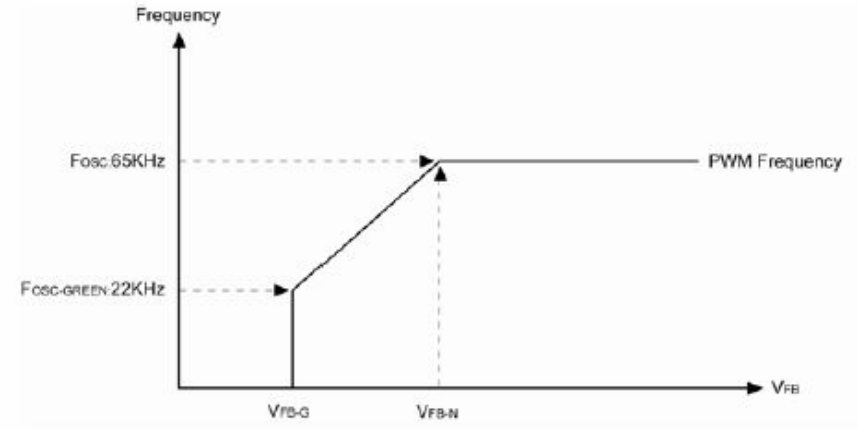
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{INOR}	R_I Operating Range		15.5		36	kΩ
RI_{MAX}	Max. R_I value for Protection			230		kΩ
RI_{MIN}	Min. R_I value for Protection			10		kΩ

Oscillator Section

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
F_{OSC}	Normal PWM Frequency	Center Frequency	R_I = 26kΩ	62	65	68	kHz
		Jitter Range		±3.7	±4.2	±4.7	kHz
T_{JTR}	Jittering Period		R_I = 26kΩ	3.9	4.4	4.9	ms
$F_{OSC-G-MIN}$	Min. R_I value for Protection		R_I = 26kΩ	18	22	25	kHz
F_{DV}	Frequency Variation vs V_{DD} Deviation					5	%
F_{DT}	Frequency Variation vs Temp. Deviation					5	%

Feedback Input Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
A_V	FB Input to Current Comparator Attenuation		1/4.5	1/4	1/3.5	V/V
Z_{FB}	Input Impedance		4		7	kΩ
$V_{FB-OPEN}$	Output High Voltage	FB Pin open	5.5			V
V_{FB-OLP}	FB open-loop trigger level		5		5.4	V/V
t_{D-OLP}	FB open-loop Protection Delay	R_I = 26kΩ	50	56	62	ms
V_{FB-N}	Green-Mode Entry FB Voltage	R_I = 26kΩ	1.9	2.1	2.3	V
V_{FB-G}	Green-Mode Ending FB Voltage	R_I = 26kΩ	V_{FB-N} -0.6	V_{FB-N} - 0.5	V_{FB-N} - 0.4	V
F_{G-TEST}	Burst Mode Test Frequency	V_{FB-G}+20mV	$F_{OSC-G-MIN}$ +0.5			kHz
I_{FB-ZDC}	Zero Duty FB Current				1.5	mA



Current Sense Section

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Z_{SENSE}	Input Impedance			12		kΩ
V_{STHFL}	Current Limit Flatten Threshold Voltage		0.85	0.9	0.95	V
V_{STHVA}	Current Limit Valley Threshold Voltage	V_{STHFL} -V_{STHVA}		0.22		V
DCY_{SAW}	Duty Cycle of SAW Limit	Max. Duty Cycle		45		%
t_{PD}	Propagation Delay to GATE Output	R_I=26 kΩ		150	200	ns
t_{LED}	Leading Edge Blanking Time	R_I=26 kΩ	200	270	350	ns

Gate Section

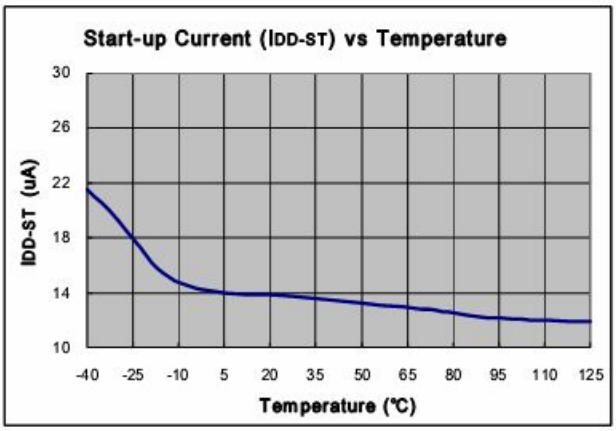
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DCY_{MAX}	Maximum Duty Cycle		80	85	90	%
V_{GL}	Output Voltage Low	V_{DD}=15V, I_O=50mA			1.5	V
V_{GH}	Output Voltage High	V_{DD}=12V, I_O=50mA	8			V
t_r	Rising Time	V_{DD}=15V, C_L=1nF	150	250	350	ns
t_f	Falling Time	V_{DD}=15V, C_L=1nF	30	50	90	ns
I_O	Peak Output Current	V_{DD}=15V, GATE=6V	230			mA
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD}=23V		18	19	V

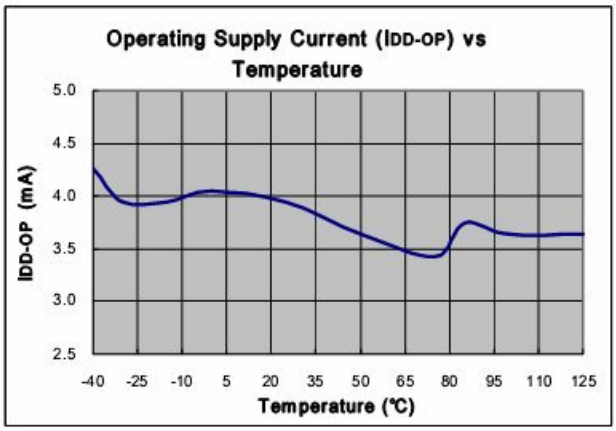
Over Temperature Protection (OTP)

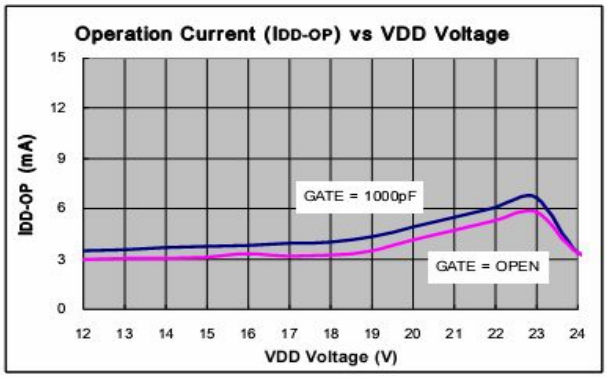
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Temp-Off	Protection Junction Temperature*1			150		°C
Temp-Restart	Restart Junction Temperature*2			130		°C

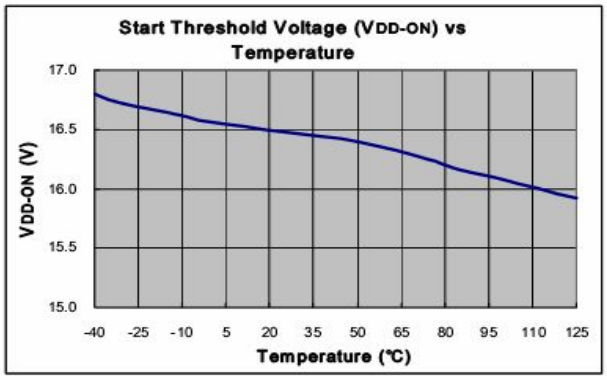
*1) When activated, the output is disabled and the latch is turned off.
*2) This is the threshold temperature for enabling the output again and resetting the latch, after over temperature protection has been activated.

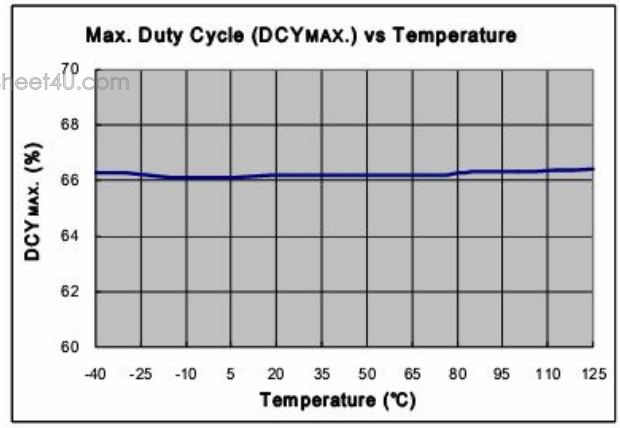
Typical Characteristics

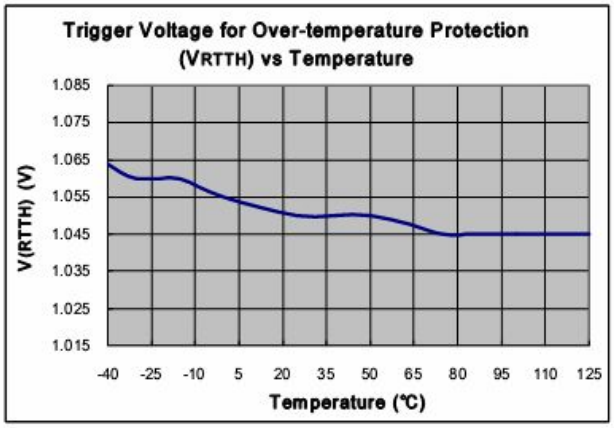


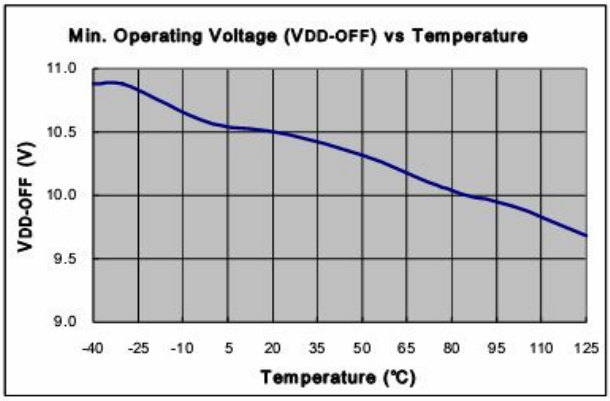


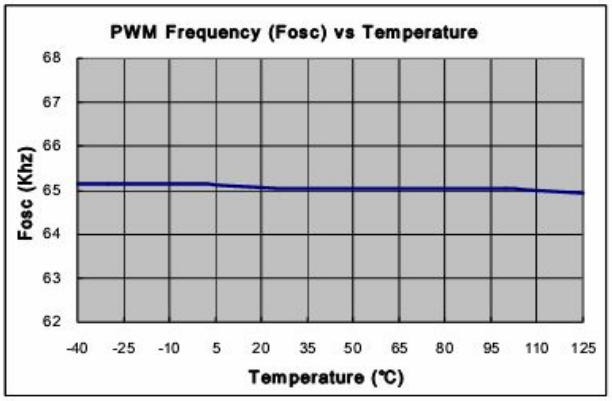


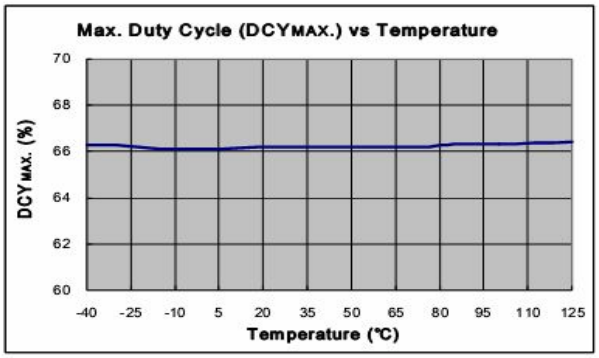


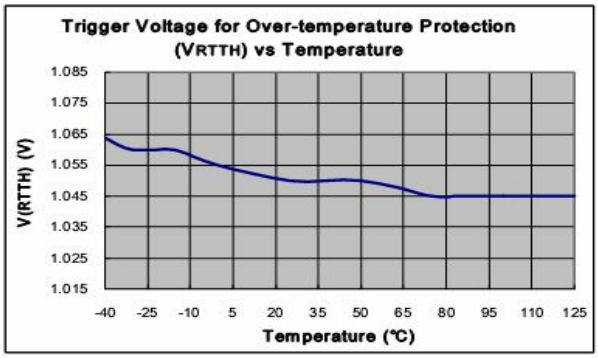












OPERATION DESCRIPTION

Start-Up Current

The typical start-up current is only 14uA. This allows a high resistance, low-wattage start-up resistor to be used, to minimize power loss. A 1.5MOhm, 0.25W, start-up resistor and a 10uF/25V VDD hold-up capacitor would be sufficient for an AC/DC adapter with a universal input range.

Operating Current

The required operating current has been reduced to 4mA. This results in higher efficiency and reduces the VDD hold-up capacitance requirement.

Green-Mode Operation.

The proprietary green-mode function provides off-time modulation to continuously decrease the PWM frequency under light-load conditions. To avoid acoustic-noise problem, the minimum PWM frequency set above 22KHz. This green-mode function dramatically reduces power consumption under light-load and zero-load conditions. Power supplies using a IK3401 Controller can easily meet even the most restrictive international regulations regarding standby power consumption.

Oscillator Operation

A resistor connected from the RI pin to GND pin generates a constant current source for the IK3401 controller. This current is used to determinate the center PWM frequency. Using a 26KOhm resistor RI results in a corresponding 65KHz PWM frequency. The relationship between RI and switching frequency is:

$$f_{PWM} = \frac{1690}{R_I\ (K\Omega)} (KHz) \quad \text{---------- (1)}$$

The range of the PWM oscillation frequency Is designed as 47KHz~109KHz.

IK3401 also integrates frequency hopping function internally. The frequency variation ranges from around 62KHz to 68KHz for a center frequency 65KHz. The frequency hopping function helps reduce EMI emission of a power supply with minimum line filters.

Leading Edge Blanking

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense-resistor. To avoid premature termination of the switching pulse, a leading-edge blanking time is build in. During this blanking period, the current-limit comparator is disabled, and it cannot switch off the gate drive.

Under-Voltage Lockout (UVLO)

The turn-on/turn-off thresholds are fixed internally at 16.5V/10.5V. To enable a IK3401 controller during start-up, the hold-up capacitor must first be charged to 16.5V through the start-up resistor.

The hold-up capacitor will continue to supply VDD before energy can be delivered from the auxiliary winding of the main transformer. VDD must not drop below 1035V during this start-up process. This UVLO hysteresis window ensures that the hold-up capacitor can adequately supply VDD during start-up.

Gate Output/Soft Driving

The IK3401 BiCMOS output stage is a fast totem pole gate driver. Cross-conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. The output driver is clamped by an internal 18V Zener diode in order to protect the power MOSFET transistors from any harmful over-voltage gate signals. A soft driving waveform is implemented to minimize EMI.

Slope Compensation

The sensed voltage across the current sense resistor is used for peak-current-mode control and cycle-by-cycle current limiting. The build-in slope compensation function improves power supply stability and prevents peak-current-mode control from causing sub-harmonic oscillations. Within every switching cycle, the IK3401 controller produces a positively sloped, synchronized ramp signal.

Constant Output Power Limit

When the SENSE voltage, across the sense resistor Rs, reaches the threshold voltage, around 0.85V, the output GATE drive will be turned off after a small delay t_{pd}. This delay will introduce an additional current proportional to t_{pd}*Vin/Lp. Since the delay is nearly constant regardless of the input voltage Vin . Higher input voltage will result in a larger additional current and hence the output power limit is also higher than under low input line voltage. To compensate this variation for wide AC input range, a saw-tooth power-limiter is designed to solve the unequal power-limit problem. The power limiter is designed as positive ramp signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inouts than at low-line inputs.

VDD Over-voltage Protection

VDD over-voltage protection has been built in to prevent damage voltage conditions. When the voltage VDD exceeds the internal threshold due to abnormal conditions, PWM output wil be latched off. Over-voltage conditions are usually caused by open feedback loops.

Limited Power Control

The FB voltage will increase every time the output of the power supply is shorted or over-loaded. If the FB voltage remains higher than a built-in threshold for longer than $t_{d\text{-}olp}$, PWM output will then be turned off. As PWM output is turned off, the supply voltage VDD will also begin decreasing.

When VDD goes below the turn-off threshold (eg, 10.5V) the controller will be totally shut down. VDD will be charged up to the turn-on threshold voltage of 16.5V through the start-up resistor until PWM output is restarted. This protection feature will continue to be activated as long as the over-loading condition persists. This will prevent the power supply from overheating due to over loading conditions.

Protection Latch Circuit

For the IK3401 family, the built-in latch function provides a versatile protection feature that does not require external components. To reset the latch circuit, it is necessary to disconnect the AC line voltage of the power supply.

Over Temperature Protection

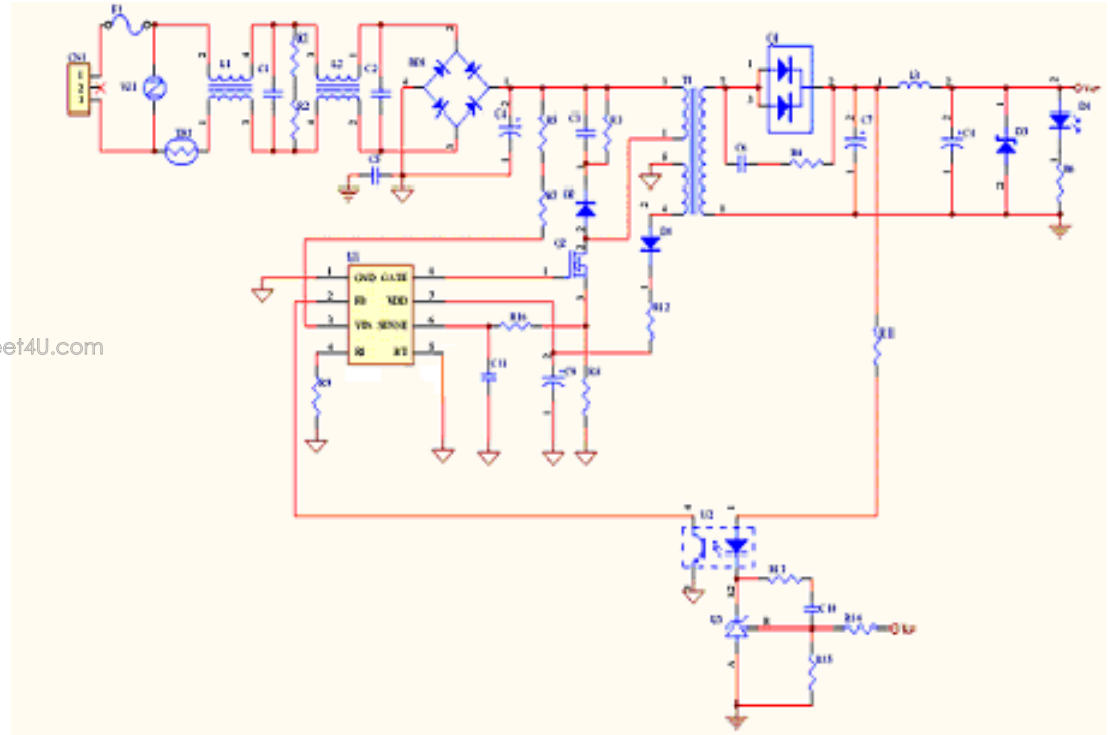
IK3401 has internal function of over temperature protection.

Noise Immunity

Noise from the current sense or the control signal may cause significant puls width jitter, particulary in continuous-conduction mode. Slope compensation helps alleviate this problem. Good placement and layout practices should be followed. The designer should avoiding long PCB traces and component leads. Compensation and filter components should be located near the IK3401. Finally, increasing the power-MOS gate resistance is advised.

REFERENCE APPLICATION

Circuit

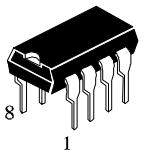


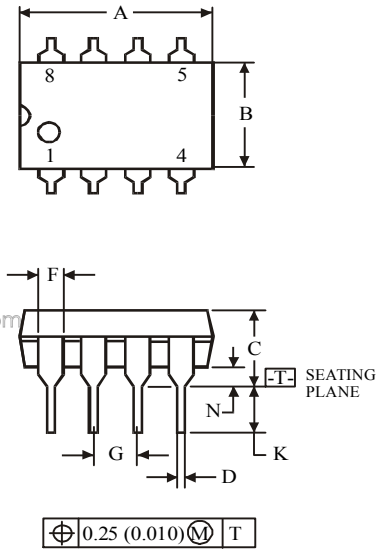
BOM

Reference	Component	Reference	Component
BD1	BD 4A/600V	R1,R2	R 1Mohm 1/4W
C1	XC 0.1uF/275V	R3	R 100Kohm 1/2W
C2	XC 0.22uF/275V	R4	R 47ohm 1/4W
C3	CC 0.01uF/500V	R5,R7	R 750Kohm 1/4W
C4	EC 120u/400V	R6	R 20Kohm 1/8W
C5	YC 222p/Y1	R8	R 0.3ohm 2W
C6	CC 1000pF/100V	R9	R 33Kohm 1/8W
C7	CC 1000pF/50V		
C8	EC 1000uF/35V	R11	R 220ohm 1/8W
C9	EC 220uF/35V	R12	R 4.7ohm 1/8W
C11	CC 470pF/50V	R13	R 6.8Kohm 1/8W
D1	LED	R14	R 154Kohm 1/8W
D2	Diode FR157	R15	R 390Kohm 1/8W
D3	ZD 18V	R16	R 100ohm 1/8W
D4	Diode FR102	THER1	Thermistor SCK054
F1	FUSE 4A/250V	T1	Transformer
L1	900uH	U1	IC IK3401
L2	15mH	U2	IC PC817
Q1	Diode 20A100V	U3	IC TL431
Q2	MOS 7A/600V	VZ1	VZ 9G

Package Outline Dimension

N SUFFIX PLASTIC DIP
(MS – 001BA)



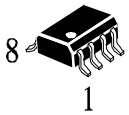


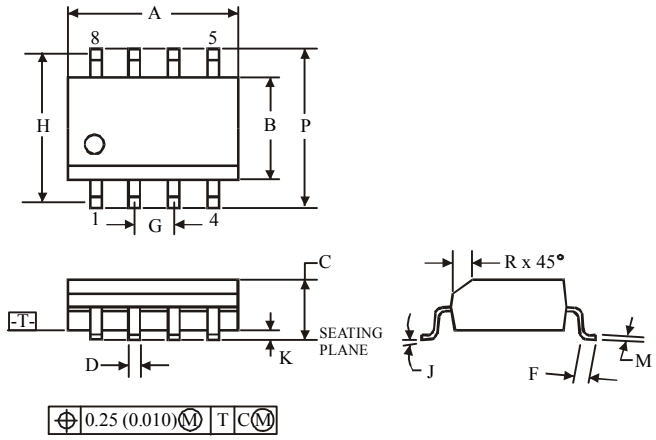
	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.
   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AA)





	Dimension, mm	
Symbol	**MIN**	**MAX**
A	4.8	5
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.72	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.