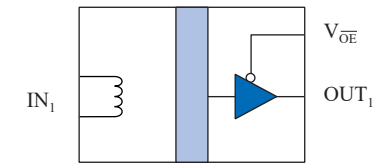
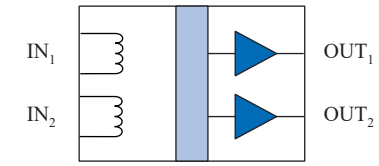
Passive-Input Digital Isolators – CMOS Outputs

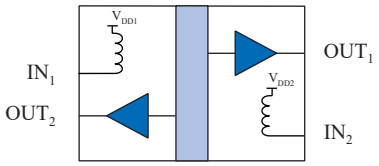
Functional Diagrams



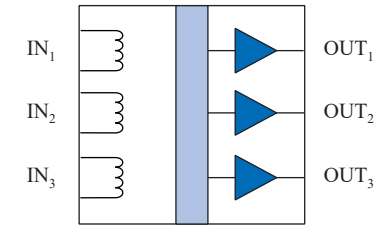
IL610



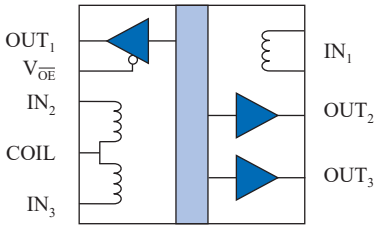
IL611



IL612



IL613



IL614

Features

- Up to 100 Mbps data rate
- Flexible inputs with very wide input voltage range
- 5 mA input current
- Failsafe output (logic high output for zero coil current)
- No carrier or clock for low EMI emissions and susceptibility
- Low power dissipation
- 3 V to 5 V power supplies
- 1000 V_{RMS}/1500 V_{DC} high voltage endurance
- 44000 year barrier life
- −40°C to 85°C temperature range
- UL 1577 recognized; IEC 60747-5-5 (VDE 0884) certified
- 8-pin MSOP, SOIC, and PDIP packages
- 0.15", 0.3", or True 8™ mm SOIC packages

Applications

- CAN Bus / Device Net
- Differential line receiver
- Optocoupler replacement
- SPI interface
- RS-485, RS-422, or RS-232
- Digital Fieldbus
- Space-critical multi-channel applications

Description

The IL600 Series are passive input digital signal isolators with CMOS outputs. They have a similar interface but better performance and higher package density than optocouplers.

The devices are manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology for small size, high speed, and low power.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

A resistor sets the input current; a capacitor in parallel with the current-limit resistor provides improved dynamic performance.

These versatile components simplify inventory requirements by replacing a variety of optocouplers, functioning over a wide range of data rates, edge speeds, and power supply levels. The devices are available in various packages, as well as bare die.

REV. AC

Absolute Maximum Ratings(1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	−55(2)		150	°C	
Ambient Operating Temperature	T_A	−40(3)		85	°C	
Supply Voltage	V_{DD}	−0.5		7	V	
DC Input Current	I_{IN}	−25		25	mA	
AC Input Current (Single-Ended Input)	I_{IN}	−35		35	mA	
AC Input Current (Differential Input)	I_{IN}	−75		75	mA	
Output Voltage	V_O	−0.5		V_{DD}+1.5	V	
Maximum Output Current	I_O	−10		10	mA	
ESD			2		kV	HBM

Note 1: Operating at absolute maximum ratings will not damage the device. Parametric performance is not guaranteed at absolute maximum ratings.
Note 2: -55ºC applies to all except IL611-1E. -20ºC applies to IL611-1E
Note 3: -40ºC applies to all except IL611-1E. -20ºC applies to IL611-1E

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	−40(3)		85	°C	
Supply Voltage	V_{DD}	3.0		5.5	V	
Output Current	I_{OUT}	−4		4	mA	
Common Mode Input Voltage	V_{CM}			400	V_{RMS}	

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)							
MSOP			3.01			mm	
0.15" SOIC			4.03			mm	
0.3" SOIC			8.03	8.3		mm	Per IEC 60601
PDIP			7.08			mm	
Total Barrier Thickness (internal)			0.012	0.013		mm	
Leakage Current				0.2		µA	240 V_{RMS}, 60 Hz
Barrier Resistance		R_{IO}		$>10^{14}$			500 V
Barrier Capacitance		C_{IO}		7		Ω || pF	f = 1 MHz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

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Safety and Approvals

IEC 60747-5-5 (VDE 0884) (File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Transient overvoltage (V_{IOTM}) and surge voltage (V_{IOSM}) 4000 V_{PK}
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	MSOP	150 V_{RMS}
-2	PDIP	300 V_{RMS}
-3	SOIC	150 V_{RMS}
None	Wide-body SOIC/True 8™	300 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)
Each part other than MSOP tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute
MSOP tested at 1200 V_{RMS} (1768 V_{PK}) for 1 second; each lot sample tested at 1500 V_{RMS} (2121 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C; MSL 1

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

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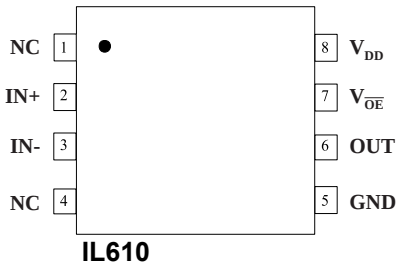
IL610 Pin Connections

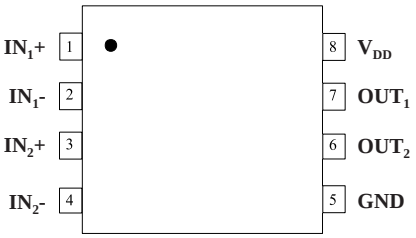
1	NC	No internal connection
2	IN+	Coil connection
3	IN−	Coil connection
4	NC	No internal connection
5	GND	Ground return for V_{DD}
6	OUT	Data out
7	$V_{\overline{OE}}$	Output enable. Internally held low with 100 kΩ
8	V_{DD}	Supply Voltage



IL610

IL611 Pin Connections

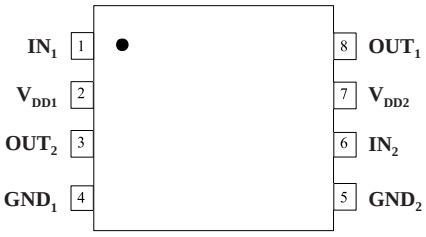
1	IN_1+	Channel 1 coil connection
2	IN_1-	Channel 1 coil connection
3	IN_2+	Channel 2 coil connection
4	IN_2-	Channel 2 coil connection
5	GND	Ground return for V_{DD}
6	OUT_2	Data out, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD}	Supply Voltage



IL611

IL612 Pin Connections

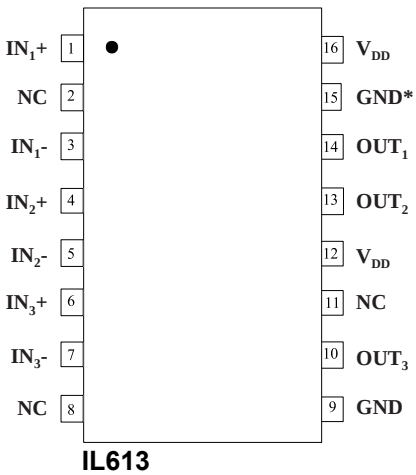
1	IN_1	Data in, channel 1
2	V_{DD1}	Supply Voltage 1
3	OUT_2	Data out, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	IN_2	Data in, channel 2
7	V_{DD2}	Supply Voltage 2
8	OUT_1	Data out, channel 1



IL612

IL613 Pin Connections

1	IN_1+	Channel 1 coil connection
2	NC	No connection (internally connected to pin 8)
3	IN_1-	Channel 1 coil connection
4	IN_2+	Channel 2 coil connection
5	IN_2-	Channel 2 coil connection
6	IN_3+	Channel 3 coil connection
7	IN_3-	Channel 3 coil connection
8	NC	No connection (internally connected to pin 2)
9	GND	Ground return for V_{DD} (internally connected to pin 15)
10	OUT_3	Data out, channel 3
11	NC	No connection
12	V_{DD}	Supply Voltage. Pin 12 and pin 16 must be connected externally
13	OUT_2	Data out, channel 2
14	OUT_1	Data out, channel 1
15	GND	Ground return for V_{DD} (internally connected to pin 9)
16	V_{DD}	Supply Voltage. Pin 12 and pin 16 must be connected externally



IL613

Note: Pins 12 and 16 must be connected externally.

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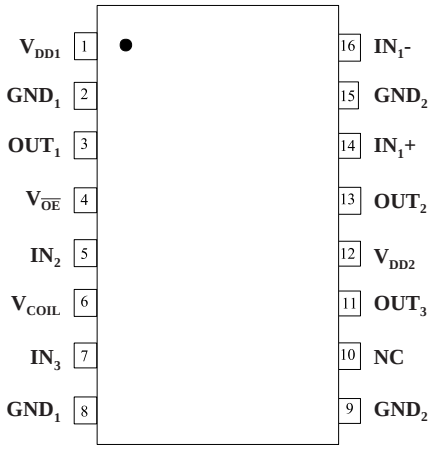
IL614 Pin Connections

1	V_{DD1}	Supply Voltage 1
2	GND_1	Ground return for V_{DD1} (internally connected to pin 8)
3	OUT_1	Data out, channel 1
4	$V_{\overline{OE}}$	Channel 1 data output enable. Internally held low with 100 kΩ
5	IN_2	Data in, channel 2
6	V_{coil}	Supply connection for channel 2 and channel 3 coils
7	IN_3	Data in, channel 3
8	GND_1	Ground return for V_{DD1} (internally connected to pin 2)
9	GND_2	Ground return for V_{DD2} (internally connected to pin 15)
10	NC	No Connection
11	OUT_3	Data out, channel 3
12	V_{DD2}	Supply Voltage 2
13	OUT_2	Data out, channel 2
14	IN_1+	Coil connection
15	GND_2	Ground return for V_{DD2} (internally connected to pin 9)
16	IN_1-	Coil connection



IL614

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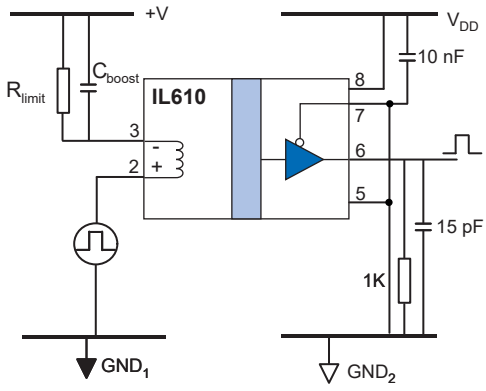
Operating Specifications

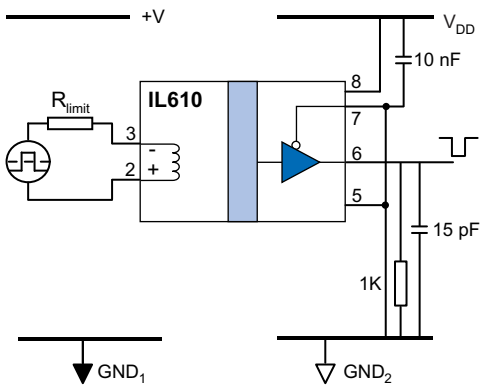
Input Specifications (V_{DD} = 3 V – 5.5 V; T = –40°C[2] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Coil Input Resistance	R_{COIL}	47	85	112	Ω	T = 25°C
		31	85	128	Ω	T = –40°C – 85°C
Coil Resistance Temperature Coefficient	TC R_{COIL}		0.2	0.25	Ω/°C	
Coil Inductance	L_{COIL}		9		nH	
DC Input Threshold (5 V)	I_{INH-DC}	0.5	1		mA	Test Circuit 1; V_{DD} = 4.5 V – 5.5 V
	I_{INL-DC}		3.5	5	mA	
DC Input Threshold (3 V)	I_{INH-DC}	0.3	0.5		mA	Test Circuit 1; V_{DD} = 3V – 3.6 V; no boost cap
	I_{INL-DC}		5	8	mA	
Dynamic Input Threshold (3 V)	$I_{INH-BOOST}$	0.5	1		mA	V_{DD} = 3V – 3.6 V; t_{IR} = t_{IF} = 3 ns; C_{BOOST} = 16 pF
	$I_{INL-BOOST}$		3.5	5	mA	
Differential Input Threshold	$I_{INH-DIFF}$	0.5	1		mA	Test Circuit 2; V_{DD} = 3V – 5.5 V; input current reverses; boost cap not required
	$I_{INL-DIFF}$		3.5	5	mA	
Failsafe Input Current[1] (5 V)	$I_{FS-HIGH}$	–25		0.5	mA	Test Circuit 1; V_{DD} = 4.5 V – 5.5 V
	I_{FS-LOW}	5		25	mA	
Failsafe Input Current[1] (3 V)	$I_{FS-HIGH}$	–25		0.3	mA	Test Circuit 1; V_{DD} = 3 V – 3.6 V
	I_{FS-LOW}	8		25	mA	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	µs	
Common Mode Transient Immunity	$\|CM_H\|$,$\|CM_L\|$	15	20		kV/µs	V_T = 300 V_{peak}

Notes:

1. Failsafe Operation is defined as the guaranteed output state which will be achieved if the DC input current falls between the input levels specified (see Test Circuit 1 for details). Note if Failsafe to Logic Low is required, the DC current supplied to the coil must be at least 8 mA using 3.3 V supplies versus 5 mA for 5 V supplies.
2. -20ºC for IL611-1E



Test Circuit 1 (Single-Ended)



Test Circuit 2 (Differential)

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5 V Electrical Specifications (V_{DD} = 4.5 V – 5.5 V; T = –40°C[5] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Quiescent Supply Current						
IL610	I_{DD}		2	3	mA	V_{DD} = 5 V, I_{IN} = 0
IL611	I_{DD}		4	6		
IL612	I_{DD1}		2	3		
IL612	I_{DD2}		2	3		
IL613	I_{DD}		6	9		
IL614	I_{DD1}		2	3		
IL614	I_{DD2}		4	6		
Logic High Output Voltage	V_{OH}	4.9	5		V	V_{DD} = 5 V, I_O = 20 µA
		4.0	4.8		V	V_{DD} = 5 V, I_O = 4 mA
Logic Low Output Voltage	V_{OL}		0	0.1	V	V_{DD} = 5 V, I_O = –20 µA
			0.2	0.8	V	V_{DD} = 5 V, I_O = –4 mA
Logic Output Drive Current	$\|I_O\|$	7	10		mA	

5 V Switching Specifications (V_{DD} = 4.5 V – 5.5 V; T = –40°C[5] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Data Rate		100			Mbps	Test Circuit 1; t_{IR} = t_{IF} = 3 ns; C_{BOOST} = 16 pF
Minimum Pulse Width[1]	PW	10			ns	
Propagation Delay Input to Output (High-to-Low)	t_{PHL}		8	15	ns	
Propagation Delay Input to Output (Low to High)	t_{PLH}		8	15	ns	
Average Propagation Delay Drift	t_{PLH}		10		ps/°C	
Pulse Width Distortion $\|t_{PHL}–t_{PLH}\|$[2]	PWD		3	5	ns	
Pulse Jitter[3]	t_J			100	ps	
Propagation Delay Skew[4]	t_{PSK}	–2		2	ns	
Output Rise Time (10–90%)	t_R		2	4	ns	
Output Fall Time (10–90%)	t_F		2	4	ns	

Notes:

1. Minimum Pulse Width is the shortest pulse width at which the specified PWD is guaranteed.
2. PWD is defined as $\| t_{PHL} - t_{PLH} \|$.
3. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.
4. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
5. -20ºC for IL611-1E

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3.3 V Electrical Specifications (V_{DD} = 3 V – 3.6 V; T = –40°C[4] – 85°C unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Quiescent Supply Current						
IL610	I_{DD}		1.3	2	mA	V_{DD} = 3.3 V, I_{IN} = 0
IL611	I_{DD}		2.6	4		
IL612	I_{DD1}		1.3	2		
IL612	I_{DD2}		1.3	2		
IL613	I_{DD}		4	6		
IL614	I_{DD1}		1.3	2		
IL614	I_{DD2}		2.6	4		
Logic High Output Voltage	V_{OH}	3.2	3.3		V	V_{DD} = 3.3 V, I_O = 20 µA
		3.0	3.1		V	V_{DD} = 3.3 V, I_O = 4 mA
Logic Low Output Voltage	V_{OL}		0	0.1	V	V_{DD} = 3.3 V, I_O = –20 µA
			0.2	0.8	V	V_{DD} = 3.3 V, I_O = –4 mA
Logic Output Drive Current	$\|I_O\|$	7	10		mA	

3.3 V Switching Specifications (V_{DD} = 3 V – 3.6 V; T = –40°C[4] – 85°C unless otherwise stated)						
Data Rate		100			Mbps	Test Circuit 1; t_{IR} = t_{IF} = 3 ns; C_{BOOST} = 16 pF
Minimum Pulse Width[1]	PW	10			ns	
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	
Average Propagation Delay Drift	t_{PLH}		10		ps/°C	
Pulse Width Distortion $\|t_{PHL} – t_{PLH}\|$ [2]	PWD		3	5	ns	
Propagation Delay Skew[3]	t_{PSK}	–2		2	ns	
Output Rise Time (10–90%)	t_R		3	5	ns	
Output Fall Time (10–90%)	t_F		3	5	ns	

Notes:

1. The Minimum Pulse Width is the shortest pulse width at which the specified PWD is guaranteed.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$.
3. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at 25°C.
4. -20ºC for IL611-1E

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Applications Information

IL600-Series Isolators are current mode devices. Changes in current flow into the input coil result in logic state changes at the output. As shown in Figure 1, output logic high is the zero input current state.

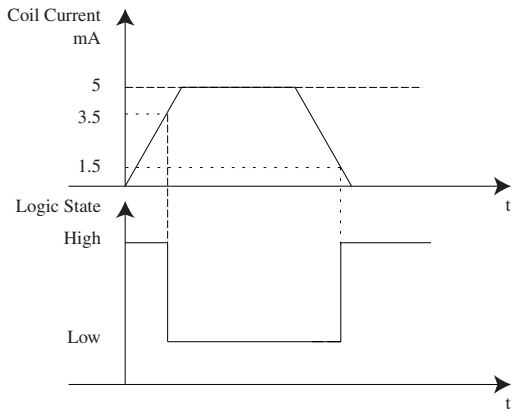

Figure 1. Typical IL600-Series Transfer Function

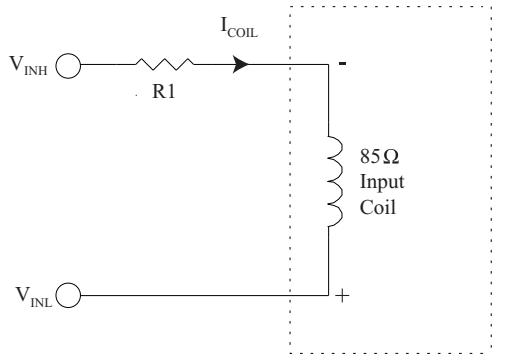

Figure 2. Limiting Resistor Calculation Equivalent Circuit

Coil Polarity

The device switches to logic low if current flows from (In−) to (In+). ***Note that the designations "In−" and "In+" refer to logic levels, not current flow.*** Positive values of current mean current flow into the In− input.

Input Resistor Selection

Resistors set the coil input current (see Figure 2). There is no limit to input voltages because there are no semiconductor input structures.

Worst-case logic low threshold current is 8 mA, which is for single-ended operation with a 3 V supply. In differential mode, where the input current reverses, the logic low threshold current is 5 mA for the range of supplies. A "boost capacitor" creates current reversals at edge transitions, reducing the input logic low threshold current to the differential level of 5 mA.

Typical Resistor Values

V_{COIL}	0.125W, 5% Resistor
3.3 V	510 Ω
5 V	820 Ω

The table shows typical values for the external resistor for 5 mA coil current. The values are approximate and should be adjusted for temperature or other application specifics. If the expected temperature range is large, 1% tolerance resistors may provide additional design margin.

Single-Ended or Differential Input

The IL610, IL611, IL613, and channel 1 of the IL614 can be run with single-ended or differential inputs (see Test Circuits on page 5). In the differential mode, current will naturally flow through the coil in both directions without a boost capacitor, although the capacitor can still be used for increased external field immunity or improved PWD.

Absolute Maximum recommended coil current in single-ended mode is 25 mA while differential mode allows up to ±75 mA to flow. The difference in specifications is due to the risk of electromigration of coil metals under constant current flow. In single ended mode, long-term DC current flow above 25 mA can cause erosion of the coil metal. In differential mode, erosion takes place in both directions as each current cycle reverses and has a net effect of zero up to the absolute maximum current.

An advantage over optocouplers and other high-speed couplers in differential mode is that no reverse bias protection for the input structure is required for a differential signal.

One of the more common applications is for an isolated Differential Line Receiver. For example, RS-485 can drive an IL610 directly for a fraction of the cost of an isolated RS-485 node (see *Illustrative Applications*).

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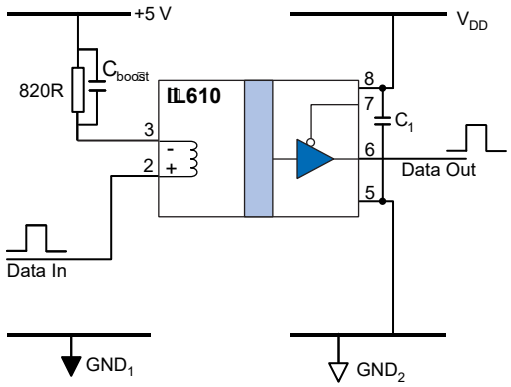
Non-inverting and Inverting Configurations

IL600-Series Isolators can be configured in non-inverting and inverting configurations (see Figure 3). In a typical non-inverting circuit, the In− terminal is connected via a 1 kΩ input resistor to the supply rail, and the input is connected to the In+ terminal. The supply voltage is +5 V and the input signal is a 5 V CMOS signal. When a logic high (+5 V) is applied to the input, the current through the coil is zero. When the input is a logic low (0 V), at least 5 mA flows through the coil from the In− side to the In+ side.

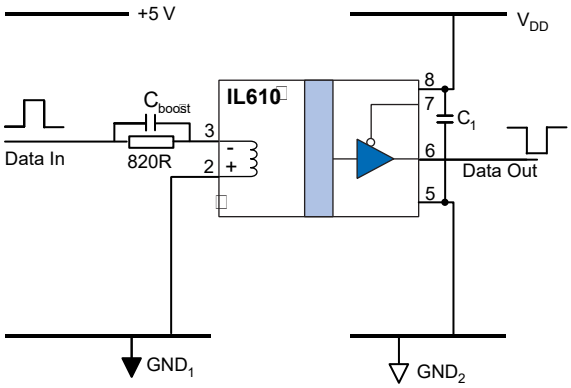
The inverting configuration is similar to standard logic. In the inverting configuration, the signal into the coil is differential with respect to ground. The designer must ensure that the difference between the logic low voltage and the coil ground is such that the residual coil current is less than 0.5 mA.

The IL612 and IL614 devices have some inputs that do not offer inverting operation. The IL612 coil In− input is hardwired internally to the device power supply; therefore it is important to ensure the isolator power supply is at the same voltage as the power supply to the source of the input logic signal. The IL614 has a common coil In− for two inputs. This pin should be connected to the power supply for the logic driving channels 2 and 3, and the channels run should be run in non-inverting mode.

Both single ended and differential inputs can be handled without reverse bias protection.



Non-Inverting Circuit Note: C_1 is 47 nF ceramic.



Inverting Circuit Note: C_1 is 47 nF ceramic.

Figure 3. Non-inverting and inverting circuits

Boost Capacitor

The boost capacitor in parallel with the current-limiting resistor boosts the instantaneous coil current at the signal transition. This ensures switching and reduces propagation delay and reduces pulse-width distortion.

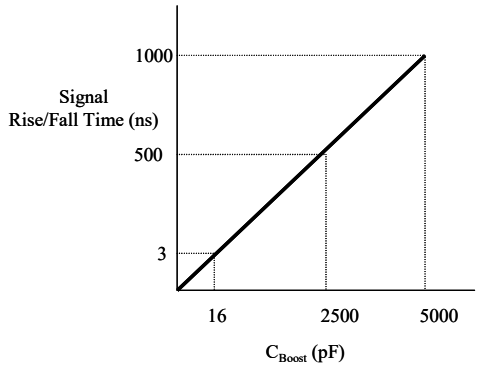


Figure 4. C_{boost} Selector

Select the value of the boost capacitor based on the rise and fall times of the signal driving the inputs. The instantaneous boost capacitor current is proportional to input edge speeds ($C\frac{dV}{dt}$). Select a capacitor value based on the rise and fall times of the input signal to be isolated that provides approximately 20 mA of additional "boost" current. Figure 4 is a guide to boost capacitor selection. For high-speed logic signals (t_r,t_f < 10 ns), a 16 pF capacitor is recommended. The capacitor value is generally not critical; if in doubt, choose a higher value.

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Dynamic Power Consumption

Power consumption is proportional to duty cycle, not data rate. The use of NRZ coding minimizes power dissipation since no additional power is consumed when the output is in the high state. In differential mode, where the logic high condition may still require a current to be forced through the coil, power consumption will be higher than a typical NRZ single ended configuration.

Power Supply Decoupling

47 nF low-ESR ceramic capacitors are recommended to decouple the power supplies. The capacitors should be placed as close as possible to the appropriate V_{DD} pin.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Electromagnetic Compatibility and Magnetic Field Immunity

Because IL600-Series Isolators are completely static, they have the lowest emitted noise of any non-optical isolators.

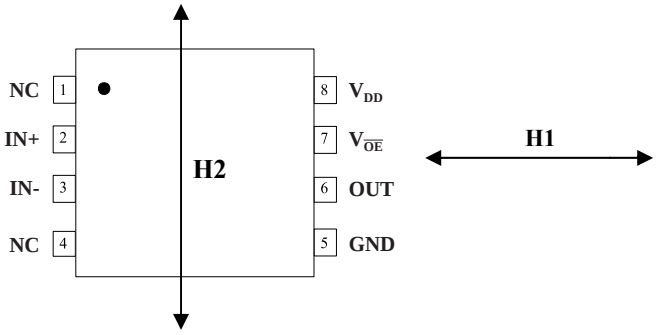
IsoLoop Isolators operate by imposing a magnetic field on a GMR sensor, which translates the change in field into a change in logic state. A magnetic shield and a Wheatstone Bridge configuration provide good immunity to external magnetic fields.

Immunity to external magnetic fields can be enhanced by proper orientation of the device with respect to the field direction, the use of differential signaling, and boost capacitors.

1. Orientation of the device with respect to the field direction

An applied field in the "H1" direction is the worst case for magnetic immunity. In this case the external field is in the same direction as the applied internal field. In one direction it will tend to help switching; in the other it will hinder switching. This can cause unpredictable operation.

An applied field in direction "H2" has considerably less effect and results in higher magnetic immunity.



2. Differential Signaling and Boost Capacitors

Regardless of orientation, driving the coil differentially improves magnetic immunity. This is because the logic high state is driven by an applied field instead of zero field, as is the case with single-ended operation. The higher the coil current, the higher the internal field, and the higher the immunity to external fields. Optimal magnetic immunity is achieved by adding the boost capacitor.

Method	Approximate Immunity	Immunity Description
Field applied in H1 direction	±20 Gauss	A DC current of 16 A flowing in a conductor 1 cm from the device could cause disturbance.
Field applied in H2 direction	±70 Gauss	A DC current of 56 A flowing in a conductor 1 cm from the device could cause disturbance.
Field applied in any direction but with boost capacitor (16 pF) in circuit	±250 Gauss	A DC current of 200 A flowing in a conductor 1 cm from the device could cause disturbance.

Data Rate and Magnetic Field Immunity

It is easier to disrupt an isolated DC signal with an external magnetic field than it is to disrupt an isolated AC signal. Similarly, a DC magnetic field will have a greater effect on the device than an AC magnetic field of the same effective magnitude. For example, signals with pulses longer than 100 µs are more susceptible to magnetic fields than shorter pulse widths.

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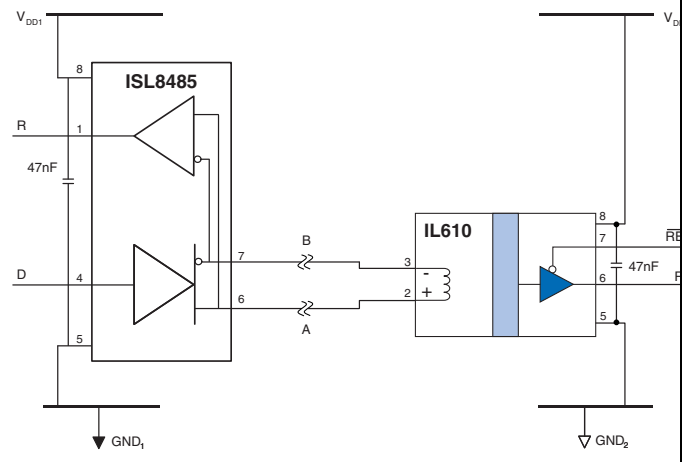
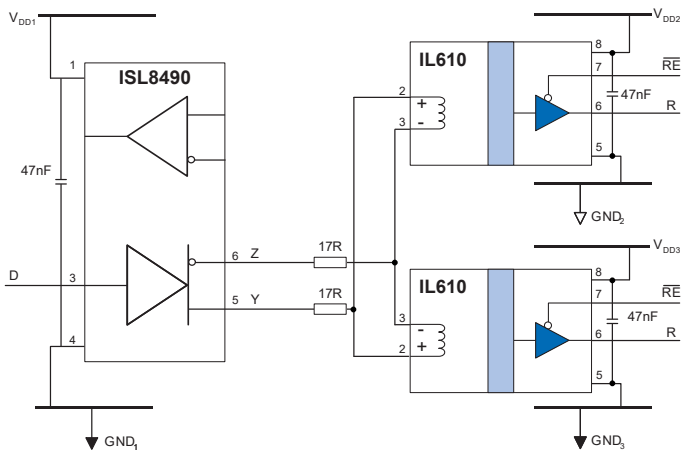
Illustrative Applications





Isolated RS-485 and RS-422 Receivers Using IL610s

IL610s can be used as simple isolated RS-485 or RS-422 receivers, terminating signals at the IL610 for a fraction of the cost of an isolated node. Cabling is simplified by eliminating the need to power the input side of the receiving board. No current-limiting resistor is needed for a single receiver because it will draw less current than the driver maximum. Current limiting resistors allow at least eight nodes without exceeding the maximum load of the transceiver. Placement of the current-limiting resistors on both lines provides better dynamic signal balance. There is generally no need for line termination resistors below data rates of approximately 10 Mbps because the IL610 coil resistance of approximately 85 Ω is close to the characteristic impedance of most cables. The circuit is intrinsically open-circuit failsafe because the IL610 is guaranteed to switch to the high state when the coil input current is less than 0.5 mA.

Number of Nodes	Current Limit Resistors (Ω)
1	None
2	17
3	22
4	27
5	27
6	27
7	30
8	33

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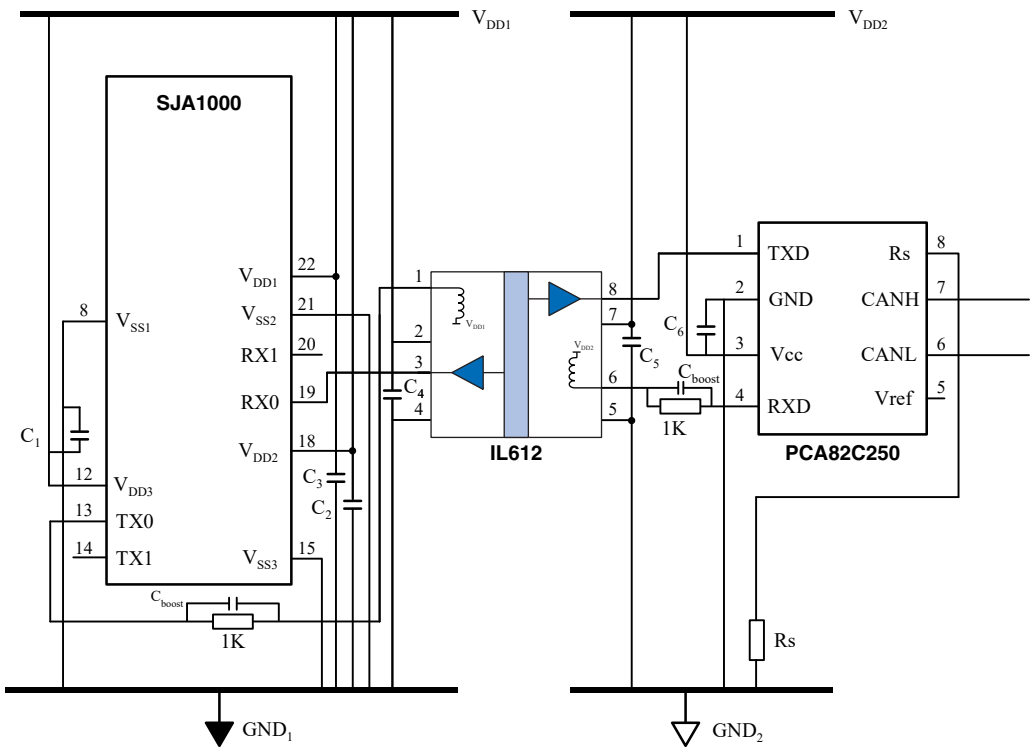
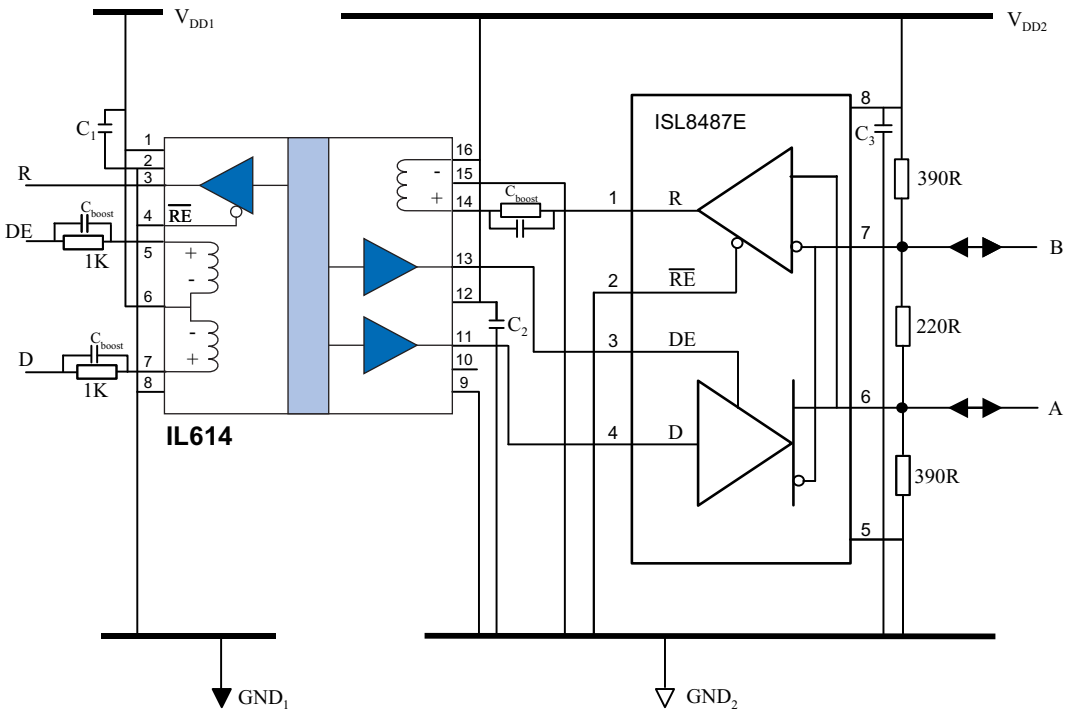


Isolated CAN Bus

Low pulse width distortion is critical for CAN bus, and IL600 Isolators are specified for just 3 ns typical pulse width distortion. Their fail-safe output (logic high output for zero coil current) ensures proper power-on. The speed of IL600 isolators easily supports the maximum CAN bus transfer speed of 1 Mbps.



Isolated RS-485 – Fractional Load

The unique IL614 three-channel isolator can be used as part of a multi-chip design with a variety of non-isolated transceivers. The IL614 provides 2.5 kV_{RMS} isolation (1 minute) and 20 kV/µs transient immunity. The IL614-3 is in a narrow-body (0.15 inch-wide) package when board space is critical.

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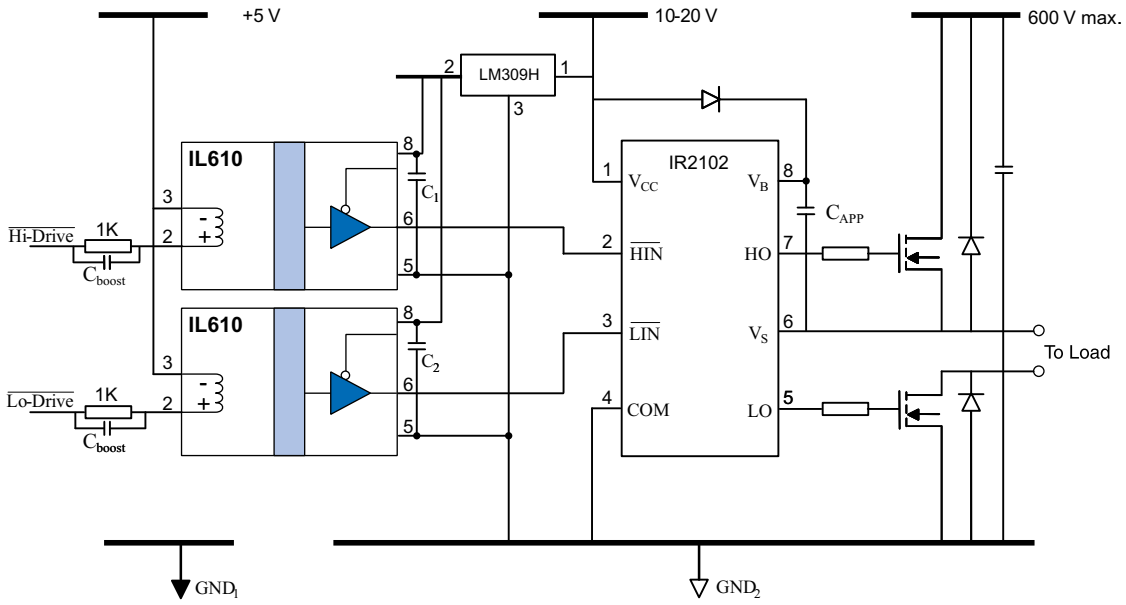
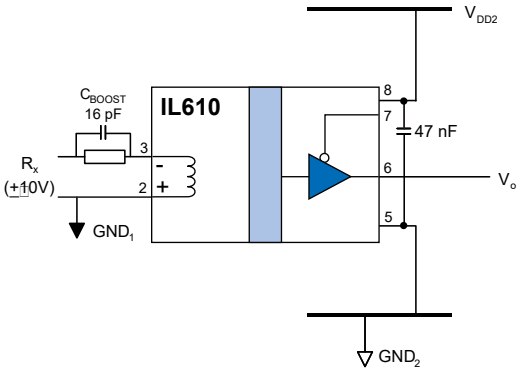


Notes:
C_{boost} is 16 pF
C_{APP} is application specific
All other capacitors are 47 nF ceramic

Single-Phase Power Control

The fail-safe output (logic high output for zero coil current) of IL600 Isolators ensures power FETs will be off on power-up. The IL600 inputs can be configured for inverting or non-inverting operation (see Applications Information).



Notes:
C_{BOOST} is 16pF ceramic
C1 and C2 are 47 nF ceramic

Isolated RS-232 Receiver Using IL610

An IL610 can be used as a simple isolated RS-232 receiver. Most RS-232 nodes have at least 5 mA drive capability to switch the IL610. Cabling is simplified by eliminating the need to power the input side of the receiving board. A similar circuit can be used for RS-422/RS-485, LVDS, or other differential networks. The IL610-1 is a unique MSOP isolator when board space is critical.

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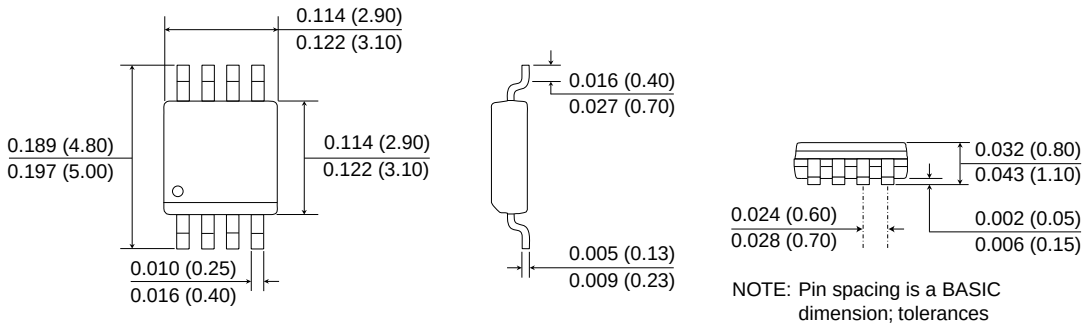
Package Drawings

8-pin MSOP (-1 suffix)

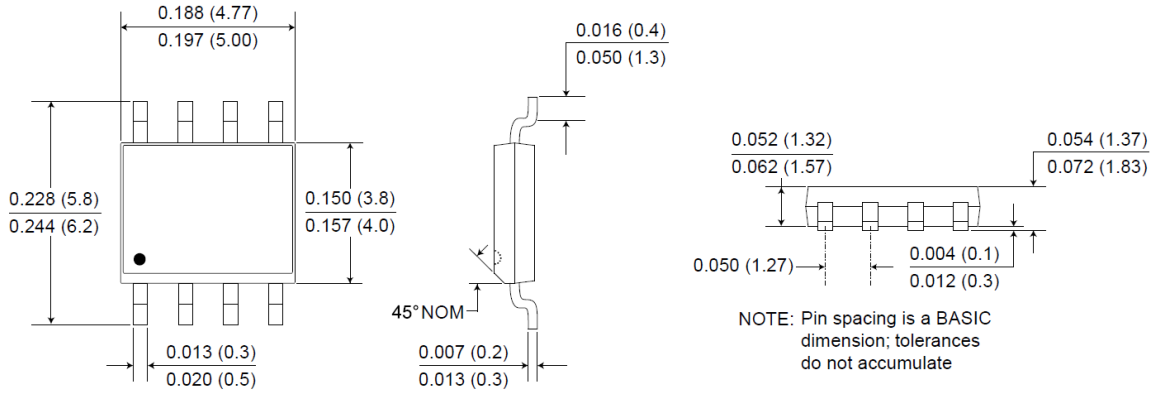
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

8-pin SOIC Package (-3 suffix)

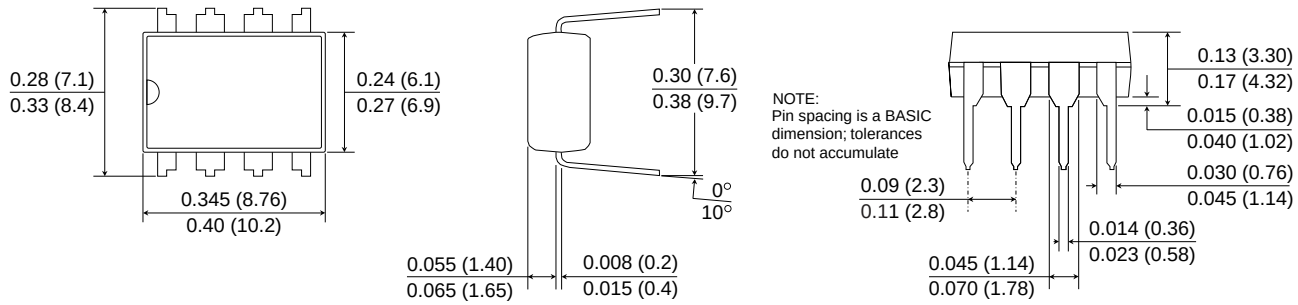
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

8-pin PDIP (-2 suffix)

Dimensions in inches (mm); scale = approx. 2.5X



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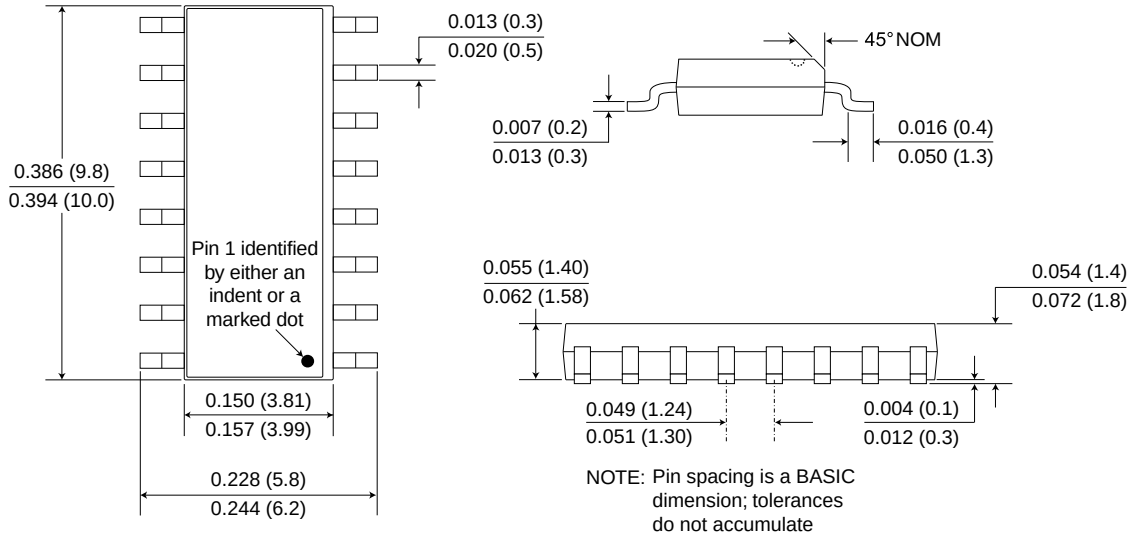
0.15" 16-pin SOIC Package (-3 suffix)

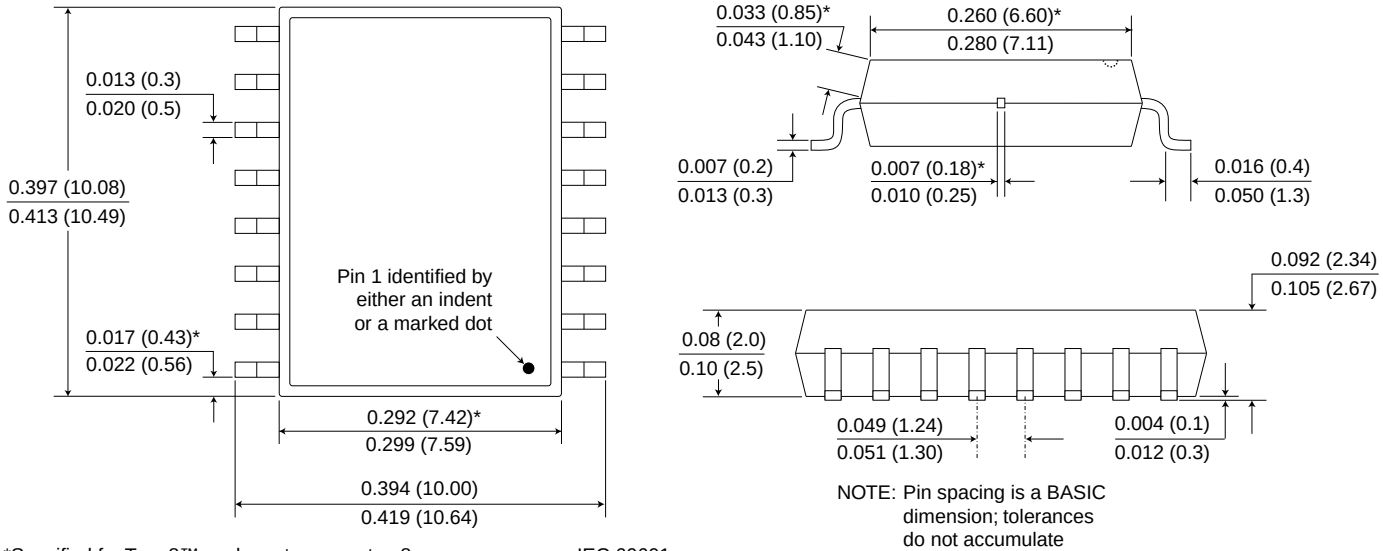
Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

0.3" 16-pin SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X



NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

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Ordering Information and Valid Part Numbers

IL 610 - 1 E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
E = RoHS Compliant

Package Type
Blank = 0.3" SOIC
-1 = MSOP
-2 = PDIP
-3 = 0.15" SOIC
-5 = Bare die

Base Part Number
610 = Single Channel
611 = 2 Drive Channels
612 = 1 Drive Channel, 1 Receive Channel
613 = 3 Drive Channels
614 = 2 Drive Channels, 1 Receive Channel

Product Family
IL = Isolators

IL610 Valid Part Numbers

IL610-1E
IL610-2E
IL610-3E
IL610-5

IL611 Valid Part Numbers

IL611-1E
IL611-2E
IL611-3E

IL612 Valid Part Numbers

IL612-2E
IL612-3E

IL613 Valid Part Numbers

IL613E
IL613-3E

IL614 Valid Part Numbers

IL614E
IL614-3E

All MSOP and SOIC part types are available on tape and reel.

RoHS COMPLIANT

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Revision History

ISB-DS-001-IL600-AC
March 2017

Changes
- Corrected 8-pin SOC Package outline dimensions.
- Changed low temperature specification for IL611-1E to -20ºC.

ISB-DS-001-IL600-AB

Changes
- IEC 60747-5-5 (VDE 0884) certification.
- Upgraded from MSL 2 to MSL 1.
- Rearranged input threshold specifications so maximum is more than minimum.

ISB-DS-001-IL600-AA

Changes
- Added VDE 0884 pending.
- Updated package drawings.
- Added recommended solder pad layouts.
- Clarified circuit polarities.

ISB-DS-001-IL600-Z

Changes
- Detailed isolation and barrier specifications.
- Cosmetic changes.

ISB-DS-001-IL600-Y

Changes
- Clarified Test Circuit 2 differential operation diagram (p.5).

ISB-DS-001-IL600-X

Changes
- Separated and clarified Input Specifications.
- Added minimum/maximum coil resistance specifications.
- Merged and simplified “Operation” and “Applications” sections.

ISB-DS-001-IL600-W

Changes
- Update terms and conditions.

ISB-DS-001-IL600-V

Changes
- Additional changes to pin spacing specification on MSOP drawing.

ISB-DS-001-IL600-U

Changes
- Changed pin spacing specification on MSOP drawing.

ISB-DS-001-IL600-T

Changes
- Added typical jitter specification at 5V.

ISB-DS-001-IL600-S

Changes
- P. 2—Deleted MSOP IEC61010 approval.

ISB-DS-001-IL600-R

Changes
- Added EMC details.

ISB-DS-001-IL600-Q

Changes
- IEC 61010 approval for MSOP versions.

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ISB-DS-001-IL600-P

Changes

- Specified coil resistance as typical only.
- Revised section on calculating limiting resistors.

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ISB-DS-001-IL600-AC

March 2017