VERTICAL DEFLECTION AMPLIFIER CIRCUIT

(functional equivalent of TDA8359J Philips)

IC ILA8359 - powerful integrated circuit designed for use in 90^{o} and 110^{o} deflection system of color TV sets. It includes frame deflecting bridge output, which operates as a high efficient class G amplifier. IC ILA8359 can operates with 25 to 200 Hz field frequencies and vertical deflection coils of 4:3 and 16:9 picture tubes. The full bridge output circuit allows to use IC in applications with 12 V power supply voltage and 45 V flyback supply voltage (depends on the configuration of deflection coils).

ILA8359 chip is designed on the basis of low voltage DMOS process, which included bipolar, CMOS and DMOP structures. DMOP output transistors (MOSFETs), are used in the output stage because of absence of secondary breakdown, to provide the best SOAR features. The internal circuit design allows to adjust correctly device operation using a small quantity of external components.

Main features:

- Small quantity of external components required;
- High efficiency fully DC coupled vertical bridge output circuit;
- Vertical flyback switch with short rise and fall times;
- Built-in guard circuit (to prevent tube damage);
- Thermal protection circuit;
- Differential mode of inputs;
- Improved EMC performance due to differential inputs.

IC is realized in 9 – pin plastic DIL-SIL power case 1509.9-A.

Permissible value of ESD potential 2000 V.

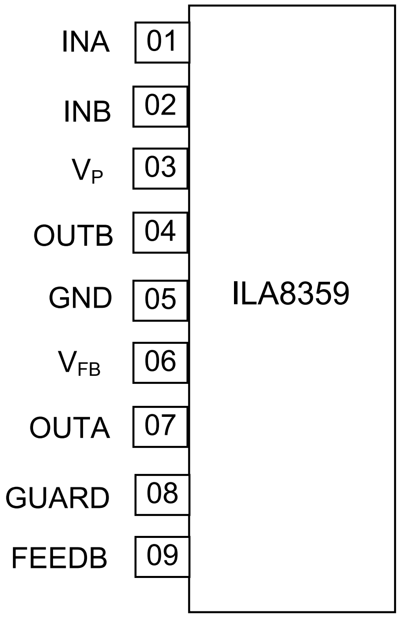
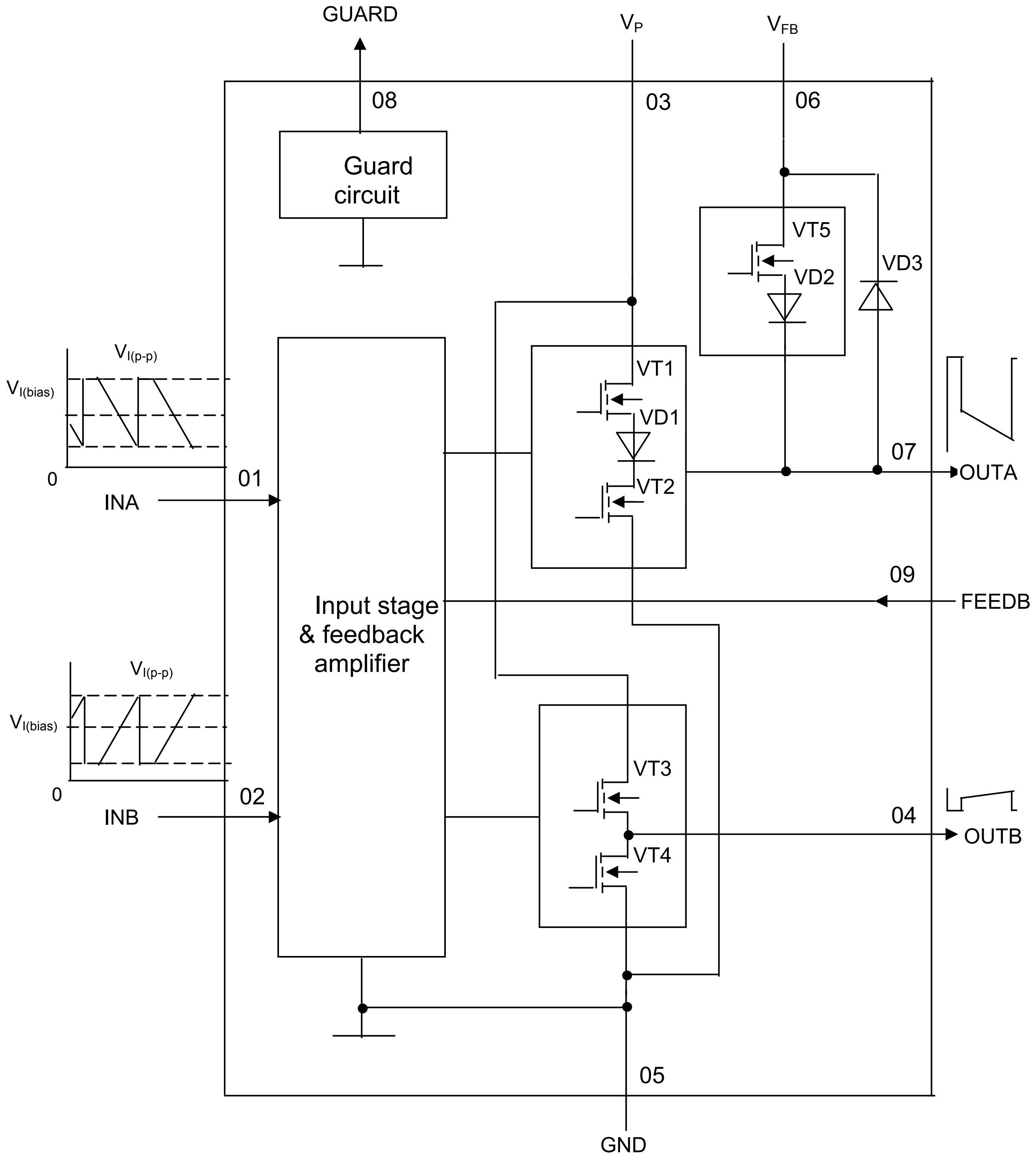


Fig 1 – Pin configuration

Table 1 – Pin description

Package pin number	Symbol	Pin description
01	INA	Input A
02	INB	Input B
03	V_P	Supply voltage
04	OUTB	Output B
05	GND	Ground
06	V_{FB}	Flyback supply voltage
07	OUTA	Output A
08	GUARD	Guard output
09	FEEDB	Feedback input



VD1 – VD3 – diodes;
VT1 – VT5 - transistors

Fig. 2 – Electric block diagram

Table 2 Absolute Maximum Ratings

Symbol	Parameters	Norm		Unit
		Min	Max	
V_P	Supply voltage	-	18,1	V
V_{FB} [1)]	Flyback supply voltage	-	68	V
$I_{O(p-p)}$	Output current	-	3,2	A
$I_{O(peak)}$	Flyback mode max (peak) output current at (t_{FB} < 1,5 ms; Flyback time)	-	±1,81	A
$V_{I(p-p)}$ [2)]	Input voltage	-	1501	mV
$V_{O(qrd)(max)}$	Max guard voltage (Max leakage current $I_{I(max)}$ = 10 μA)	-	18,1	V
I_{lu}	Latch current	-	200 [3)]	mA
		-200 [4)]	-	
T_{stg}	Storage temperature	-60	150	°C
T_J	Junction temperature	-	150	°C

1) To limit voltage on pin 07 up to 68 V, V_{FB} should be 66 V because of voltage drop on the internal diode between pins07 and 06 in the first part of flyback.
2) Allowable range of input voltages is ($V_{I(bias)}$ + V_{dif}) < 1600 mV.
3) Max voltage on pin not more 1,5V_P. Determined for $T_{j(max)}$.
4) Max voltage on pin not more minus 1,5V_P. Determined for $T_{j(max)}$

Table 3 – Recommended operation modes

Symbol	Parameters	Norm		Unit
		Min	Max	
V_P	Supply voltage	7,5	18	V
V_{FB}	Flyback supply voltage	$2V_P$	66	V
$I_{O(p-p)}$	Output current	-	3,2	A
$I_{O(peak)}$	Flyback mode max (peak) output current at ($t_{FB} < 1,5$ ms; Flyback time)	-	±1,8	A
$V_{I(p-p)}$ 1)	Input voltage	0	1500	mV
$V_{I(bias)}$ 1)	Input bias voltage	100	1600	mV
$V_{O(qrd)(max)}$	Max guard voltage (Max leakage current $I_{I(max)} = 10\ \mu A$)	-	18	V
P_{tot} 2)	Total power dissipation	-	-	W
T_J	Junction temperature	-	125	°C

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1) Allowable range of input voltages is ($V_{I(bias)} + V_{dif}$) < 1600 mV.

2) Absolute maximum power P_{tot},mW, dissipated by IC at the ambient temperature T_A, is calculated by formula:

$$P_{tot} = (125 - T_A) \bullet R_{th(j-a)} \quad , \qquad (1`)$$

where 125 – junction absolute maximum operating temperature, °C

$R_{th(j-a)}$ – thermal resistance "junction – ambient", °C /W. $R_{th(j-a)}$ is estimated as 65°C /W.

For IC with additional external heat sink thermal resistance junction-ambient $R_{th(j-a)}$, °C /W , is determined as :

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-a)} \quad , \qquad (2)$$

$R_{th(j-c)}$ - thermal resistance "junction – case", °C /W. $R_{th(j-c)}$ is estimated as 6°C /W.

$R_{th(c-a)}$ - resistance "case-ambient" (is determined by the design of heat sink and specified by IC consumer),°C /W

Table 4 – Electric parameters (V_P = 12 V, V_{FB} = 45 V, -25C ≤ T_A≤ 85°C unless otherwise specified)

Symbol	Parameter	Mode of measurement	Norm		Unit
			Min.	Max.	
$I_{P(q)(av)}$	Consumption current , (during scan)	V_P = 12 V; R_L = ∞; $V_{I(bias)}$ = 0,88 V; T_A = 25 °C	-	15	mA
		V_P = 7,5; 12; 18 V T_A = -25; 85 °C	-	25	
$I_{P(q)}$	Consumption current (no signal, no load)	V_P = 12 V; V_{FB} = 45 V; R_L = ∞;$V_{I(bias)}$ = 0,88 V; T_A = 25 °C	-	75	mA
		V_P = 7,5; 12; 18 V T_A = -25; 85 °C	-	100	
$I_{FB(q)(av)}$	Flyback consumption current (during scan)	V_P = 12 V; V_{FB} from 45 to 66 V; $V_{I(bias)}$ = 0,88 V; T_A = 25 °C	-	10	mA
		V_P = 7,5; 12; 18 V T_A = -25; 85 °C	-	20	
$I_{I(bias)}$	Input bias current	V_P = 12 V; V_{FB} = 45 V; T_A = 25 °C	-	-35	μA
		V_P = 7,5; 12; 18 V T_A = -25; 85 °C	-	-40	
LEc	Nonlinearity ratio of near by unit	V_P = 12 V; V_{FB} = 45 V; $I_{O(p-p)}$ = 2,7 A; T_A = 25 °C	-	2,0	%
		T_A = -25; 85 °C V_P = 12; 18 V	-	10,0	
		V_P = 7,5 V; V_{FB} =15 V; T_A = -25; 85 °C			
LE	Nonlinearity ratio	V_P = 12 V; V_{FB} = 45 V; $I_{O(p-p)}$ = 2,7 A; T_A = 25 °C	-	3,0	%
		T_A = -25; 85 °C; V_P = 12; 18 V	-	15,0	
		V_P = 7,5 V ;V_{FB} = 15 V			
$V_{loss(FB)}$	Voltage between pins 06 & 07	V_P = 12 V; V_{FB} = 45 V; $V_{I(bias)1}$ = 1,6 V $V_{I(bias)2}$ = 0,1 VI_O = -1,1 A T_A = 25 °C T_A = -25; 85 °C	-	8,5 9,0	V
		V_{IO} = -1,6 A T_A = 25 °C T_A = -25; 85 °C	-	9,0 9,5	

Table 4continued

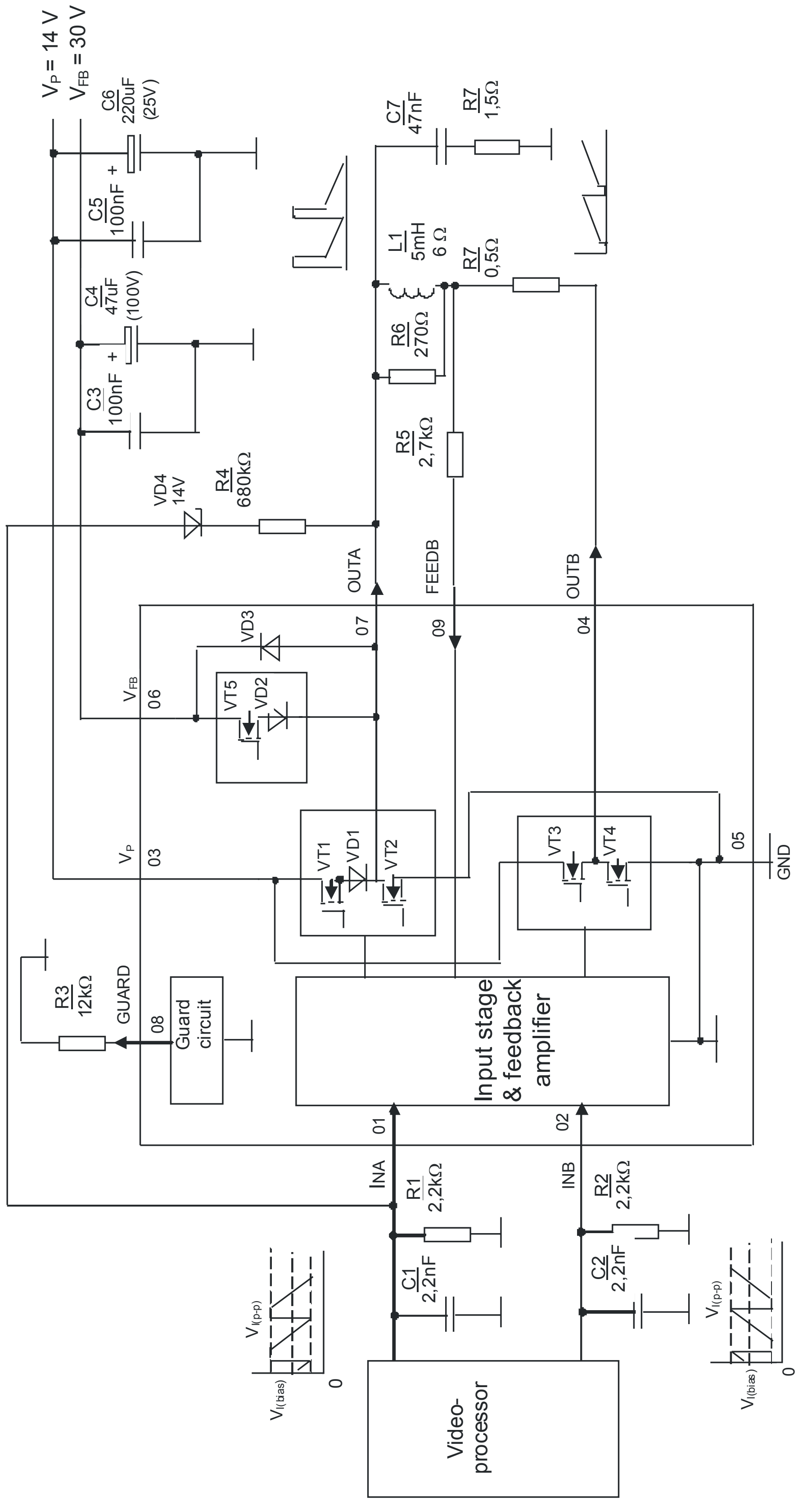
Symbol	Parameter	Mode of measurement	Norm		Unit
			Min.	Max.	
V_{offset}	Offset voltage on input of amplifier with back-coupling	V_P = 12 V; V_{FB} = 45 V; V_{dif} = 0 V; $V_{I(bias)}$ = 0,2 V; T_A = 25 °C T_A = -25; 85 °C	-15 -25	15 25	mV
		$V_{I(bias)}$ = 1,0 V; T_A = 25 °C T_A = -25; 85 °C	-20 -40	20 40	
$\Delta V_{offset(T)}$	Offset voltage variation with temperature,	V_P = 12 V; V_{FB} = 45 V; V_{dif} = 0 V; $V_{I(bias)}$ = 0,2; 1,0 V T_A = -25; 25; 85 °C	-	40	µV/K
$I_{O(grd)l}$	Guard circuit output current (guard circuit active)	V_P = 12 V; V_{FB} = 45 V; $V_{I(bias)1}$ = 1,6 V; $V_{I(bias)2}$ = 0,1 V; V_{08} = 4,5 V; T_A = 25 °C	-1,0	-2,5	mA
		V_P = 7,5; 12; 18 V; T_A = -25; 85 °C	0	-4,0	
$V_{O(grd)l}$	Guard circuit output voltage (pin 08) (guard circuit active)	V_P = 12 V; V_{FB} = 45 V; $V_{I(bias)1}$ = 1,6 V; $V_{I(bias)2}$ = 0,1 V; I_{O8} = 100 µA; T_A = 25 °C	5,0	7,0	mA
		V_P = 7,5; 12; 18 V; T_A = -25; 85 °C	3,0	9,0	
$I_{O(grd)h}$	Guard circuit output current (guard circuit disabled)	V_P = 12 V; V_{FB} = 45 V; V_{O8} = 0 V; T_A = 25 °C	-	-10	µA
		V_P = 7,5; 12; 18 V; T_A = -25; 85 °C	-	-80	
$V_{loss(1)}$	Voltage loss (drop) first scan part	V_P = 12 V; V_{FB} = 45 V; $V_{I(bias)1}$ = 1,6 V; $V_{I(bias)2}$ = 0,1 V; I_O = 1,1 A T_A = 25 °C T_A = -25; 85 °C	-	4,5 5,0	V
		I_O = 1,6 A T_A = 25 °C T_A = -25; 85 °C	-	6,6 7,5	
$V_{loss(2)}$	Voltage loss (drop) second scan part	V_P = 12 V; V_{FB} = 45 V; $V_{I(bias)1}$ = 1,6 V; $V_{I(bias)2}$ = 0,1 V; I_O = -1,1 A T_A = 25 °C T_A = -25; 85 °C	-	3,3 3,8	V
		I_O = -1,6 A T_A = 25 °C T_A = -25; 85 °C	-	4,8 5,2	

Table 4continued

Symbol	Parameter	Mode of measurement	Norm		Unit
			Min.	Max.	
PSRR	Power supply ripple rejection ratio,	$V_{P(rip)}$ = 0,5 V (rms); 50 Гц ≤ $f_{P(rip)}$ ≤ 1 kHz T_A = 25 °C	80	-	dB
$\Delta G_{V(T)}$	Voltage gain variation with temperature	V_P = 12 V; V_{FB} = 45 V; T_A = -25; 25; 85 °C	-	10^{-4}	K^{-1}
Note - A minus sign (“-“) before parameter value indicates current direction only (drain current). The value of current taken a magnitude of the current meter readings					

Table 5 – Typical electric parameters
(V_P = 12 V, V_{FB} = 45 V, T_A = 25 °C, f_P = 50 Hz, $V_{I(bias)}$ = 880 mV unless otherwise specified)

Symbol	Parameter	Mode of measurement	Typical value	Unit
V_O	DC output voltage	V_{dif} = 0 V	0,5 V_P	V
$G_{V(ol)}$	Open-loop voltage gain	-	60	dB
$f_{-3dB(h)}$	High -3 dB cut-off frequency	Without back-coupling	1,0	kHz
G_V	Voltage gain		1,0	-



f_{vert} = 50 Hz; t_{FB} = 640 μs; $I_{I(bias)}$ = 400 μA; $I_{I(p-p)}$ = 290 μA; $I_{O(p-p)}$ = 2,4 A

Fig 3 – Application diagramm

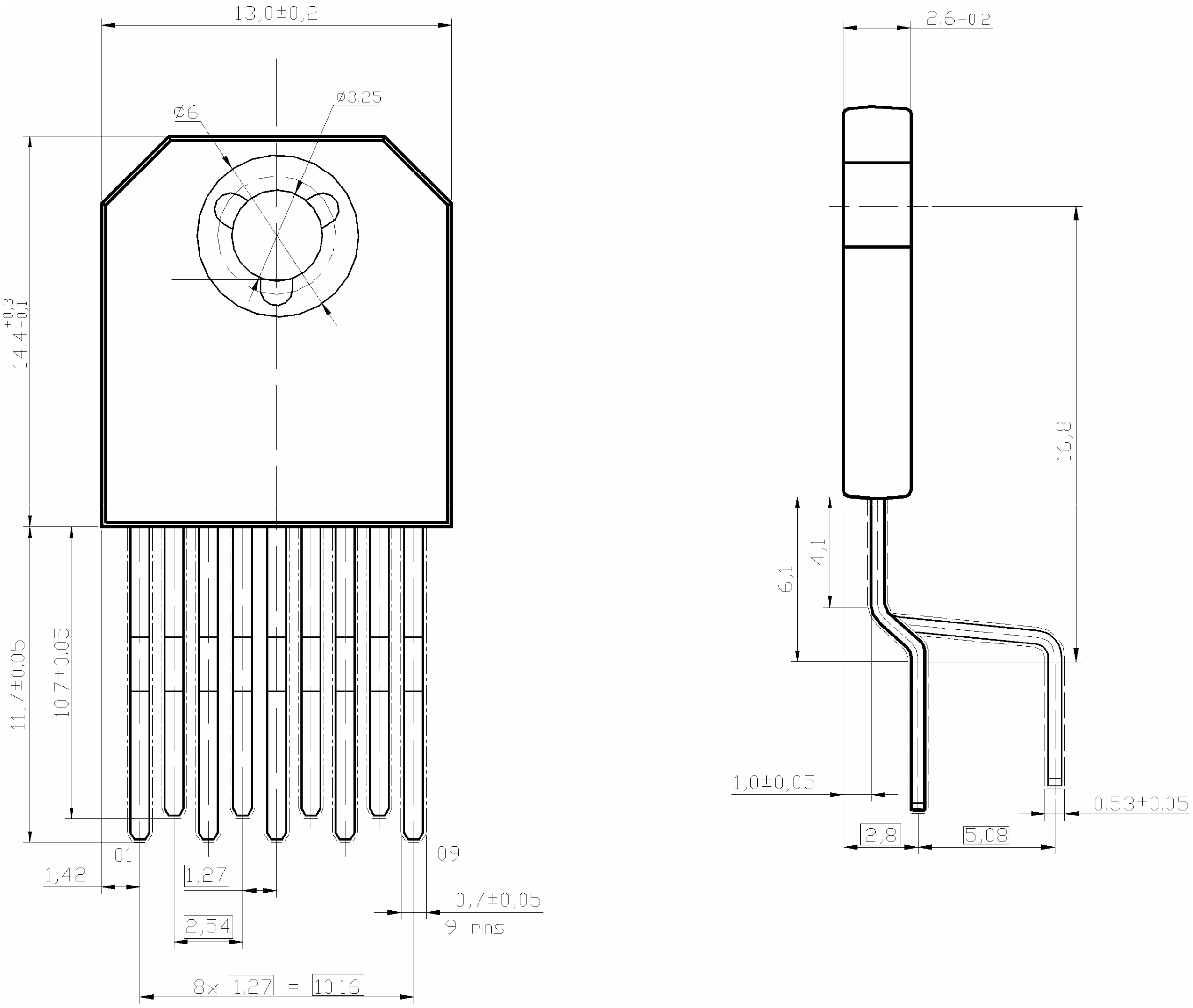
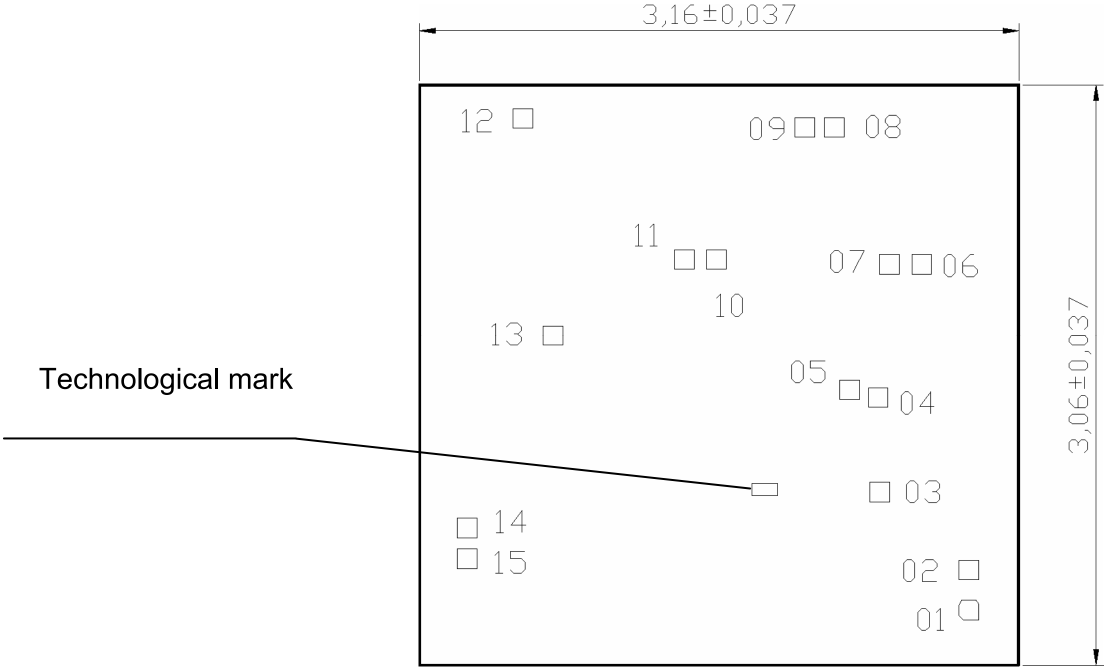


Fig. 4 –DBS 9P (1509.9-A) package outline

Technological mark



Contact pad coordinates are indicated in the table 6.

Technological mark on chip ILA8359 has coordinates, mm: left bottom corner x = 1.488 , y = 0.579.

Chip thickness is 0,35±0,02.

Fig. 5– Chip outline drawing

Table 6 Contact pad location table

Contact pad number	Coordinates (Left bottom corner), mm	
	X	У
01	2.845	0.240
02	2.845	0.450
03	2.374	0.860
04	2.366	1.359
05	2.216	1.399
06	2.596	2.062
07	2.426	2.062
08	2.134	2.784
09	1.980	2.784
10	1.513	2.088
11	1.343	2.088
12	0.492	2.831
13	0.650	1.686
14	0.199	0.670
15	0.199	0.510
Note - Coordinates and size of the contact pads 0,104 x 0,104 mm are given by the layer «Passivation»		

Table 7 Chip pad

Chip pad number	Symbol	Pin description
01	INA	Input A
02	INB	Input B
03, 04, 05	V_P	Supply voltage
06, 07	OUTB	Output B
08, 09	GND	Ground
12	V_{FB}	Flyback supply voltage
10, 11, 13	OUTA	Output A
14	GUARD	Guard output
15	FEEDB	Feedback input