

Dual Optically-Coupled Isolator

Optoelectronic Products

ILD-74

General Description

The ILD-74 comprises two distinct optoisolators with transistor output, in a single 8-pin dual in-line package. Each channel consists of a GaAs emitter optically coupled to a phototransistor.

High Current Transfer Ratio

1500 V Minimum Isolation Input-to-Output

$10^{11} \Omega$ Isolation Resistance

Low Coupling Capacitance—Typically 0.5 pF

I/O Compatible With Integrated Circuits

Two Packages Fit Into a Standard

16-Pin DIP Socket

Absolute Maximum Ratings

Maximum Temperature

Storage Temperature -55°C to $+150^{\circ}\text{C}$

Operating Temperature -55°C to $+100^{\circ}\text{C}$

Pin Temperature (Soldering, 7 s) 260°C

Total Package Power Dissipation at $T_A = 25^{\circ}\text{C}$ 400 mW

Derate Linearly from 25°C 5.33 mW/ $^{\circ}\text{C}$

Input Diode (Each Channel)

V_R Reverse Voltage 3.0 V

I_F Forward dc Current 100 mA

I_{pk} Peak Forward Current at 1 μs pulse, 300 pps 3.0 A

P_D Power Dissipation at $T_A = 25^{\circ}\text{C}$ 150 mW

Derate Linearly from 50°C 1.33 mW/ $^{\circ}\text{C}$

Output Transistor (Each Channel)

V_{CE} Collector-to-Emitter Voltage 20 V

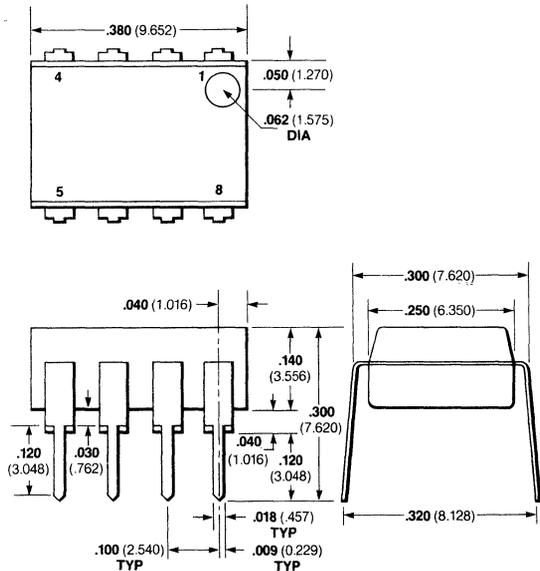
V_{EC} Emitter-to-Collector Voltage 6.0 V

P_D Power Dissipation at $T_A = 25^{\circ}\text{C}$ 150 mW

Derate Linearly from 25°C 2.0 mW/ $^{\circ}\text{C}$

I_C Collector Current 30 mA

Package Outline



Notes

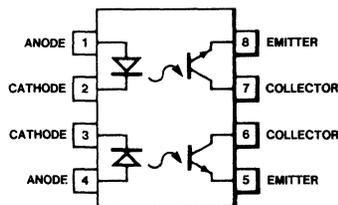
All dimensions in inches bold and millimeters (parentheses)

Tolerance unless specified = $\pm .015$ ($\pm .381$)

Package weight is 0.4 gram

Connection Diagram

DIP (Top View)



Pin

1	Anode	Channel # 1
2	Cathode	Channel # 1
3	Cathode	Channel # 2
4	Anode	Channel # 2
5	Emitter	Channel # 2
6	Collector	Channel # 2
7	Collector	Channel # 1
8	Emitter	Channel # 1

Typical Electrical Characteristics

ILD-74

Electrical Characteristics—Input Diode $T_A = 25^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
V_F	Forward Voltage		1.3		V	$I_F = 60\text{ mA}$
V_R	Reverse Voltage		3.0		V	$I_R = 100\ \mu\text{A}$
C_J	Junction Capacitance		100		pF	$V_F = 0\text{ V}$

Electrical Characteristics—Output Transistor $T_A = 25^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
V_{CE0}	Collector-to-Emitter Voltage	20			V	$I_C = 1.0\text{ mA}$, $I_F = 0$
I_{CE0}	Collector-to-Emitter Leakage Current		5.0	500	nA	$V_{CE} = 5.0\text{ V}$, $I_F = 0$
C_{CE}	Collector-to-Emitter Capacitance		2.0		pF	$V_{CE} = 0$

Electrical Characteristics—Coupled $T_A = 25^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions
V_{IO}	Input-to-Output Voltage	1500			V	
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage			0.5	V	$I_C = 2.0\text{ mA}$, $I_F = 16\text{ mA}$
$I_C/I_F(\text{CTR})$	Collector Current Transfer Ratio (Note 1)	12.5	35		%	$V_{CE} = 5.0\text{ V}$, $I_F = 16\text{ mA}$
R_{IO}	Input-to-Output Resistance		10^{14}		Ω	$V_{IO} = 500\text{ V}$
C_{IO}	Input-to-Output Capacitance		0.5		pF	$f = 1.0\text{ MHz}$
$t_{D(on)}$	Propagation Delay Times		6.0		μs	$V_{CE} = 5.0\text{ V}$, $I_F = 16\text{ mA}$
$t_{D(off)}$			25		μs	$R_L = 2.4\text{ k}\Omega$

Notes

- Collector current transfer ratio is defined as the ratio of the collector current to the forward bias input current.
- Rise time is defined as the time for the collector current to rise from 10% to 90% of peak value. Fall time is defined as the time required for the current to decrease from 90% to 10% of peak value.