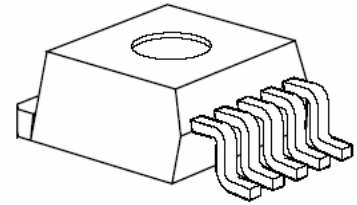


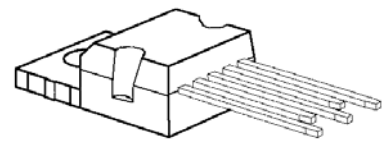
## IC of low power voltage regulator 5V/400mA with low drop voltage (FUNCTIONAL EQUIVALENT OF TLE4275 INFINEON)

ILE4275G, ILE4275S - are integrated circuits of voltage regulator 5V/400 mA with low-drop voltage. ICs realized in 5-pin plastic packages ILE4250G - P-TO263-5-1, ILE4250S – P-TO220-5-12.

ICs of voltage regulator 5V/400 mA are purposed to supply DC voltage 5V with 2% accuracy at a range of input voltages from 5,6 to 40 V , with drop voltage 0,5V at load current 300 mA. ICs are used in power supply units of electronic devices, including automotive electronics. Maximum input voltage is 45 V. The ICs are tolerant to over voltage of both polarities (positive & negative), provide internal current limitation and output voltage thermal shutdown. Reset function is available.



**Fig. 1 – View of IC in P-TO263-5-1 package**



**Fig. 2 – View of IC in P-TO220-5-12 package**

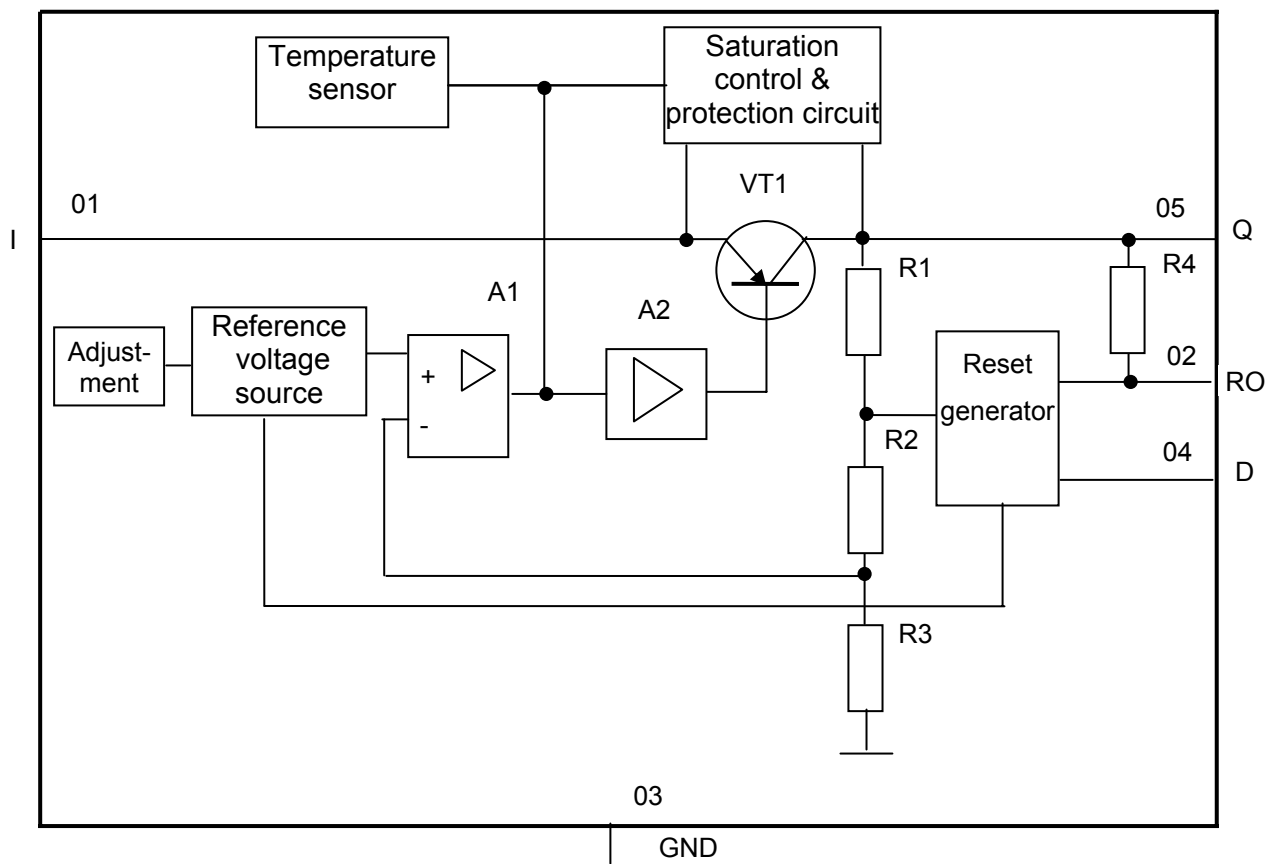
### Main features

- High accuracy of the output voltage  $5\text{ V} \pm 2\%$ ;
- Low-drop voltage ;
- Built-in overheating protection;
- Reverse polarity proof;
- Low consumption current;
- Input voltage up to 45 V;
- Suitable for use in automotive electronics;
- Wide junction temperature range  $-40 \dots +150^{\circ}\text{C}$ ;
- Reset function.

Permissible value of ESD potential 1000V

**Table 1 Pins description**

Chip pad number	Package pin number	Symbol	Function
01	01	I	Input
02	02	RO	Reset output
03	03	GND	Common pin (Ground)
04	04	D	Reset delay pin
05, 06	05	Q	Output
07 - 10	-	-	Not bonded (not used)



A1 – control amplifier;  
 A2 – buffer;  
 R1 – R4 –resistors;  
 VT1 - transistor

**Fig. 3 – Electric block diagram**

**Table 2 Absolute Maximum Ratings**

Symbol	Parameters	Norm		Unit
		min.	max.	
T <sub>J</sub>	Junction temperature	-40*	150	°C
T <sub>stg</sub>	Storage temperature	-50	150	°C
U <sub>I</sub>	Input voltage	-42	45	V
U <sub>D</sub>	Reset delay pin voltage	-0.3**	7**	V
I <sub>D</sub>	Reset delay pin current	-2	2	mA
U <sub>R</sub>	Reset pin voltage	-0,3**	25**	V
I <sub>RO</sub>	Reset pin current	-5	5	mA
U <sub>Q</sub>	Output voltage	-1,0**	16**	V

\* Ambient temperature is indicated.  
 \*\* Voltage is not applied to input I

**Table 3 – Recommended operation modes**

Symbol	Parameter	Norm		Unit
		Min.	Max.	
T <sub>J</sub>	Junction temperature	-40*	150	°C
U <sub>I</sub>	Input voltage	5,6	40	V
U <sub>Q</sub>	Output voltage	4,9	5,1	V

Note:

Maximum power P<sub>tot</sub>,W, dissipated by IC at ambient temperature T<sub>A</sub>, is calculated by formula:

$$P_{tot} = (150 - T_A) / R_{th\ j-a} , \quad (1)$$

150 – maximum permissible operating junction temperature, °C.

R<sub>th j-a</sub> - thermal resistance junction ambient (for IC without heat sink), °C /W,

for ILE4275G without heat sink R<sub>th ja</sub> is equal 80 °C /W

for ILE4275S without heat sink R<sub>th ja</sub> is equal 65 °C /W

for IC with heat sink R<sub>th ja</sub> is calculated by formula

$$R_{th\ j-a} = R_{th\ j-c} + R_{th\ c-a} , \quad (2)$$

R<sub>th j-c</sub> - thermal resistance junction case, °C /W. R<sub>th jc</sub> = 4 °C/W.

Thermal resistance case-ambient R<sub>th c-a</sub> is determined by heat sink design and is selected by IC customer.

Application circuit and heat sink and ambient temperature have to provide junction temperature not more T<sub>J</sub> ≤ 150 °C.

\* Ambient temperature is indicated.

**Table 4 – Electric parameters**

( $U_I = 13,5 \text{ V}$ ,  $U_{ADJ} > 2,0 \text{ V}$ ,  $-40 \text{ °C} \leq T_J \leq 150 \text{ °C}$  unless otherwise specified)

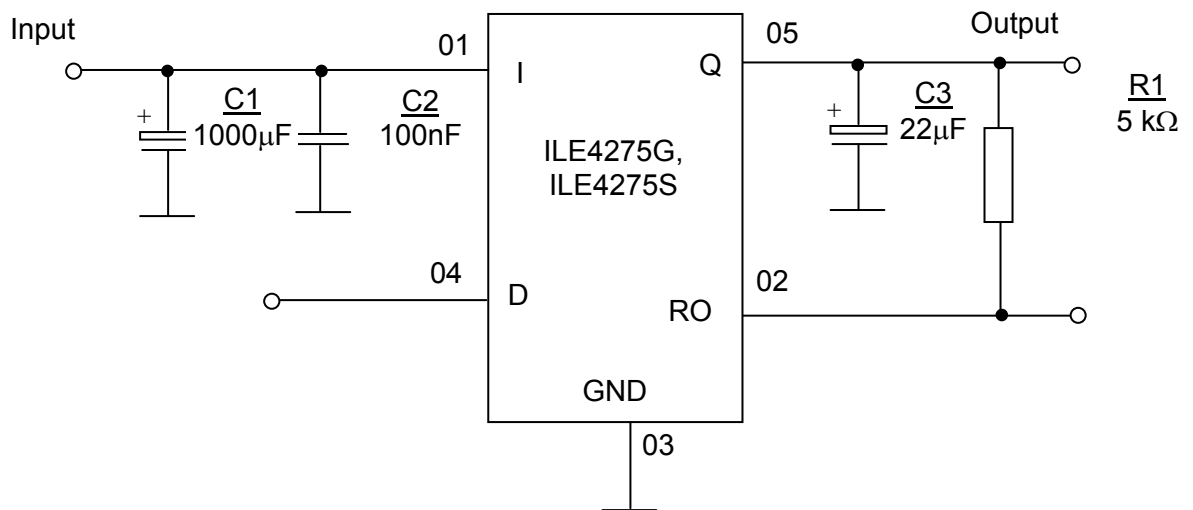
Symbol	Parameter	Mode of measurement	Norm		Unit
			Min.	Max.	
$I_q$	Consumption current $I_q = I_I - I_Q$	$I_Q = -1 \text{ mA}$ , $T_J = 25 \text{ °C}$	-	0,2	mA
		$I_Q = -1 \text{ mA}$ , $T_J < 85 \text{ °C}$	-	0,22	
		$I_Q = -250 \text{ mA}$	-	10	
		$I_Q = -400 \text{ mA}$	-	22	
$I_{Qmax}$	Maximum output current	-	450	-	mA
$U_{dr}$	Drop voltage	$I_Q = -300 \text{ mA}$ Note 2	-	0.5	V
$U_Q$	Output voltage	$6 \text{ V} \leq U_I \leq 28 \text{ V}$ $-5 \text{ mA} \leq I_Q \leq -400 \text{ mA}$	4.9	5.1	V
		$6 \text{ V} \leq U_I \leq 40 \text{ V}$ $-5 \text{ mA} \leq I_Q \leq -200 \text{ mA}$	4.9	5.1	
$\Delta U_{Q(U)}$	Supply (input) voltage regulation of output voltage	$8 \text{ V} \leq U_I \leq 32 \text{ V}$ $I_Q = -5 \text{ mA}$	-15	15	mV
$\Delta U_{Q(I)}$	Load current regulation of output voltage	$-5 \text{ mA} \leq I_Q \leq -400 \text{ mA}$	-	30	mV
Reset generator parameters					
$U_{RT}$	Reset generator switching threshold voltage	-	4.5	4.8	V
$I_{ROH}$	Reset output leakage current	$U_{ROH} = 5 \text{ V}$	-	10	$\mu\text{A}$
$U_{ROL}$	Reset output low level voltage	$R_{ext} \geq 5 \text{ k}\Omega$ , $U_Q > 1 \text{ V}$	-	0,4	V
$U_{DL}$	RO output switching to low threshold voltage	-	0,2	0,7	V
$U_{DU}$	RO output switching to high threshold voltage	-	1,5	2,2	V
$I_d$	Charge current	$U_D = 1 \text{ V}$	3,0	9,0	$\mu\text{A}$
$t_d$	Reset delay time	$C_D = 47 \text{ nF}$	10	22	ms
$t_{RR}$	Reset reaction time	$C_D = 47 \text{ nF}$	-	2	$\mu\text{s}$
<p>Notes</p> <p>1. Measurement of electric parameters is processed with connected input capacities <math>C_{I1} = 100 \mu\text{F}</math>, <math>C_{I2} = 100 \text{ nF}</math> and output capacity <math>C_Q = 22 \mu\text{F}</math>.</p> <p>2. Drop voltage <math>U_{dr} = U_I - U_Q</math> is measured, when the output voltage <math>U_Q</math> has dropped 100mV from the nominal value obtained at <math>U_I = 13.5 \text{ V}</math>.</p> <p>* Ambient temperature is indicated.</p>					

**Table 5 – Typical electric parameters**  
 ( $U_I = 13,5\text{ V}$ ,  $-40\text{ °C} \leq T_J \leq 150\text{ °C}$  unless otherwise specified)

Symbol	Parameter	Mode of measurement	Typical value	Unit
PSRR	Ripple rejection ratio	$f_r = 100\text{ Hz}$ , $I_Q = -100\text{ mA}$ $U_r = 0,5^{**}\text{ V (p - p)}$	60	dB
$dU_Q/dT$	Temperature factor of output voltage	-	0,5	mV/°C

\* Ambient temperature is indicated.

\*\* It is permitted to measure at  $U_{r(p-p)} = 3\text{ V}$ , but for that PSRR norm to be revised



**Fig 4 – Typical application diagram**

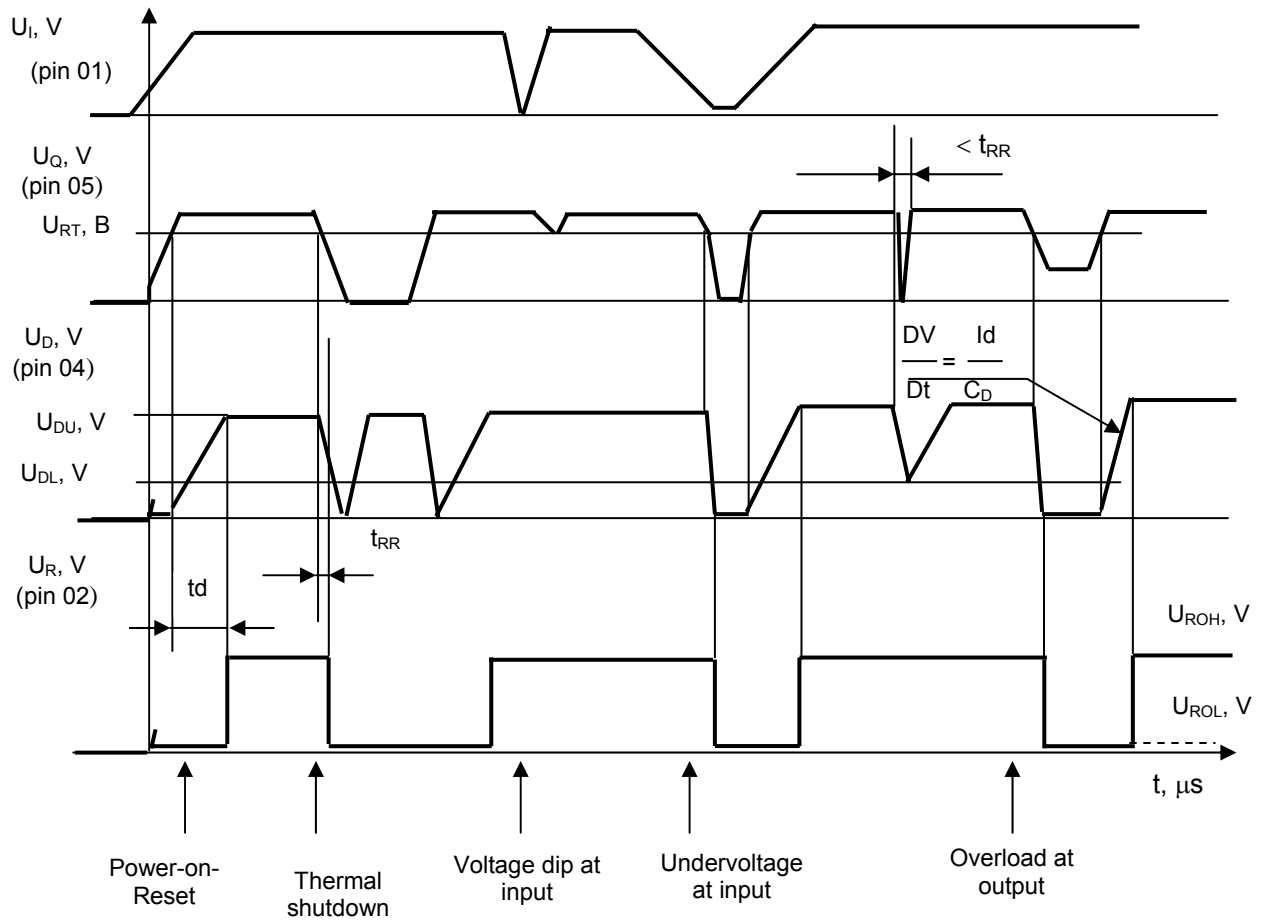


Fig 5 – Operation timing diagram

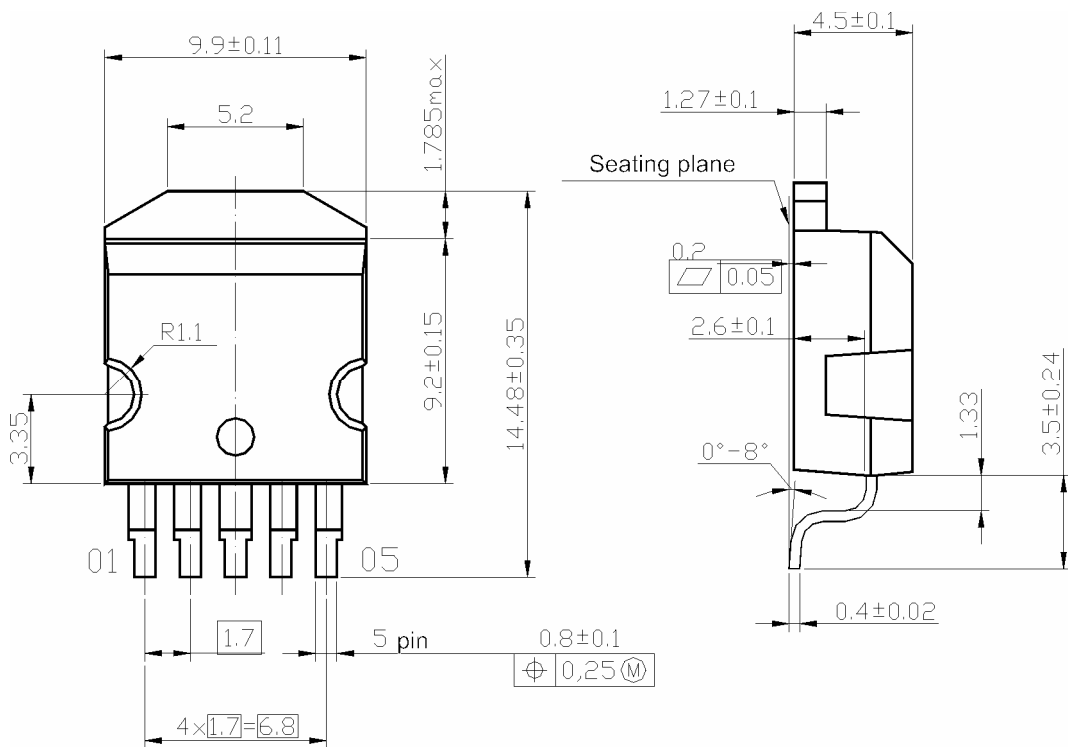


Fig 6 – P-TO263-5-1 package outline

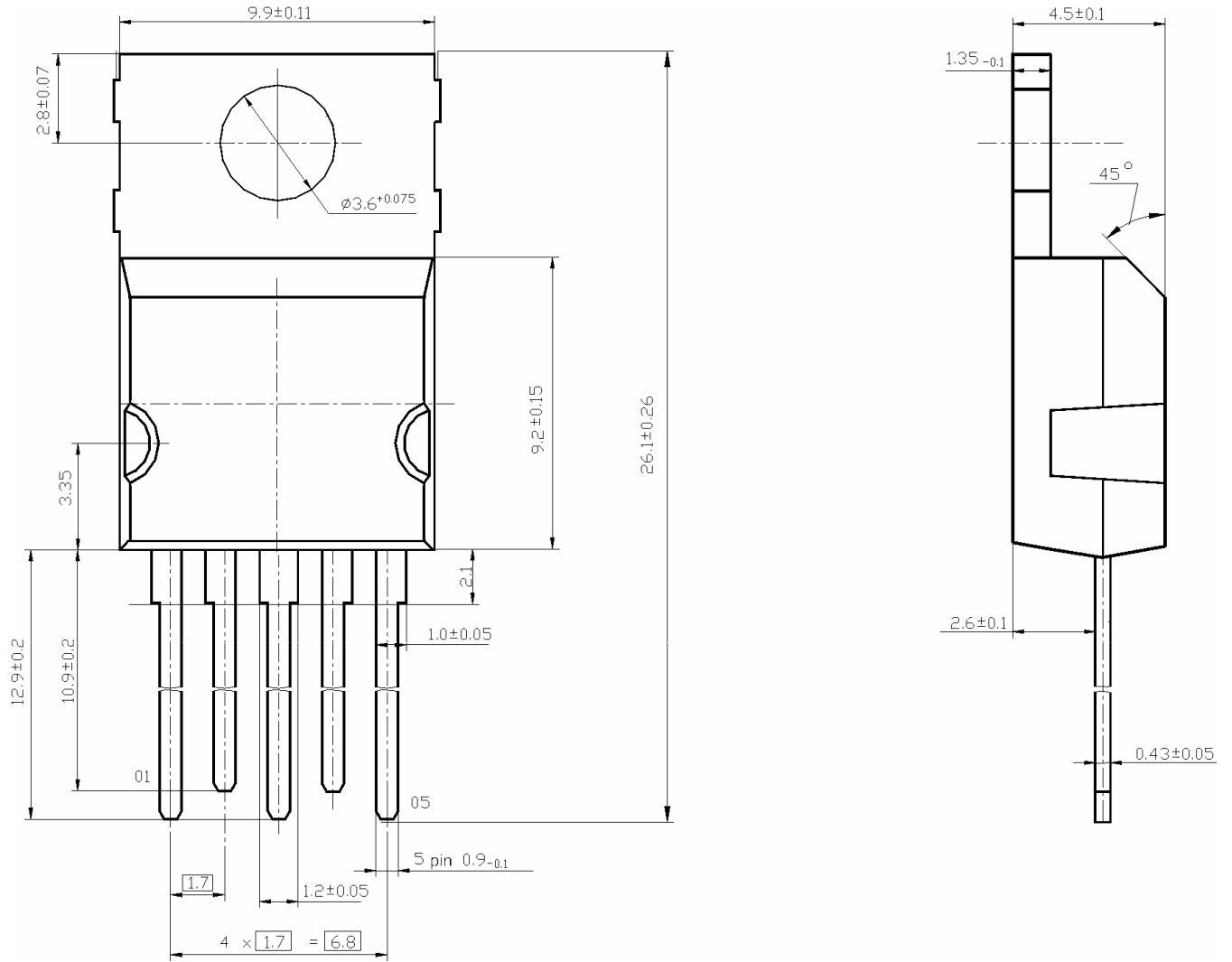
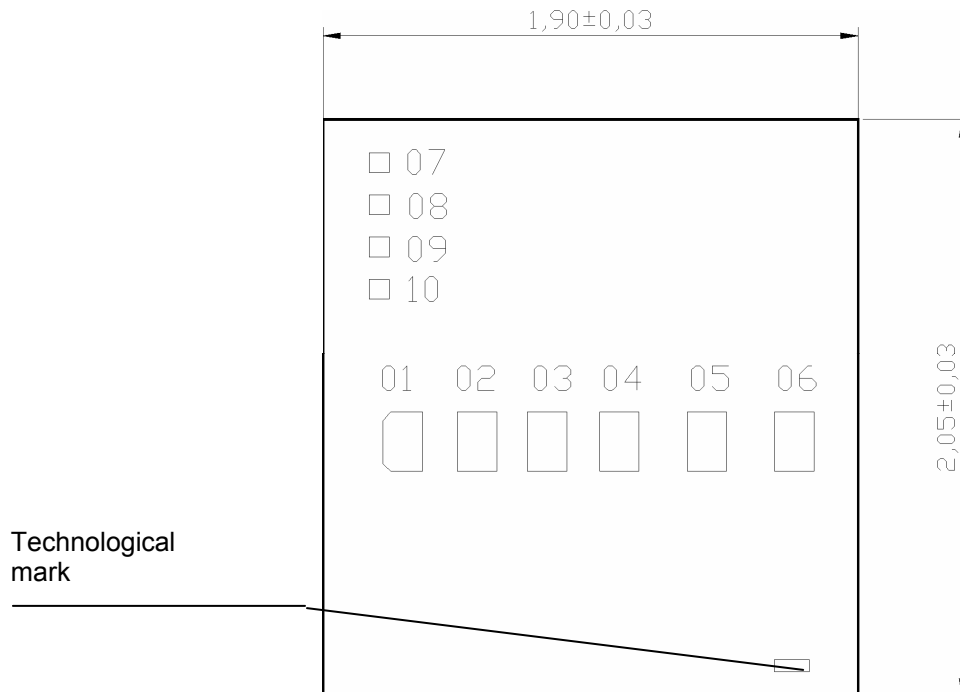


Fig. 7 – P-TO220-5-12 package outline





Contact pad coordinates are indicated in the table 6.

Technological mark on chip «4275» has coordinates, mm: left bottom corner  $x = 1,6755$  ,  $y = 0,1055$  .

Chip thickness is  $0,35 \pm 0,02$ .

**Fig. 8– Chip outline drawing**

**Table 6 Contact pad location table**

Contact pad number	Coordinates (Left bottom corner), mm	
	X	Y
01	0,213	0,797
02	0,477	0,797
03	0,7255	0,797
04	0,9815	0,797
05	1,2925	0,797
06	1,6035	0,797
07	0,164	1,862
08	0,164	1,712
09	0,164	1,562
10	0,164	1,412

**Notes**

- Coordinates and size of the contact pads are given by the layer «Passivation»
- Sizes of contact pads are  
01 – 06 -  $0,140 \times 0,140$  mm,  
07 - 10 -  $0,070 \times 0,070$  mm
- Bevel of two corners of the first contact pad ( $24 \pm 2$ )  $\mu$ m