

5350-pixel × 6-line CCD Linear Sensor (Color)

Description

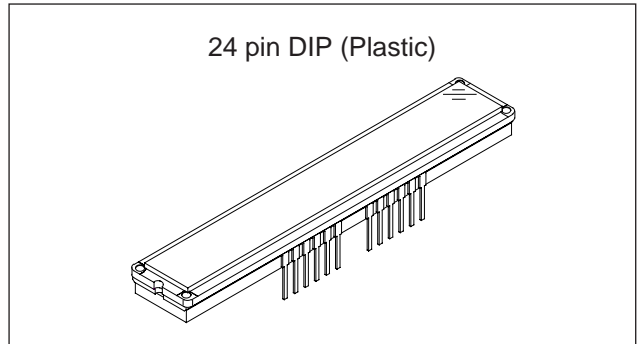
The ILX128MA is a reduction type CCD linear sensor developed for color image scanner, and has shutter function per each color. This sensor reads A3-size documents at a density of pseudo 800DPI, and reads A4-size at a density of pseudo 1200DPI.

Features

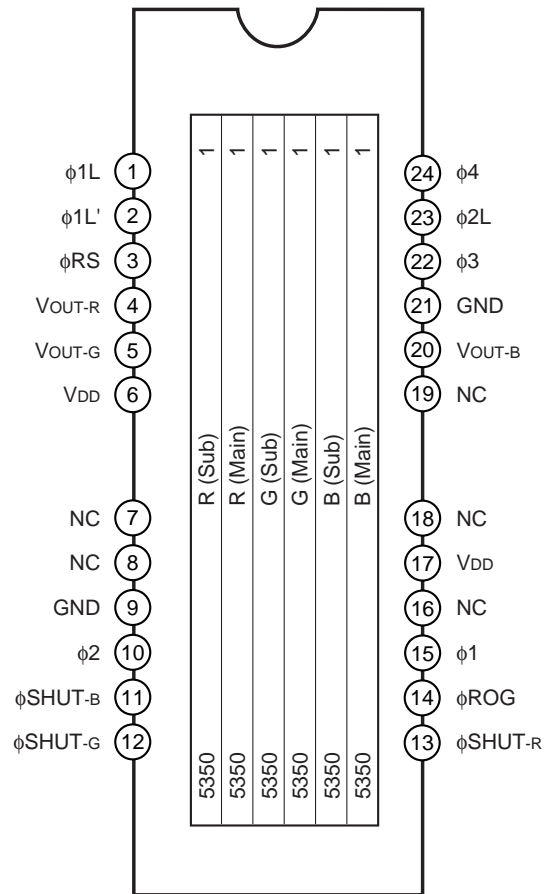
- Number of effective pixels: 32100 pixels (5350 pixels × 6)
- Pixel size: 6μm × 8μm (8μm pitch)
- Distance between line: 48μm (6 lines: Rsub – Rmain, Rmain – Gsub, Gsub – Gmain, Gmain – Bsub, Bsub – Bmain)
- Single-sided readout
- Shutter function
- Ultra-high sensitivity/Ultra-low lag
- Supply voltage: Single 12V power supply
- Input clock pulse: CMOS 5V drive
- Number of output: 3 (R, G, B)
- Package: 24-pin Plastic-DIP

Absolute Maximum Ratings

- Supply voltage V_{DD} 15 V
- Input clock voltage 7 V
- Operating temperature -10 to +55 °C
- Storage temperature -30 to +80 °C

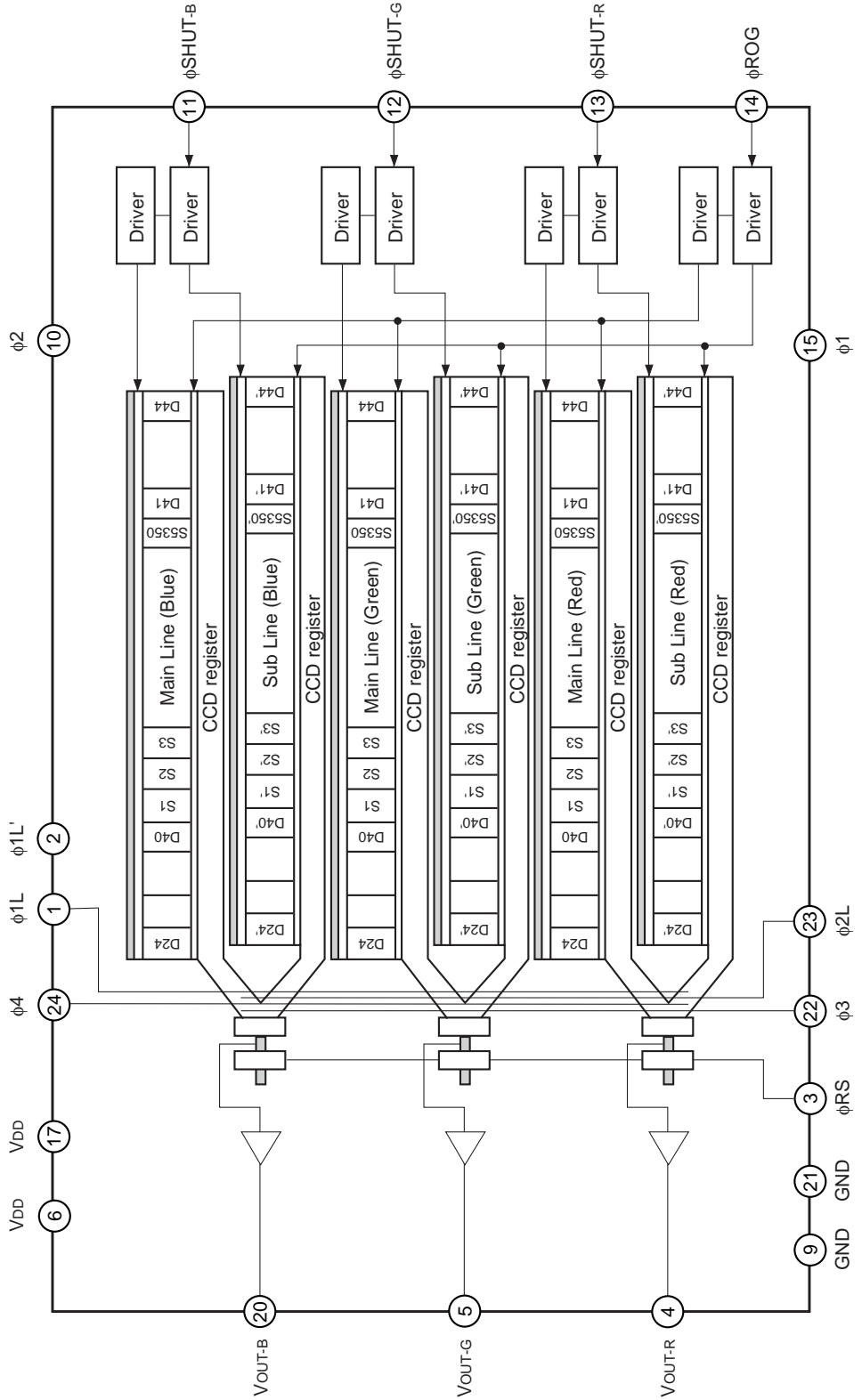


Pin Configuration (Top View)



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Block Diagram



Note) D24 and D24' are the start pixels for the optical black of Main Line and Sub Line. (These are not pixels immediately before multiplex.)

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	$\phi 1L$	Clock pulse input	13	$\phi SHUT-R$	Clock pulse input
2	$\phi 1L'$	Clock pulse input	14	ϕROG	Clock pulse input
3	ϕRS	Clock pulse input	15	$\phi 1$	Clock pulse input
4	V_{OUT-R}	Signal output (red)	16	NC	NC*
5	V_{OUT-G}	Signal output (green)	17	V_{DD}	12V power supply
6	V_{DD}	12V power supply	18	NC	NC
7	NC	NC	19	NC	NC
8	NC	NC	20	V_{OUT-B}	Signal output (blue)
9	GND	GND	21	GND	GND
10	$\phi 2$	Clock pulse input	22	$\phi 3$	Clock pulse input
11	$\phi SHUT-B$	Clock pulse input	23	$\phi 2L$	Clock pulse input
12	$\phi SHUT-G$	Clock pulse input	24	$\phi 4$	Clock pulse input

* Connecting to GND is recommended.

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12	12.6	V

Input Pin Capacity

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of $\phi 1$, $\phi 2$	$C_{\phi 1}$, $C_{\phi 2}$	—	1530	—	pF
Input capacity of $\phi 1L$, $\phi 1L'$, $\phi 2L$	$C_{\phi 1L}$, $C_{\phi 1L'}$, $C_{\phi 2L}$	—	20	—	pF
Input capacity of $\phi 3$, $\phi 4$	$C_{\phi 3}$, $C_{\phi 4}$	—	20	—	pF
Input capacity of ϕRS	$C_{\phi RS}$	—	20	—	pF
Input capacity of ϕROG	$C_{\phi ROG}$	—	10	—	pF
Input capacity of $\phi SHUT^{*1}$	$C_{\phi SHUT}$	—	10	—	pF

*1 $\phi SHUT$ represents $\phi SHUT-R$, $\phi SHUT-G$ and $\phi SHUT-B$.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
$\phi 1, \phi 2, \phi 1L, \phi 1L', \phi 2L$	$f\phi 1, f\phi 2, f\phi 1L, f\phi 1L', f\phi 2L$	—	1	3	MHz
$\phi 3, \phi 4$	$f\phi 3, f\phi 4$	—	2	6	MHz
ϕRS	$f\phi RS$	—	2	6	MHz

Input Clock Voltage Condition

Item		Min.	Typ.	Max.	Unit
$\phi 1L, \phi 1L', \phi 2L, \phi 3, \phi 4$	High level	4.75	5.0	5.25	V
	Low level	0	—	0.1	V
$\phi 1, \phi 2, \phi RS, \phi ROG, \phi SHUT$	High level	4.75	5.0	5.25	V
	Low level	0	—	0.5	V

Electrooptical Characteristics (Note 1)

(Ta = 25°C, VDD = 12V, f_{RS} = 2MHz, Input clock = 5Vp-p, Light source = 3200K, IR cut filter CM-500S (t = 1mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks	
Sensitivity	Red	R _R	1.33	1.9	2.47	V/(lx · s)	Note 2
	Green	R _G	3.01	4.3	5.59		
	Blue	R _B	1.82	2.6	3.38		
Sensitivity nonuniformity	PRNU	—	4	15	%	Note 3	
Adjacent pixel difference	PDF	—	4	15	%	Note 4	
Saturation output voltage	V _{SAT}	2	3	—	V	Note 5	
Overflow exposure	OE	2 × SE _{min}	—	—		Note 6	
Saturation exposure	Red	SE _R	0.8	1.6	—	lx · s	Note 7
	Green	SE _G	0.4	0.7	—		
	Blue	SE _B	0.6	1.2	—		
Dark voltage average	V _{DRK}	—	0.3	2.0	mV	Note 8	
Dark signal nonuniformity	DSNU	—	1.5	5.0	mV	Note 9	
Image lag	IL	—	0.02	—	%	Note 10	
Current consumption	I _{VDD}	—	32	50	mA	—	
Total transfer efficiency	TTE	92	98	—	%	—	
Output impedance	Z _o	—	250	—	Ω	—	
Offset level	V _{os}	4.7	6.2	7.7	V	Note 11	
Offset level difference	ΔV _{os}	—	40	200	mV	Note 12	
Dynamic range	DR	1000	10000	—	—	Note 13	

Note)

- For each color, the black level of Main Line is defined as the average value of D24, D25 to D39, and the black level of Sub Line is defined as the average value of D24', D25' to D39'. The following electrooptical characteristics signal processing is performed.
- For the sensitivity test light is applied with a uniform intensity of illumination.
- PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.
V_{OUT} = 500mV (Typ.)

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100 [\%]$$

Where the maximum output of the effective pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

- PDF = (ΔV_{MAX}/V_{AVE}) × 100 [%]

Here, V_{AVE} is defined as the average output, and ΔV_{MAX}, the maximum value of ΔV_i in the range of the following pixel.

Red, green, blue pixel arrangement PDF is when i = 1 to 5349. However, the definition of ΔV_i is as follows.

$$\Delta V_i = ABS \{V_{OUT} (i) - V_{OUT} (i + 1)\}$$

V_{OUT} (i) is signal output of an effective pixel (i pixel) and V_{OUT} (i + 1) is of the adjacent pixel (i + 1 pixel).

5. Specifies at the minimum value of the saturation output voltage.
6. SE_{min} is the exposure at the minimum value (2V) of the saturation output voltage.
7. Saturation exposure is defined as in the right figure. $SE = V_{SAT}/R$
8. For each color, Main Line is defined by the difference between the average value of D2 to D22 dummy signal during no incident light and of D24 to D40, S1 to S5350. Sub Line is defined by the difference between the average value of D2' to D22' dummy signal during no incident light and of D24' to D40', S1' to S5350'.

Optical signal integration time τ_{int} stands at 10ms.

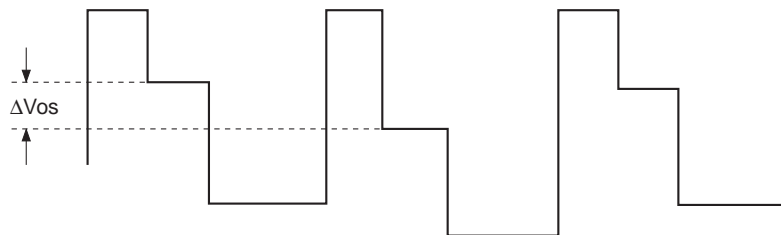
9. For each color, calculate the difference as follows; the maximum and minimum values of the dark output voltage of respective Main Line and Sub Line; the dark voltage average value of respective Main Line and Sub Line. Then, the highest value is defined as dark signal nonuniformity.

Optical signal integration time τ_{int} stands at 10ms.

10. $V_{OUT} = 500mV$ (Typ.)
11. V_{os} is defined as the output DC value when ϕ_{RS} is high.
12. For each color, the Main Line offset level of the optical black pixel is defined as $V_{os-main}$, the Sub Line offset level, V_{os-sub} . Then, the offset level difference is defined as indicated below.

$$\Delta V_{os} = |V_{os-main} - V_{os-sub}|$$

ϕ_{1L} and ϕ_{1L}' are set to the same clock input.

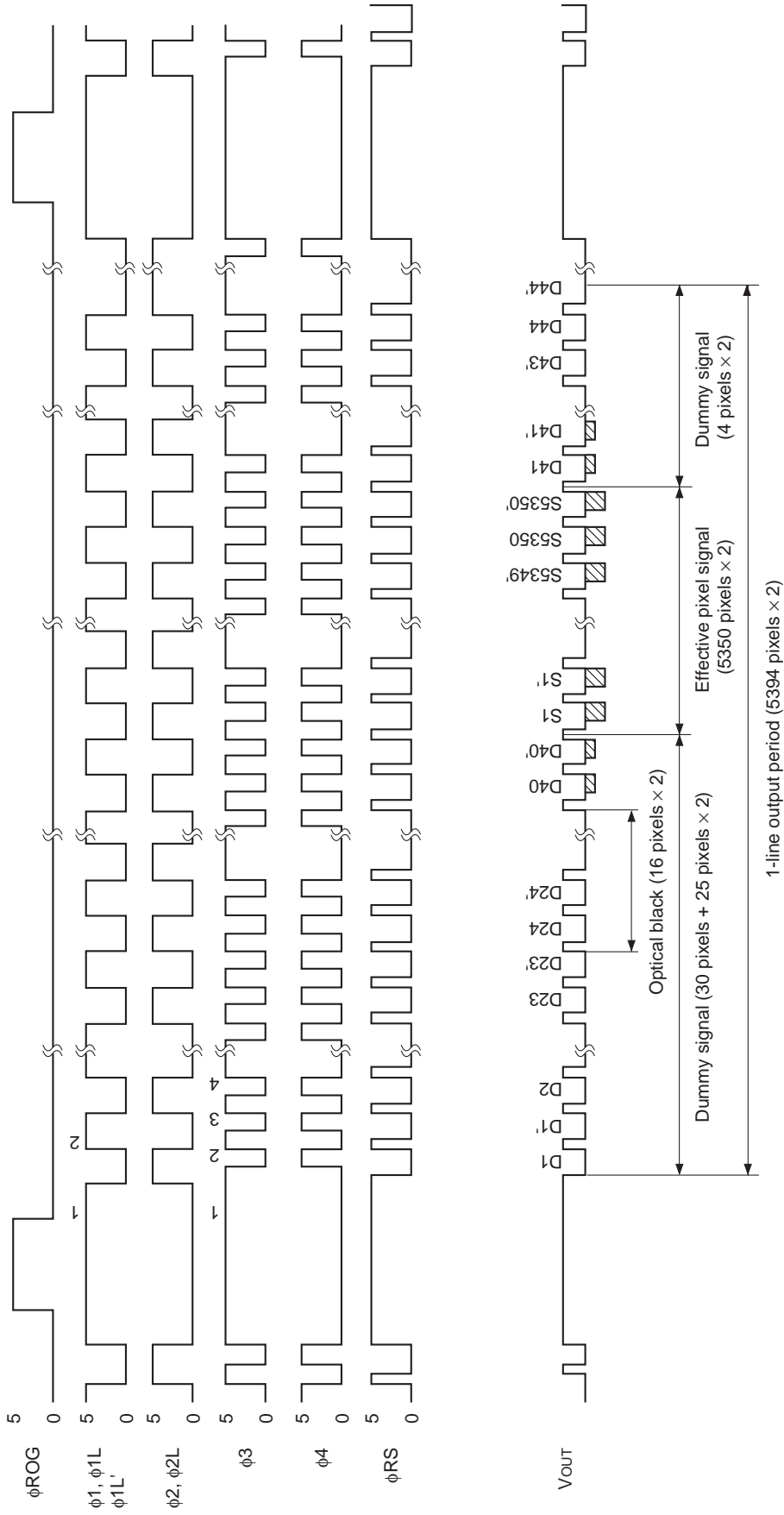


13. Dynamic range is defined as follows.

$$DR = V_{SAT}/V_{DRK}$$

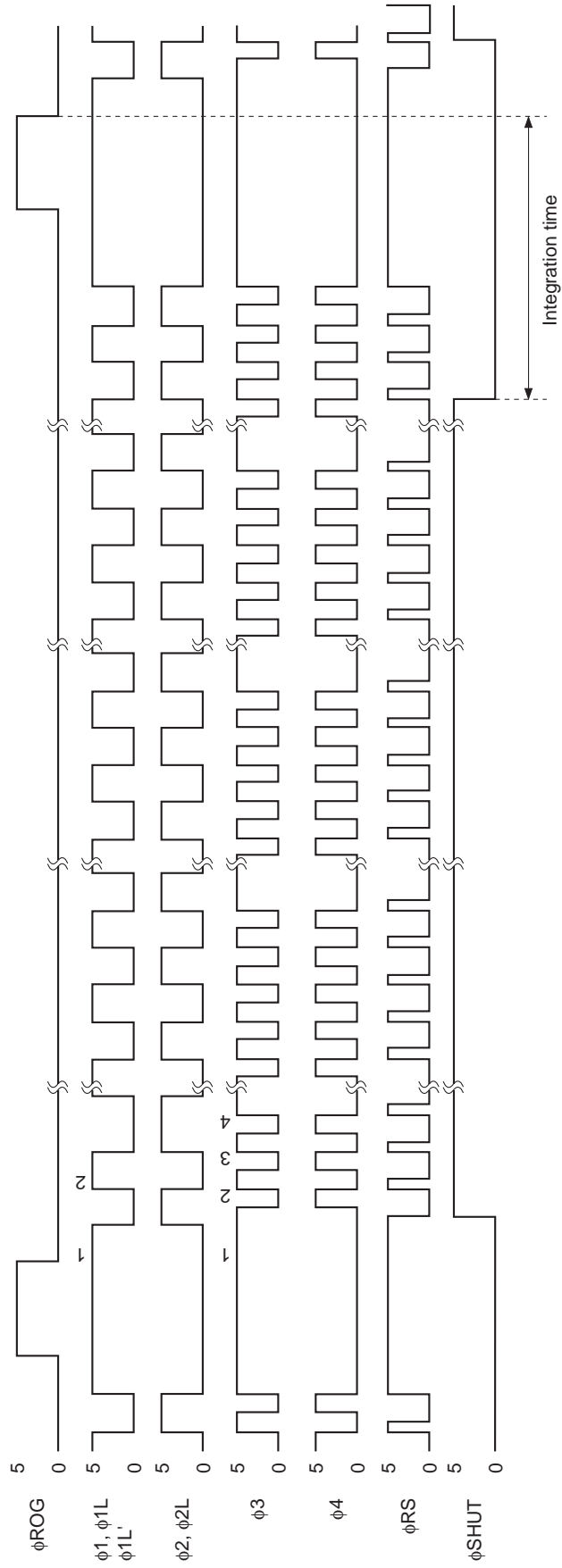
When the optical signal integration time is shorter, the dynamic range gets wider because the optical signal integration time is in proportion to the dark voltage.

Clock Timing Chart 1



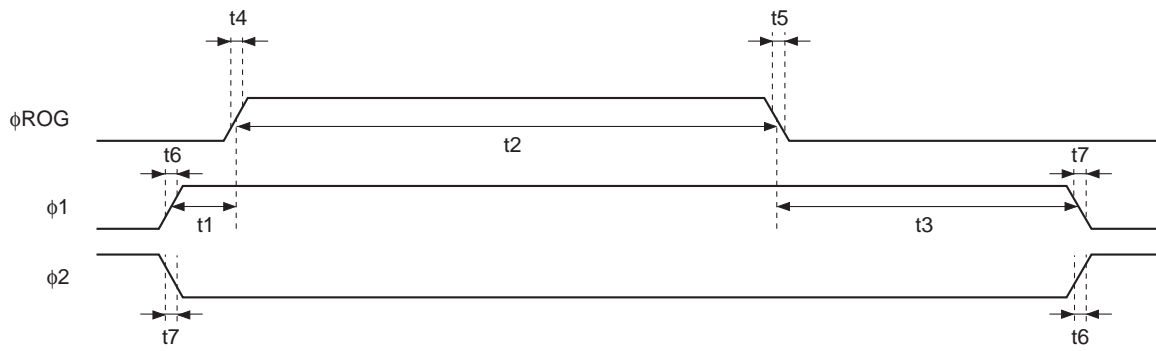
Note) The transfer pulse ϕ_1 , ϕ_2 , ϕ_{1L} , ϕ_{1L}' and ϕ_{2L} must have more than 5394 cycles. ϕ_3 and ϕ_4 must have more than 10788 cycles.

Clock Timing Chart 2 (shutter operation)

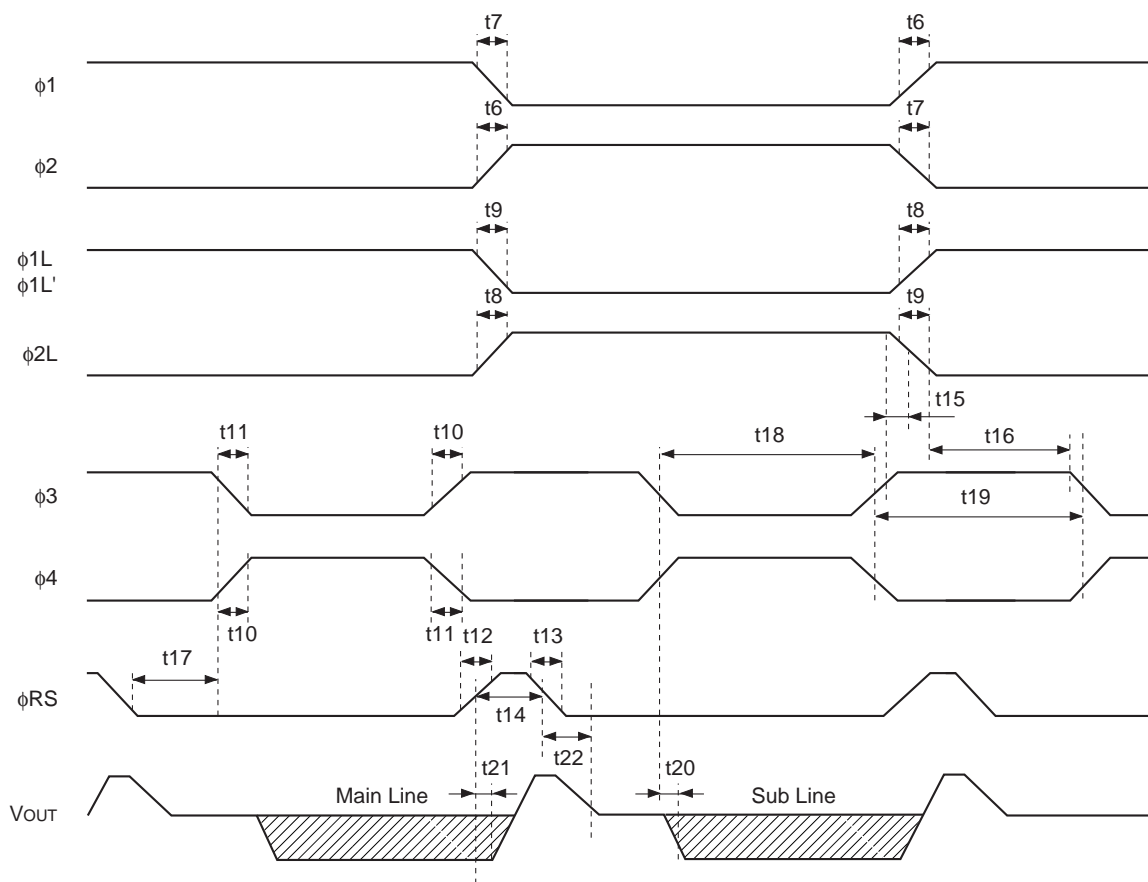


Note) Shutter pulse must not be high to low level or low to high level during effective pixel period.

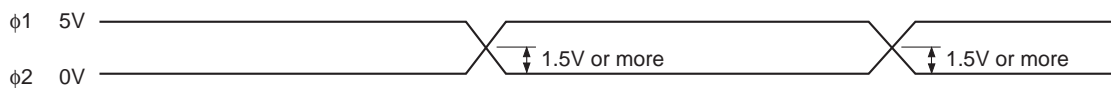
Clock Timing Chart 3



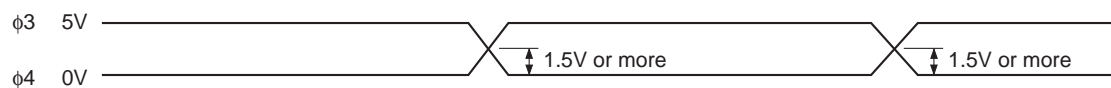
Clock Timing Chart 4



ϕ_1 and ϕ_2 Cross Point



ϕ_3 and ϕ_4 Cross Point



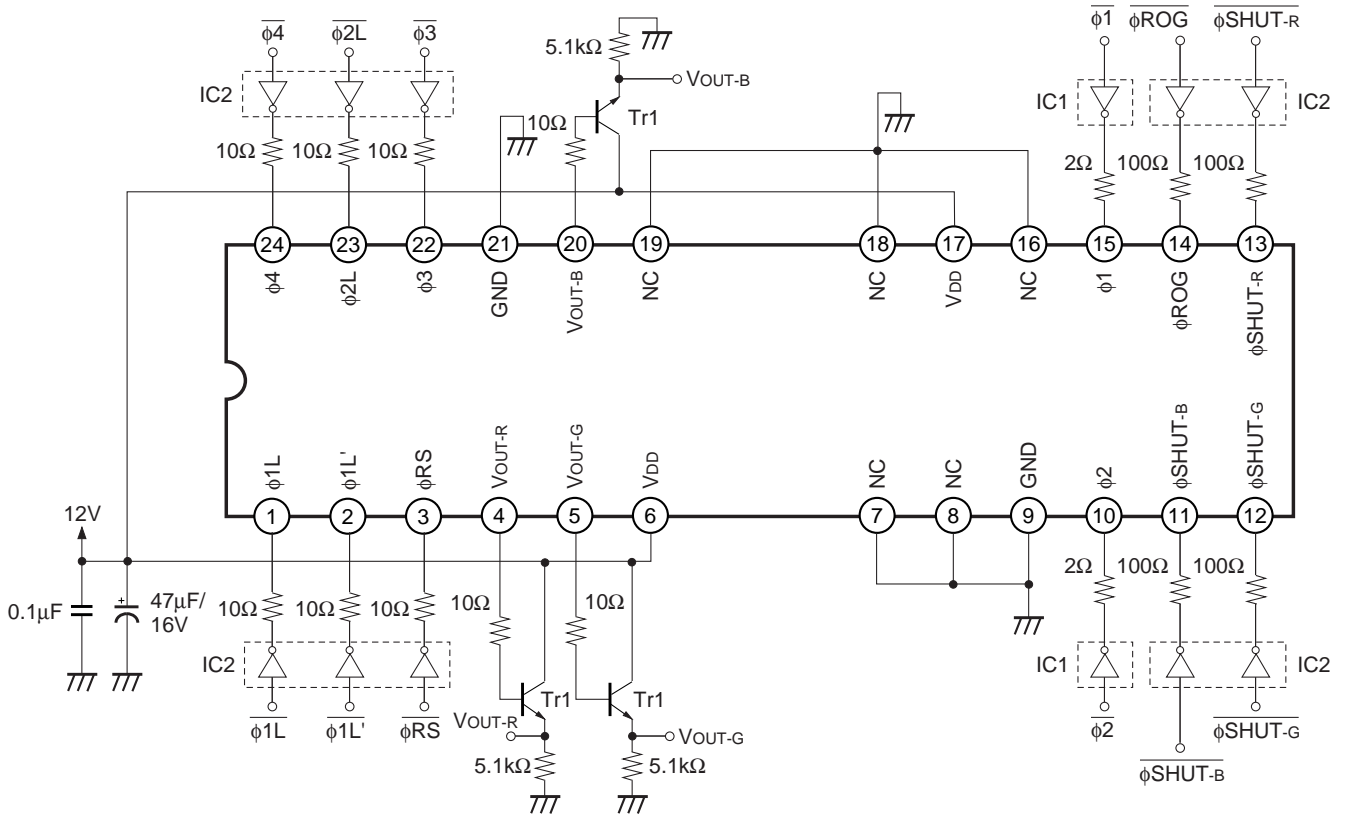
Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
ϕ ROG, ϕ 1 pulse timing	t1	50	100	—	ns
ϕ ROG pulse high level period	t2	1200	1500	—	ns
ϕ ROG, ϕ 1 pulse timing	t3	1200	1500	—	ns
ϕ ROG pulse rise time	t4	0	5	10	ns
ϕ ROG pulse fall time	t5	0	5	10	ns
ϕ 1 pulse rise/ ϕ 2 pulse fall time	t6	0	20	60	ns
ϕ 1 pulse fall/ ϕ 2 pulse rise time	t7	0	20	60	ns
ϕ 1L, ϕ 1L' pulse rise/ ϕ 2L pulse fall time	t8	0	10	30 ^{*1}	ns
ϕ 1L, ϕ 1L' pulse fall/ ϕ 2L pulse rise time	t9	0	10	30 ^{*1}	ns
ϕ 3 pulse rise/ ϕ 4 pulse fall time	t10	0	10	30 ^{*1}	ns
ϕ 3 pulse fall/ ϕ 4 pulse rise time	t11	0	10	30 ^{*1}	ns
ϕ RS pulse rise time	t12	0	10	30 ^{*1}	ns
ϕ RS pulse fall time	t13	0	10	30 ^{*1}	ns
ϕ RS pulse high level period	t14	20	250 ^{*1}	—	ns
ϕ 1L', ϕ 2L – ϕ 3, ϕ 4 pulse timing 1	t15	35	40	—	ns
ϕ 1L', ϕ 2L – ϕ 3, ϕ 4 pulse timing 2	t16	35	210 ^{*1}	—	ns
ϕ RS, ϕ 3 pulse timing	t17	50	125 ^{*1}	—	ns
ϕ 3, ϕ 4 pulse low level period	t18	35	250	—	ns
	t19	35	250	—	ns
Signal output delay time	t20	—	35	—	ns
	t21	—	8	—	ns
	t22	—	35	—	ns

The recommended duty of ϕ 1, ϕ 2, ϕ 1L, ϕ 2L, ϕ 3 and ϕ 4 = 50%.

*1 These timing is the recommended condition under $f_{\phi RS} = 2\text{MHz}$.

Application Circuit*1

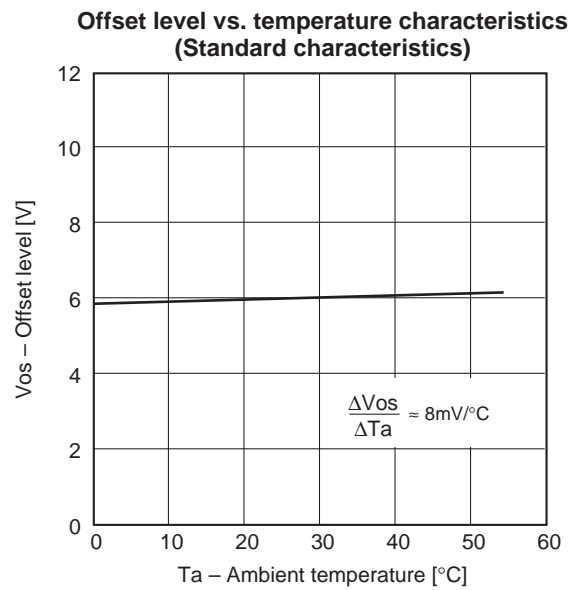
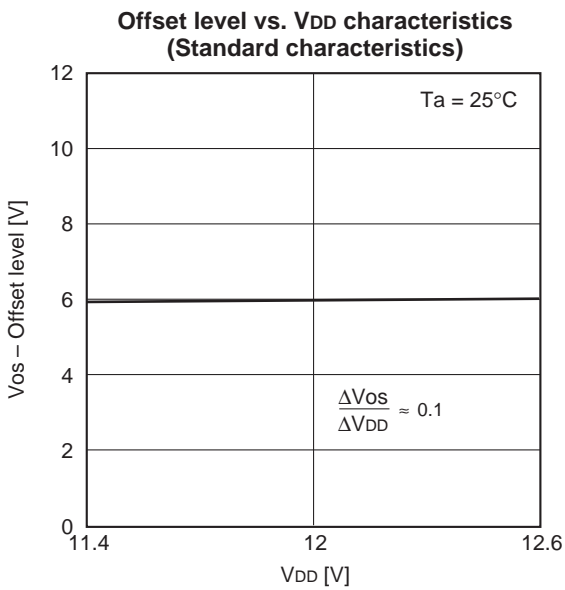
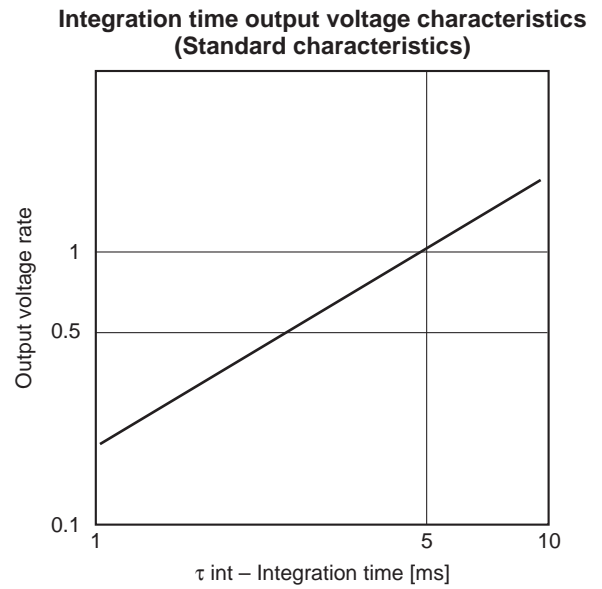
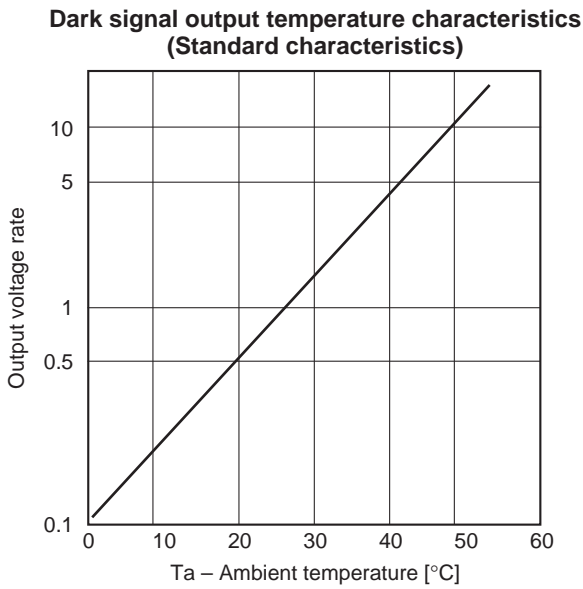
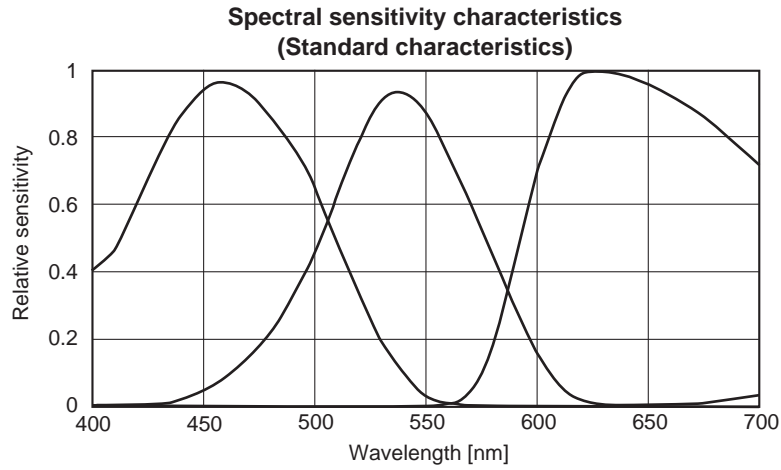


IC1: 74AC04
 IC2: 74HC04
 Tr1: 2SC2785

*1 Data rate $f_{\phi RS} = 2\text{MHz}$

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Example of Representative Characteristics ($V_{DD} = 12V$, $T_a = 25^\circ C$)



Notes on Handling

1. Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

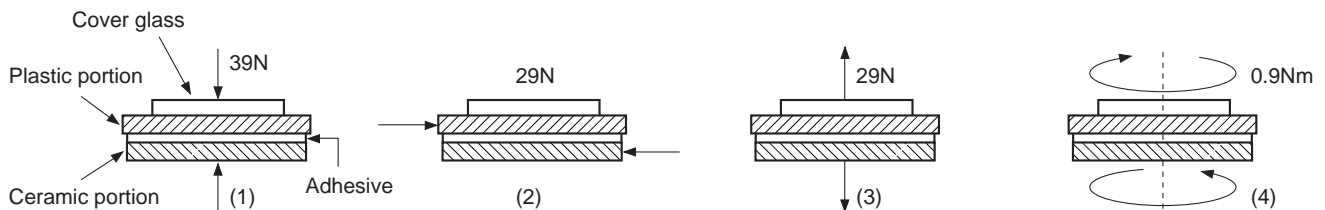
- Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
- When handling directly use an earth band.
- Install a conductive mat on the floor or working table to prevent the generation of static electricity.
- Ionized air is recommended for discharge when handling CCD image sensors.
- For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Notes on Handling CCD Packages

The following points should be observed when handling and installing plastic packages.

a) Remain within the following limits when applying static load to the package.

- Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
- Shearing strength: 29N/surface
- Tensile strength: 29N/surface
- Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion.

Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the package to crack or dust to be generated.

- Applying repetitive bending stress to the external leads.
- Applying heat to the external leads for an extended period of time with soldering iron.
- Rapid cooling or heating.
- Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
- Applying the metal a crash or a rub against the plastic portion.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

d) The notch of the plastic portion is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch or ceramic may overlap with the notch of the plastic portion.

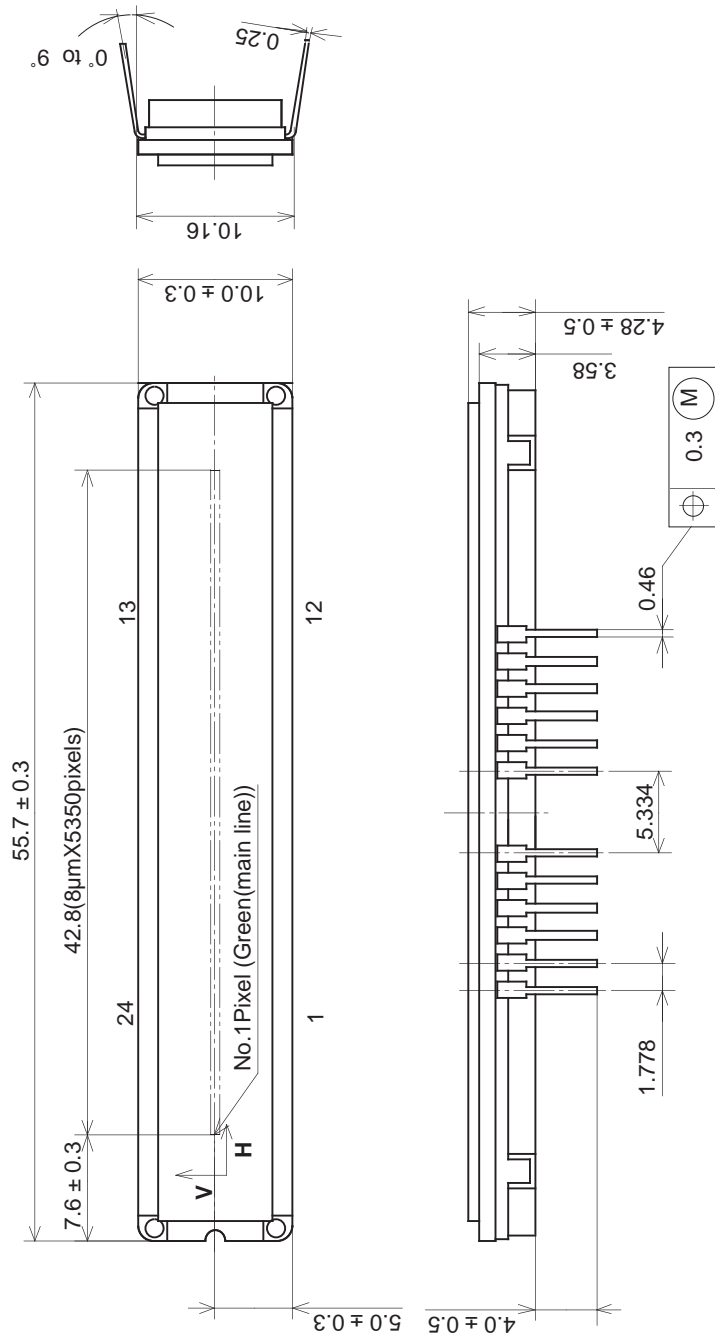
3. Soldering

- Make sure the package temperature does not exceed 80°C.
- Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
- To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, ground the controller. For the temperature control system, use a zero-cross type.

4. Dust and dirt protection
 - a) Operate in clean environments.
 - b) Do not either touch mirror surfaces by hand or have any object come in contact with mirror surfaces. Should dirt stick to a mirror surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
 - c) Clean with a cotton bud and ethyl alcohol if the mirror surfaces are grease stained. Be careful not to scratch the mirror surfaces.
 - d) Keep in a case to protect from dust and dirt. To prevent dew condensation on the mirror surfaces, preheat or precool when moving to a room with great temperature differences.
5. Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
6. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

24pin SDIP (400mil)



1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic-Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42ALLOY
PACKAGE MASS	5.43g
DRAWING NUMBER	LS-B27(E)