SONY

ILX137K

10700-pixel × 6-line CCD Linear Sensor (Color)

Description

The ILX137K is a reduction type CCD linear sensor developed for color image scanner. This sensor reads A4-size documents at a density of pseudo 2400DPI.

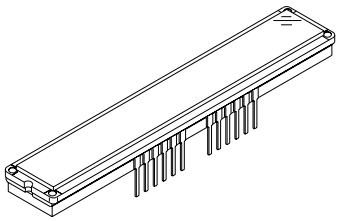
Features

- Number of effective pixels:
  64200 pixels (10700 pixels × 6)
- Pixel size: 2.4µm × 4µm (4µm pitch)
- Distance between line:
  2 lines between the same color (8µm)
  16 lines between different colors (64µm)
- On-chip microlens
  Cylindrical lens (width 6µm)
- Single-sided readout
- Supply voltage: Single 12V power supply
- Input clock pulse: CMOS 5V drive
- Number of output: 3 (R, G, B)
- Package: 24-pin Plastic-DIP

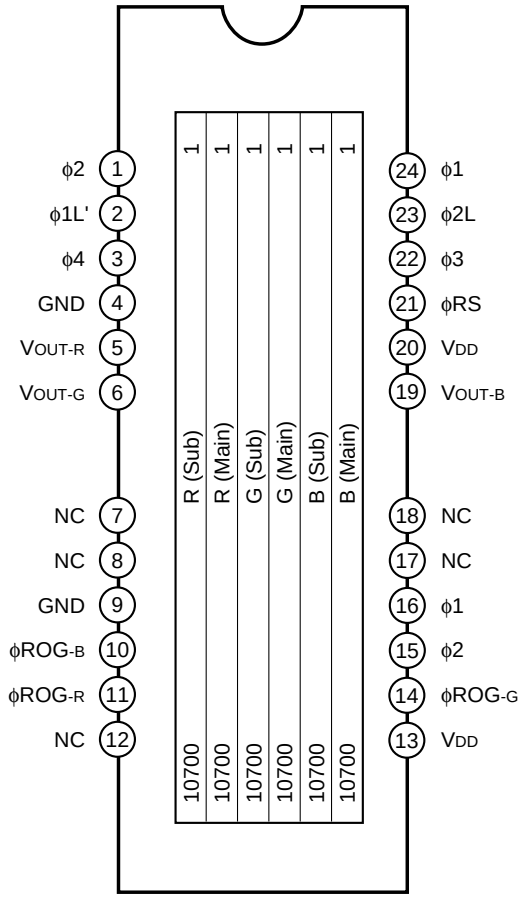
Absolute Maximum Ratings

• Supply voltage	V_{DD}	15	V
• Input clock voltage		7	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

24 pin DIP (Plastic)



Pin Configuration (Top View)



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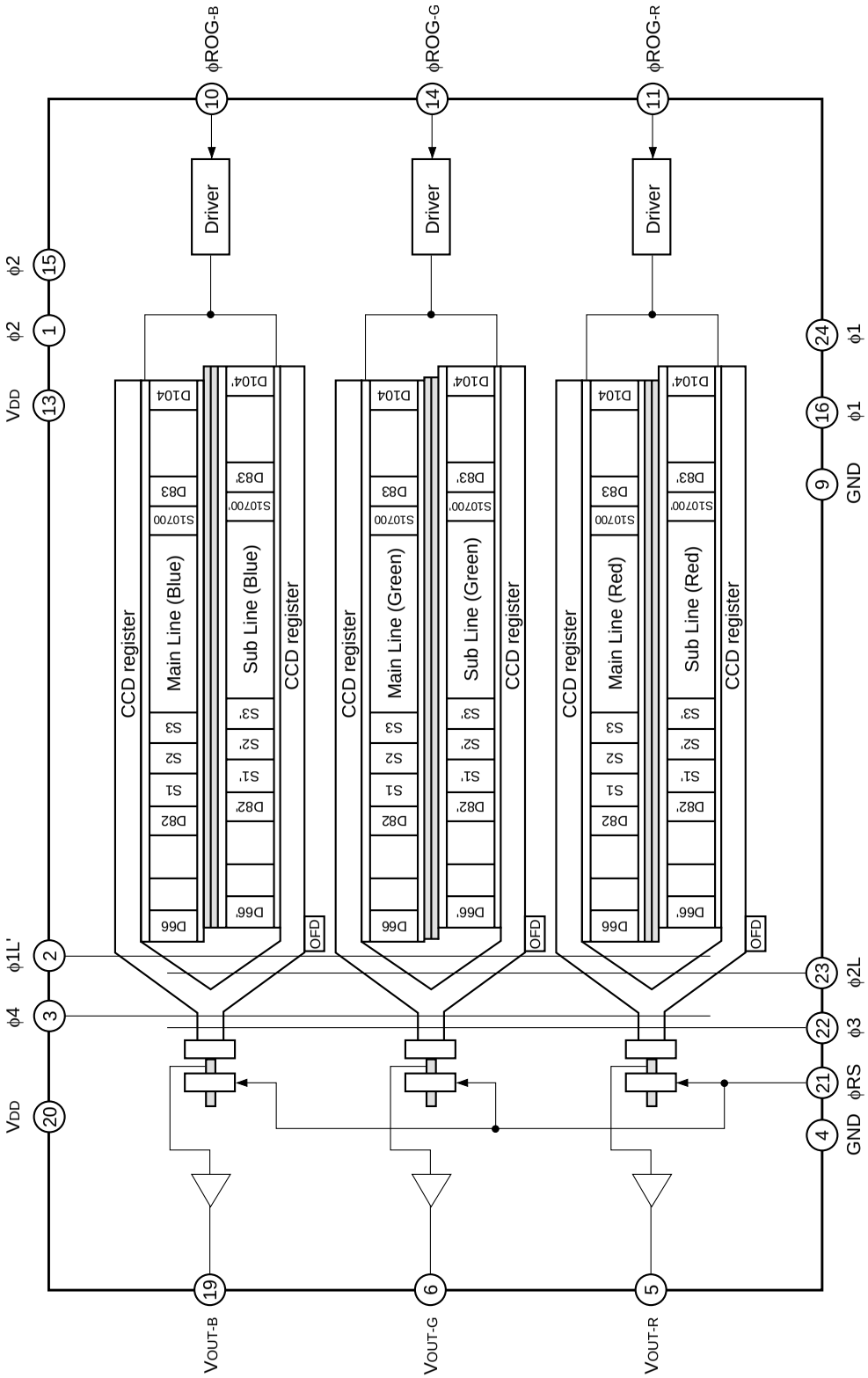
Block Diagram



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	φ2	Clock pulse input	13	V_{DD}	12V power supply
2	φ1L'	Clock pulse input	14	φROG-G	Clock pulse input
3	φ4	Clock pulse input	15	φ2	Clock pulse input
4	GND	GND	16	φ1	Clock pulse input
5	V_{OUT-R}	Signal output (red)	17	NC	NC
6	V_{OUT-G}	Signal output (green)	18	NC	NC
7	NC	NC	19	V_{OUT-B}	Signal output (blue)
8	NC	NC	20	V_{DD}	12V power supply
9	GND	GND	21	φRS	Clock pulse input
10	φROG-B	Clock pulse input	22	φ3	Clock pulse input
11	φROG-R	Clock pulse input	23	φ2L	Clock pulse input
12	NC	NC	24	φ1	Clock pulse input

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	11.4	12.0	12.6	V

Input Pin Capacitance

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacitance of φ1, φ2	Cφ1, Cφ2	—	2350	—	pF
Input capacitance of φ1L', φ2L	Cφ1L', Cφ2L	—	20	—	pF
Input capacitance of φ3, φ4	Cφ3, Cφ4	—	20	—	pF
Input capacitance of φRS	CφRS	—	10	—	pF
Input capacitance of φROG	CφROG	—	10	—	pF

* φROG represents φROG-R, φROG-G and φROG-B.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φ1L', φ2L	fφ1, fφ2, fφ1L', fφ2L	—	1	6	MHz
φ3, φ4	fφ3, fφ4	—	2	6	MHz
φRS	fφRS	—	2	6	MHz

Input Clock Voltage Conditions

Item		Min.	Typ.	Max.	Unit
φ1L', φ2L, φ3, φ4	High level	4.75	5.0	5.25	V
	Low level	0	—	0.1	V
φ1, φ2, φRS, φROG	High level	4.75	5.0	5.25	V
	Low level	0	—	0.5	V

Electro-optical Characteristics (Note 1)

Ta = 25°C, V_{DD} = 12V, $f\phi_{RS}$ = 2MHz, Input clock = 5Vp-p, Light source = 3200K,
IR cut filter CM-500S (t = 1.0mm)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	0.62	0.96	1.30	V/(lx · s)	Note 2
	Green	R_G	0.81	1.25	1.69		
	Blue	R_B	0.54	0.84	1.14		
Sensitivity nonuniformity		PRNU	—	4	18	%	Note 3
Adjacent pixel difference		PDF	—	4	16	%	Note 4
Saturation output voltage		V_{SAT}	1	1.5	—	V	Note 5
Overflow exposure		OE	3 × SEmin	—	—		Note 6
Saturation exposure	Red	SE_R	—	1.56	—	lx · s	Note 7
	Green	SE_G	—	1.20	—		
	Blue	SE_B	—	1.79	—		
Dark voltage average		V_{DRK}	—	0.1	2.0	mV	Note 8
Dark signal nonuniformity		DSNU	—	0.6	4.0	mV	Note 9
Image lag		IL	—	0.02	—	%	Note 10
Current consumption		I_{VDD}	—	18	35	mA	—
Total transfer efficiency		TTE	92	98	—	%	—
Output impedance		Z_O	—	300	—	Ω	—
Offset level		V_{OS}	5.0	6.5	8.0	V	Note 11
Offset level difference		ΔV_{OS}	—	—	100	mV	Note 12

Notes)

1. For each color, the black level of Main Line is defined as the average value of D66, D67 to D81, and the black level of Sub Line is defined as the average value of D66', D67' to D81'. The following electro-optical characteristics signal processing is performed.
2. For the sensitivity test light is applied with a uniform intensity of illumination.
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.

   V_{OUT} = 500mV (Typ.)

   $$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

   Where the maximum output of the effective pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.
4. PDF = $(\Delta V_{MAX}/V_{AVE}) \times 100$ [%]

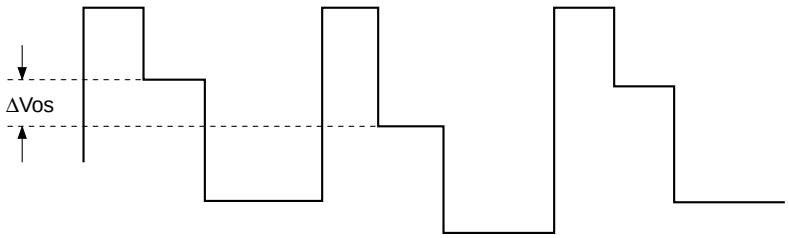
   Here, V_{AVE} is defined as the average output, and ΔV_{MAX}, the maximum value of ΔV_i in the range of the following pixel.

   Red, green, blue pixel arrangement PDF is when i = 1 to 10699. However, the definition of ΔV_i is as follows.

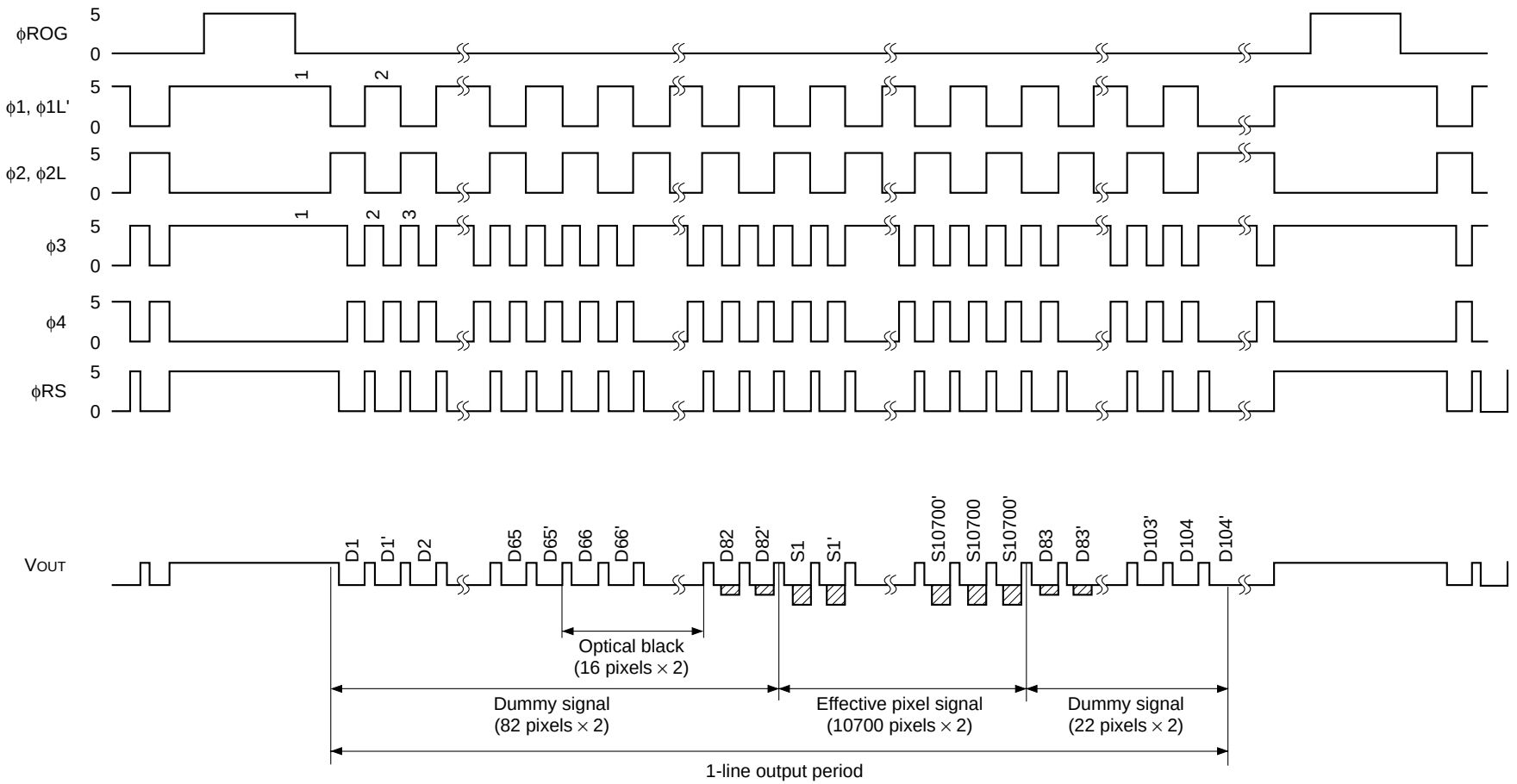
   ΔV_i = ABS {V_{OUT} (i) – V_{OUT} (i + 1)}

   V_{OUT} (i) is signal output of an effective pixel (i pixel) and V_{OUT} (i + 1) is of the adjacent pixel (i + 1 pixel).

5. Specifies at the minimum value of the saturation output voltage.
6. SEmin is the exposure at the minimum value (1V) of the saturation output voltage.
7. Saturation exposure is defined as in the following figure for each color.
   $SE = V_{SAT}/R$
8. For each color, Main Line is defined by the difference between the average value of D2 to D64 dummy signal during no incident light and of D66 to D82, S1 to S700. Sub Line is defined by the difference between the average value of D2' to D64' dummy signal during no incident light and of D66' to D82', S1' to S10700'. Optical signal integration time τ int stands at 20ms.
9. For each color, calculate the difference as follows; the maximum and minimum values of the dark output voltage of respective Main Line and Sub Line; the dark voltage average value of respective Main Line and Sub Line. Then, the highest value is defined as dark signal nonuniformity. Optical signal integration time τ int stands at 20ms.
10. V_{OUT} = 500mV (Typ.)
11. Vos is defined as the output DC value when ϕRS is high.
12. For each color, the Main Line offset level of the optical black pixel is defined as Vos-main, the Sub Line offset level, Vos-sub. Then, the offset level difference is defined as indicated below.
    $\Delta Vos = |$ Vos-main – Vos-sub $|$

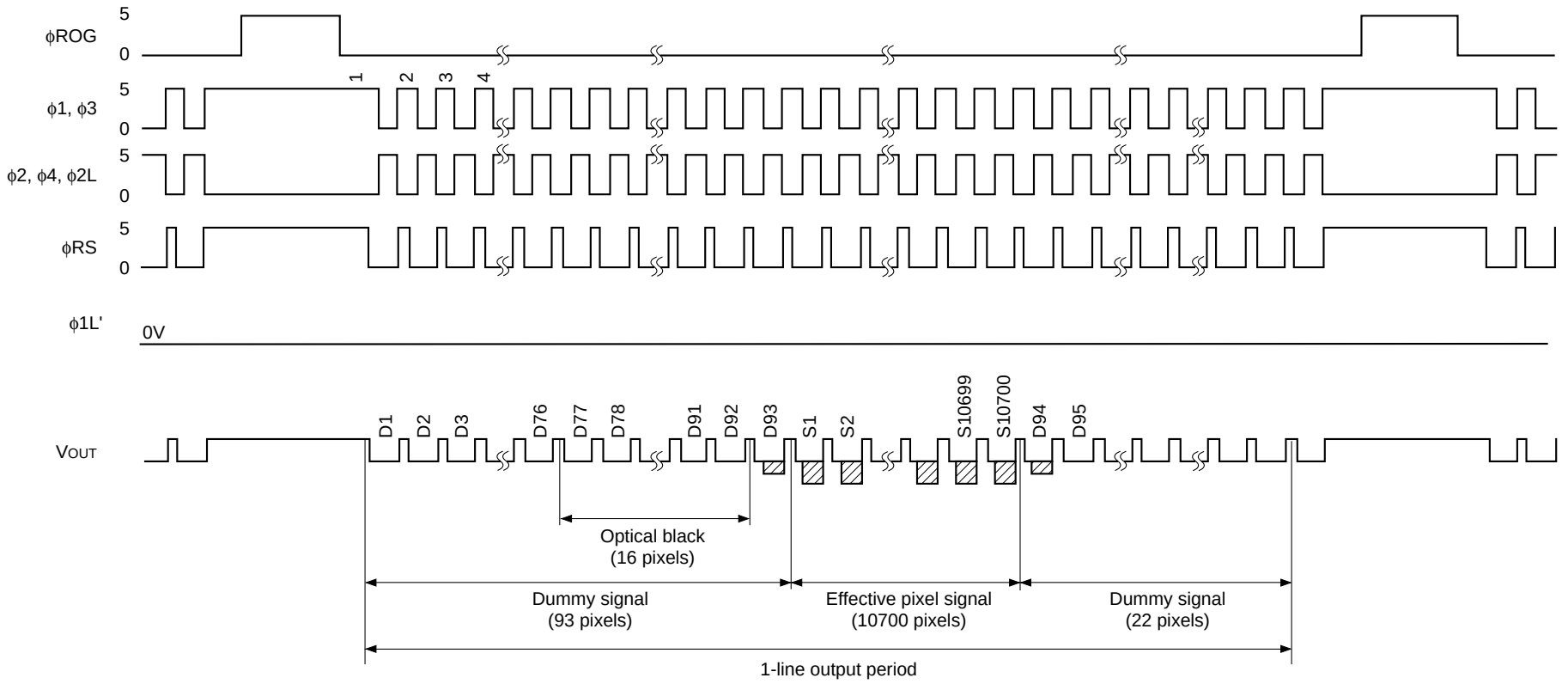


Clock Timing Chart 1 (Using both Main Line and Sub Line)



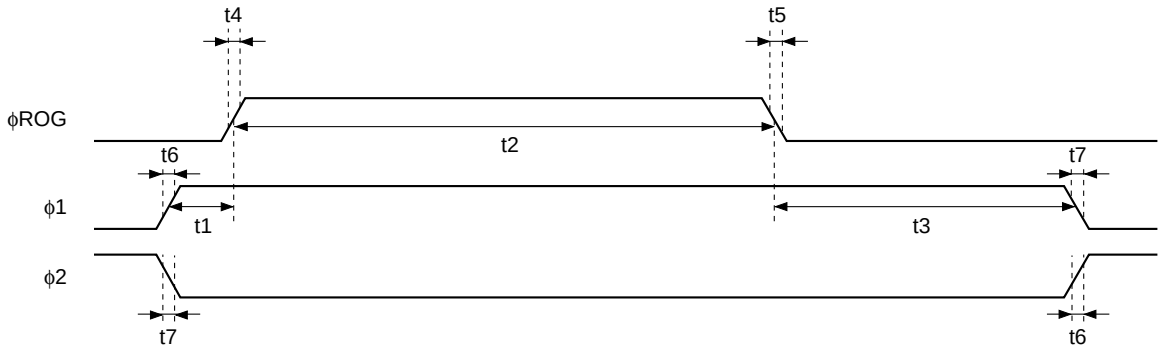
Note) The transfer pulse φ1, φ2, φ1L' and φ2L must have more than 10805 cycles.
φ3 and φ4 must have more than 21610 cycles.

Clock Timing Chart 2 (Using only Main Line)

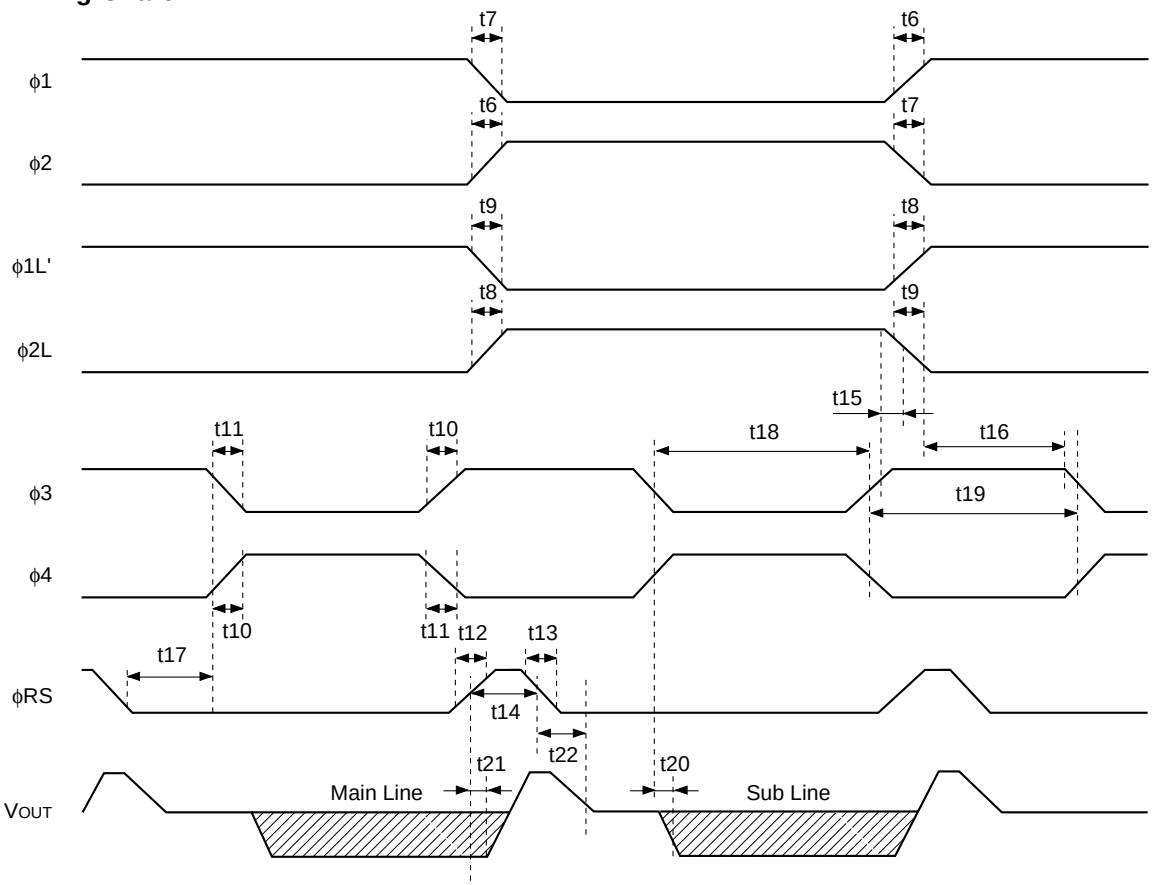


Note) The transfer pulse φ1, φ2, φ1L', φ2L, φ3 and φ4 have must more than 10816 cycles.

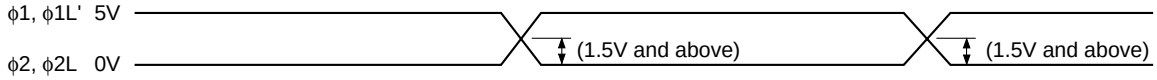
Clock Timing Chart 3



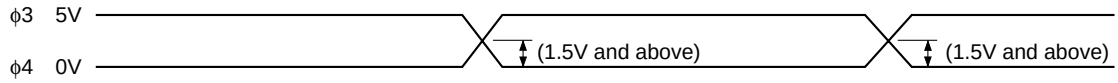
Clock Timing Chart 4



φ1, φ2, φ1L' and φ2L Cross Point



φ3 and φ4 Cross Point



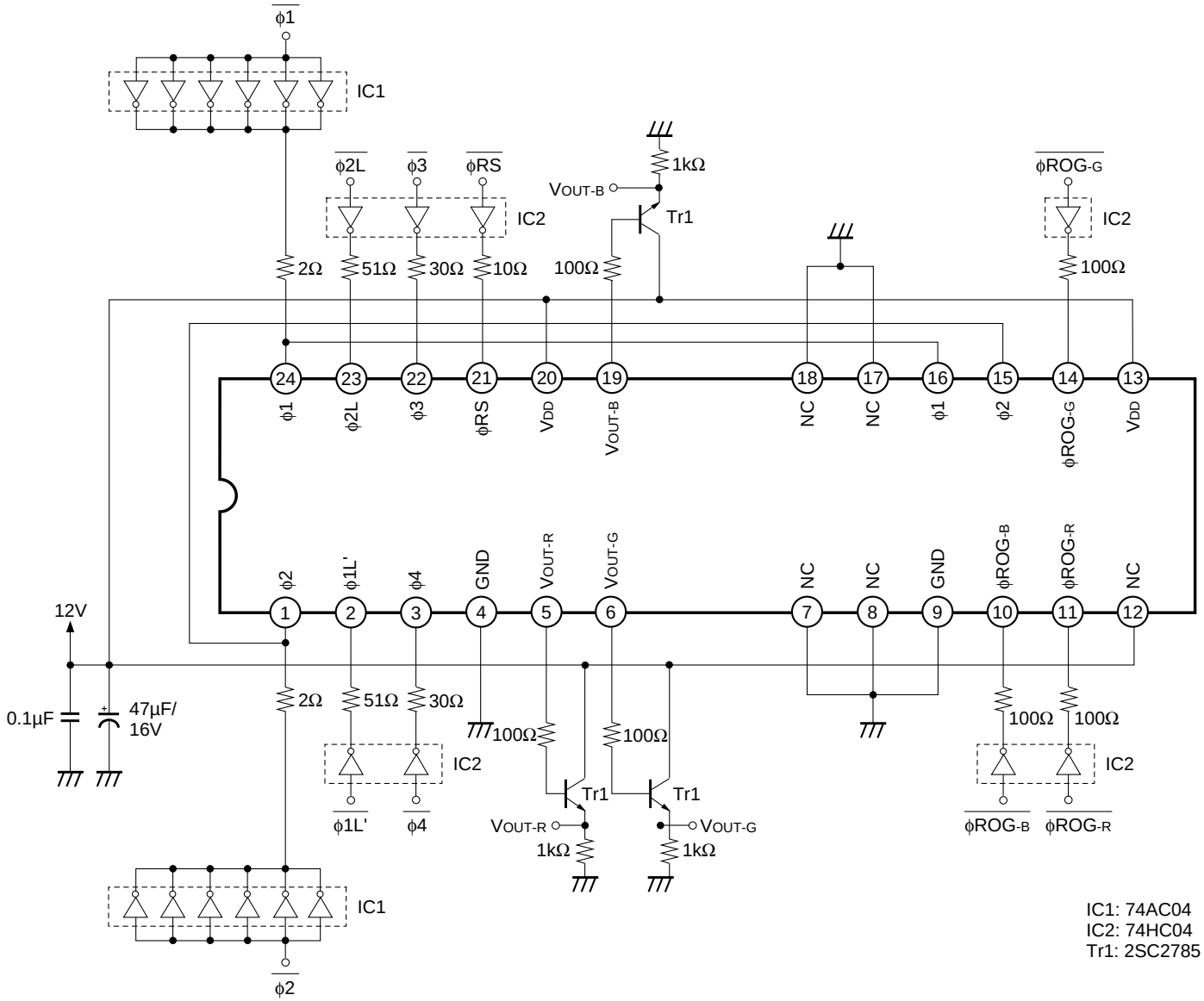
Clock Pulse Recommended Timing

Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φ1 pulse timing	t1	50	100	—	ns
φROG pulse high level period	t2	100	—	—	µs
φROG, φ1 pulse timing	t3	1200	1500	—	ns
φROG pulse rise time	t4	0	5	30	ns
φROG pulse fall time	t5	0	5	30	ns
φ1 pulse rise/φ2 pulse fall time	t6	0	20	60	ns
φ1 pulse fall/φ2 pulse rise time	t7	0	20	60	ns
φ1L' pulse rise/φ2L pulse fall time	t8	0	10	30*1	ns
φ1L' pulse fall/φ2L pulse rise time	t9	0	10	30*1	ns
φ3 pulse rise/φ4 pulse fall time	t10	0	10	30*1	ns
φ3 pulse fall/φ4 pulse rise time	t11	0	10	30*1	ns
φRS pulse rise time	t12	0	10	30*1	ns
φRS pulse fall time	t13	0	10	30*1	ns
φRS pulse high level period	t14	20	100*1	—	ns
φ1L', φ2L – φ3, φ4 pulse timing 1	t15	0	40	—	ns
φ1L', φ2L – φ3, φ4 pulse timing 2	t16	35	210*1	—	ns
φRS, φ3 pulse timing	t17	50	125*1	—	ns
φ3, φ4 pulse low level period	t18	35	250	—	ns
	t19	35	250	—	ns
Signal output delay time	t20	—	30	—	ns
	t21	—	10	—	ns
	t22	—	30	—	ns

The recommended duty of φ1, φ2, φ1L', φ2L, φ3 and φ4 = 50%.

*1 These timing is the recommended condition under $f_{\phi RS}$ = 2MHz.

Application Circuit

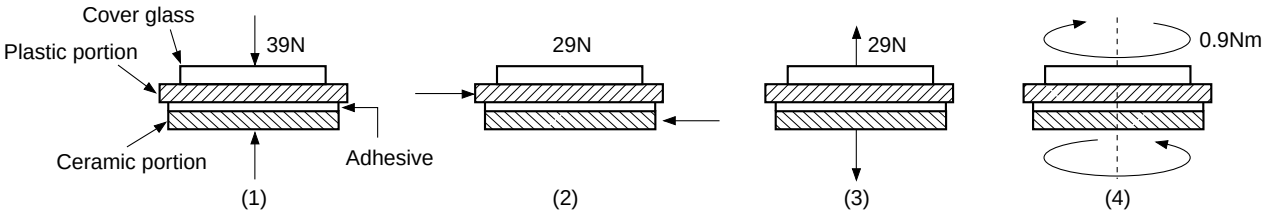


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes of Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Packages
   The following points should be observed when handling and installing packages.
   a) Remain within the following limits when applying static load to the package:
      (1) Compressive strength: 39N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
      (2) Shearing strength: 29N/surface
      (3) Tensile strength: 29N/surface
      (4) Torsional strength: 0.9Nm



   b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
   c) Be aware that any of the following can cause the package to crack or dust to be generated.
      (1) Applying repetitive bending stress to the external leads.
      (2) Applying heat to the external leads for an extended period of time with soldering iron.
      (3) Rapid cooling or heating.
      (4) Prying the plastic portion and ceramic portion away at a support point of the adhesive layer.
      (5) Applying the metal a crash or a rub against the plastic portion.
      Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.
   d) The notch of the plastic portion is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch or ceramic may overlap with the notch of the plastic portion.

3) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

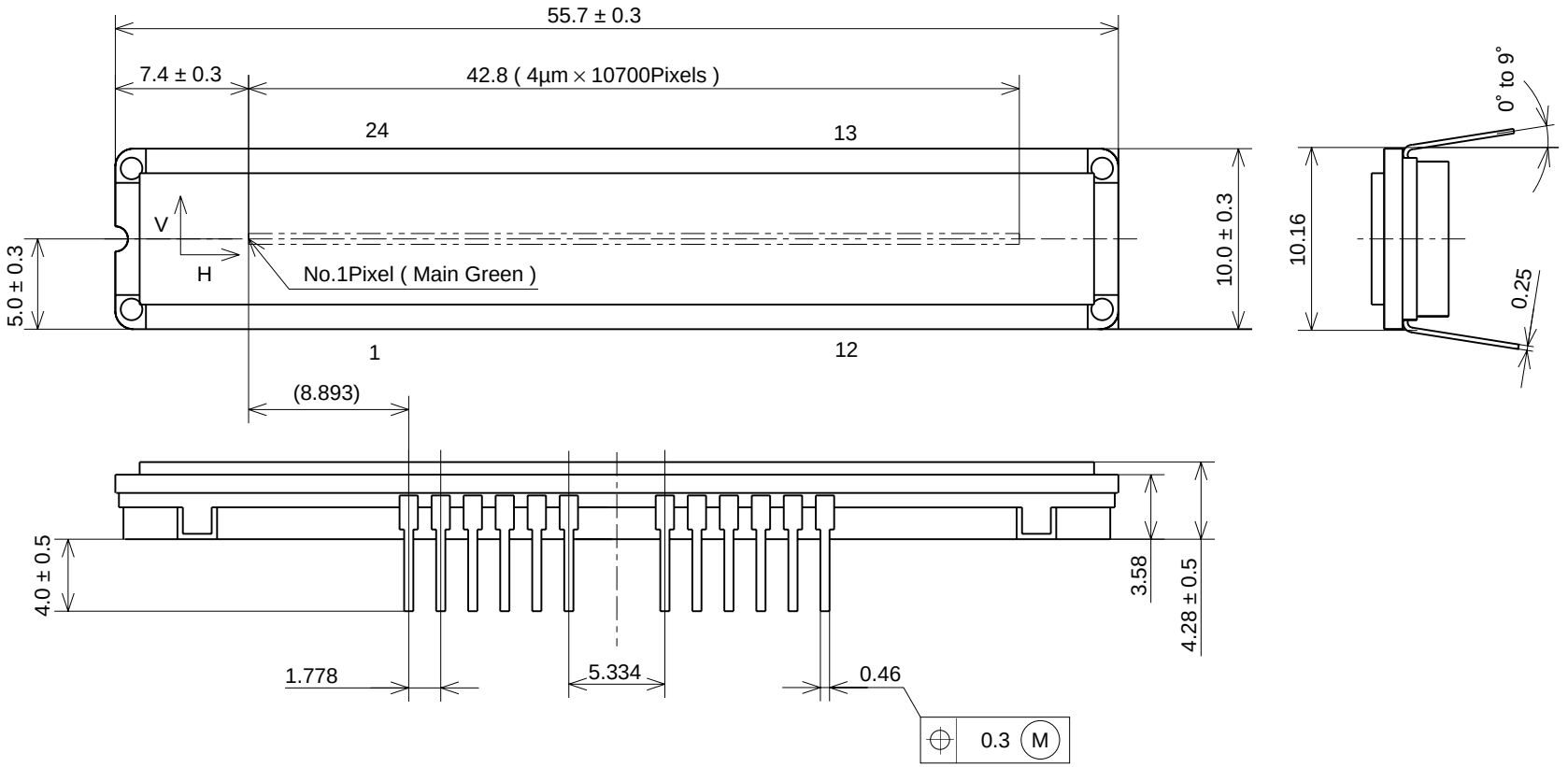
4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit: mm

24Pin DIP (400mil)



PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic, Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.43g
DRAWING NUMBER	LS-B36(E)

1. The height from the bottom to the sensor surface is 2.38 ± 0.3mm.
2. The thickness of the cover glass is 0.7mm, and the refractive index is 1.5.