SONY

ILX522K

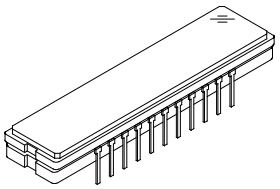
2048 × 2pixel CCD Linear Sensor (Color)

For the availability of this product, please contact the sales office.

Descriptions

The ILX522K is a reduction type CCD linear sensor designed for color image scanner use. This sensor reads B4 size documents at a density of 200 DPI. (Dot Per Inch), and has 2lines analog memories to adjust the position of green line and red/blue line. A built-in timing generator and clock-drivers ensure direct drive at 5V logic.

22 pin DIP (Cer-DIP)



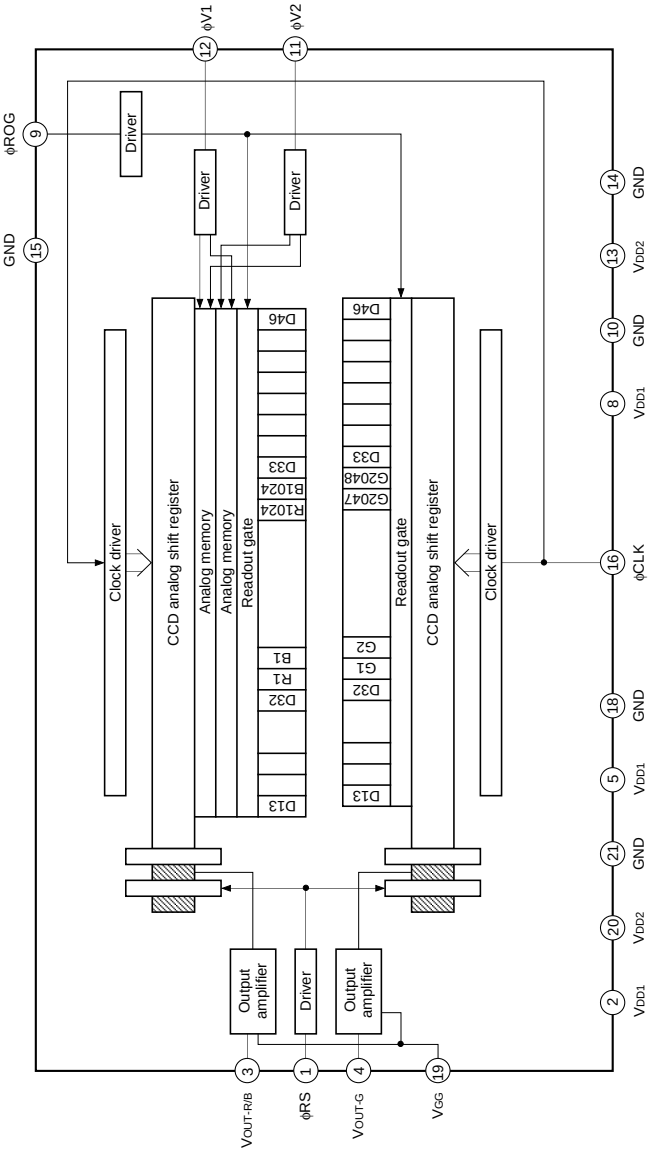
Features

- Number of effective pixels: 2048 × 2pixels
- Pixel size
  - Red/Blue pixel: 14µm × 12µm (14µm pitch)
  - Green pixel: 14µm × 14µm (14µm pitch)
- Built-in timing generator, clock-drivers
- Ultra-low lag
- Good linearity
- High sensitivity
- Input Clock Pulse: CMOS 5V drive

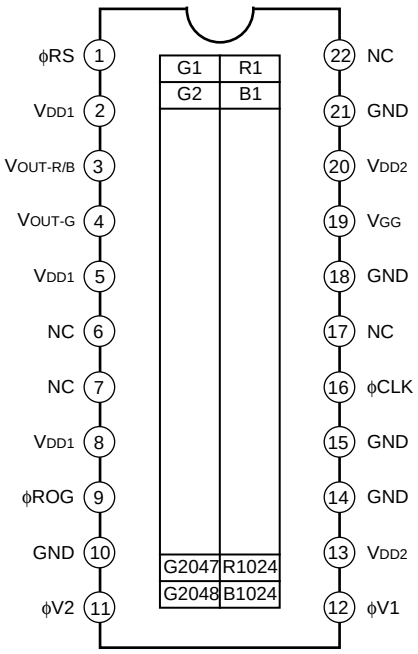
Absolute Maximum Ratings

• Supply voltage	V_{DD1}	11	V
	V_{DD2}	6	V

Block Diagram



Pin Configuration (Top View)



E95436-PP

Pin Description

Pin No.	Symbol	Description
1	ϕRS	Clock pulse input
2	V_{DD1}	9V power supply
3	$V_{OUT-R/B}$	R/B signal out
4	V_{OUT-G}	G signal out
5	V_{DD1}	9V power supply
6	NC	NC
7	NC	NC
8	V_{DD1}	9V power supply
9	ϕROG	Clock pulse input
10	GND	GND
11	ϕV2	Clock pulse input
12	ϕV1	Clock pulse input
13	V_{DD2}	5V power supply
14	GND	GND
15	GND	GND
16	ϕCLK	Clock pulse input
17	NC	NC
18	GND	GND
19	V_{GG}	Output gate bias
20	V_{DD2}	5V power supply
21	GND	GND
22	NC	NC

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD1}	8.5	9.0	9.5	V
V_{DD2}	4.75	5.0	5.25	V

Note) Rules for raising and lowering power supply voltage.
To raise power supply voltage, first raise V_{DD1} (9V) and then V_{DD2} (5V).
To lower voltage, first lower V_{DD2} (5V) and then V_{DD1} (9V).

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕRS, ϕCLK	CϕRS, CϕCLK	—	10	—	pF
Input capacity of ϕV1, ϕV2	CϕV1, CϕV2	—	10	—	pF
Input capacity of ϕROG	CϕROG	—	10	—	pF
Input clock frequency	fϕRS, fϕCLK	—	—	3.5	MHz

Electrical Characteristics (Note 1)

(Ta = 25°C, V_{DD1} = 9V, V_{DD2} = 5V fϕRS = 3.5MHz Light source = 3200K, IR cut filter CM-500S (t = 1.0mm))

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity	Red	R_R	5.2	8.0	10.8	V/(lx · s)	Note 2
	Green	R_G	6.5	10.0	13.5		
	Blue	R_B	2.8	4.3	5.8		
Sensitivity nonuniformity		PRNU	—	5.0	15.0	%	Note 3
Saturation output voltage		V_{SAT}	1.0	1.5	—	V	Note 4
Dark voltage average	Green	V_{DRK-G}	—	0.3	1.5	mV	Note 5
	Red/Blue	$V_{DRK-R/B}$	—	1.5	9.0		
Dark signal nonuniformity	Green	$DSNU_{-G}$	—	0.6	3.0		
	Red/Blue	$DSNU_{-R/B}$	—	2.0	12.0		
Image lag		IL	—	0.02	—	%	Note 6
9V supply current		I_{VDD1}	—	20	40	mA	—
5V supply current		I_{VDD2}	—	16.0	32.0	mA	—
Total transfer efficiency		TTE	92.0	98.0	—	%	—
Output impedance		Z_O	—	150	—	Ω	—
Offset level		V_{OS}	—	5.4	—	V	Note 7

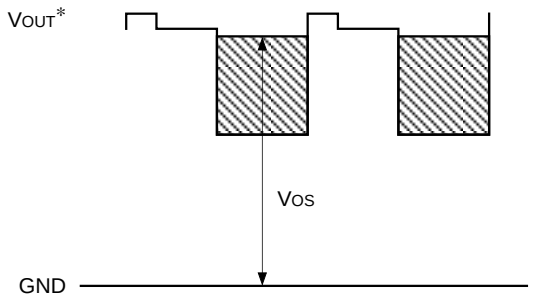
Note:

1) In accordance with the given electrooptical characteristics, the black level is defined as the average of D3, D4, to D10.
2) For the sensitivity test light is applied with a uniform intensity of illumination.
3) PRNU is defined as indicated below in each color. Ray incidence conditions are the same as for Note 2.

$$PRNU = \frac{(V_{MAX} - V_{MIN})/2}{V_{AVE}} \times 100\ [\%]$$

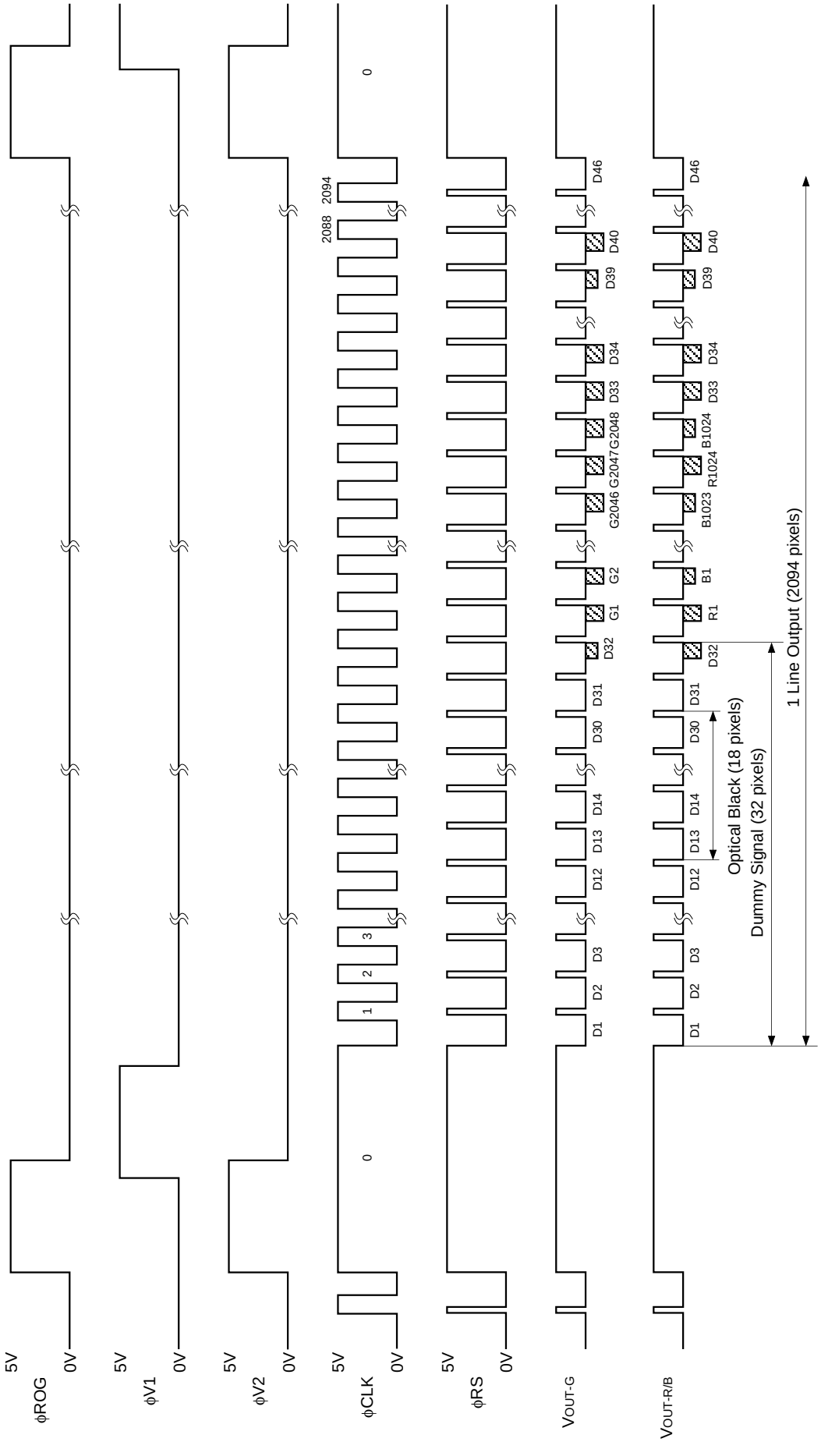
The maximum output of each color is set to V_{MAX}, the minimum output to V_{MIN}, and the average output to V_{AVE}.

4) Use below the minimum value of the saturation output voltage.
5) Optical signal accumulated time τint stands at 5ms.
6) V_{OUT-G} = 500mV (Typ.)
7) V_{OS} is defined as indicated below.



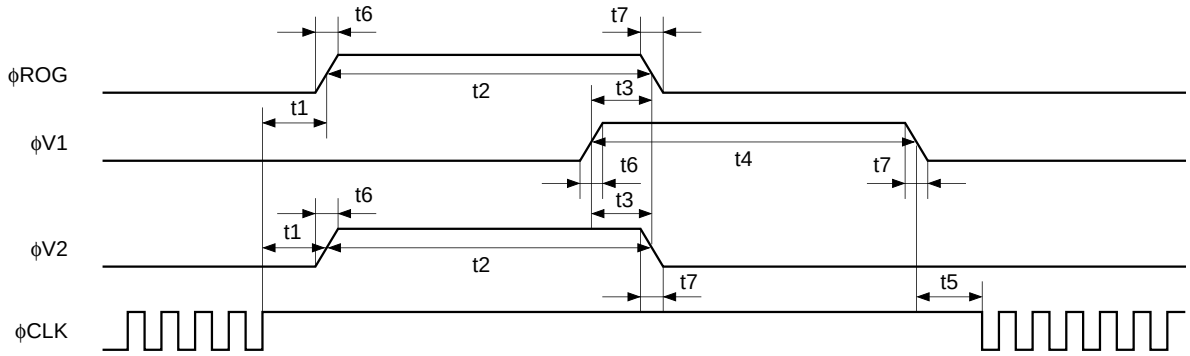
* V_{OUT} indicates V_{OUT-G} and $V_{OUT-R/B}$.

Clock Timing Chart



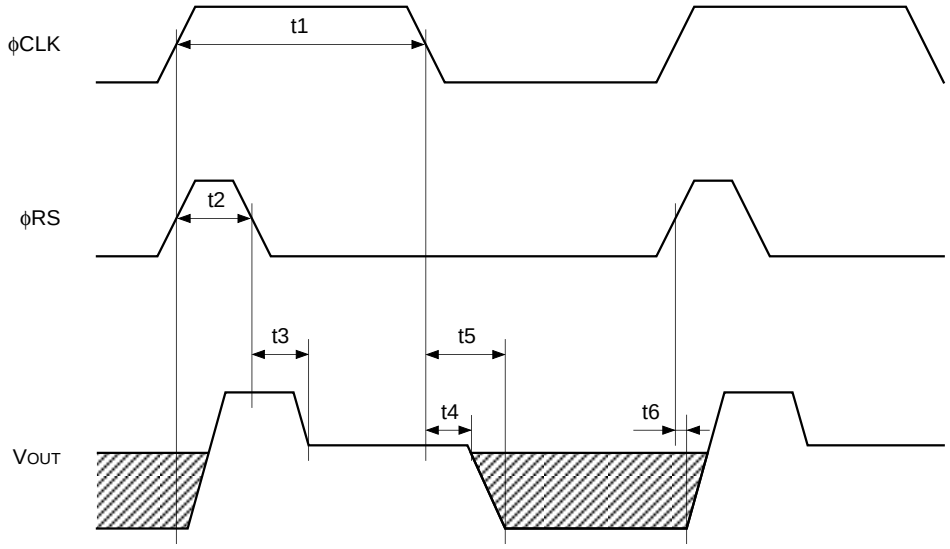
Note) φCLK, φRS pulses must have more than 2094 cycles.

φROG, φV1, φV2, φCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φV2 – φCLK pulse timing	t1	1	2	—	µs
φROG, φV1, φV2 pulse period	t2, t4	28	30	—	µs
φROG – φV1 pulse timing	t3	1	2	—	µs
φV1 – φCLK pulse timing	t5	1	2	—	µs
φROG, φV1, φV2 pulse rise time, fall time	t6, t7	0	10	30	ns

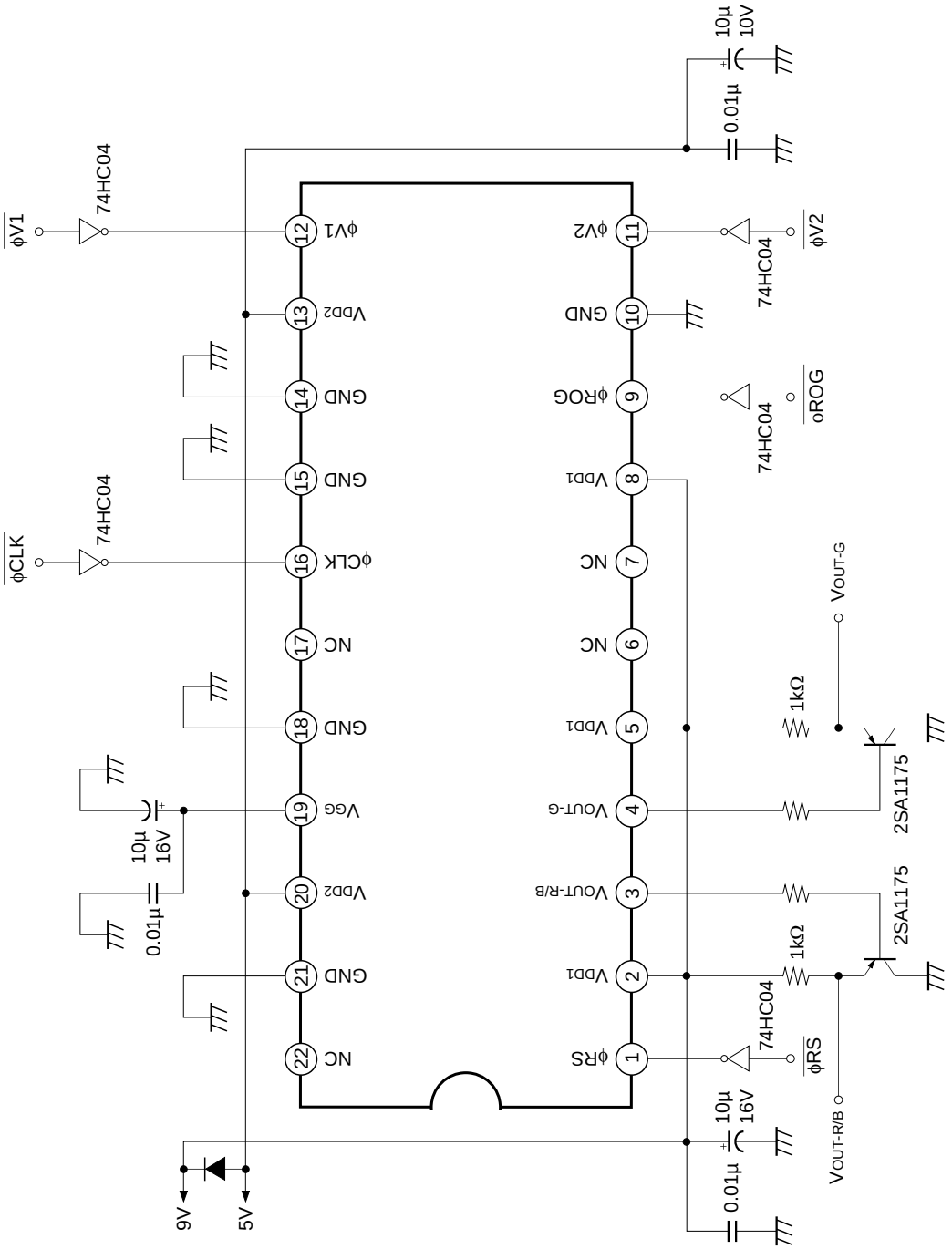
φCLK, φRS, VOUT Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse high level period	t1	135	500*	—	ns
φRS pulse high level period	t2	30	250*	—	ns
Signal output delay time	t3	—	60	—	ns
	t4	—	25	—	ns
	t5	—	70	—	ns
	t6	—	25	—	ns

* These timing is the condition under fφRS = 1MHz.

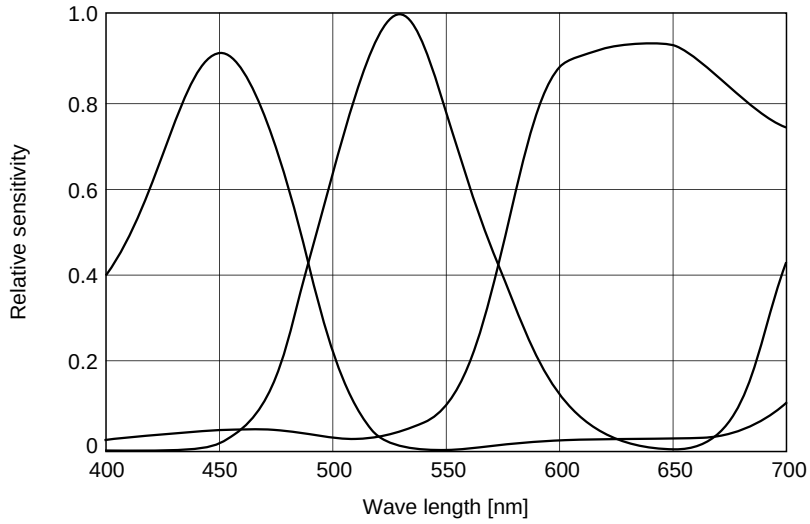
Application Circuit



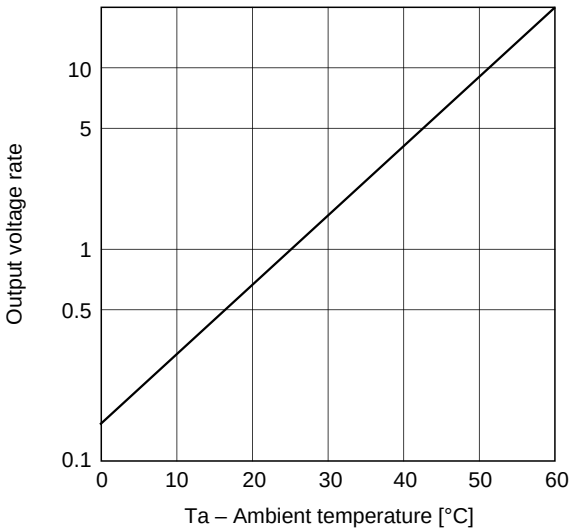
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics (V_{DD1} = 9V, V_{DD2} = 5V, Ta = 25°C)

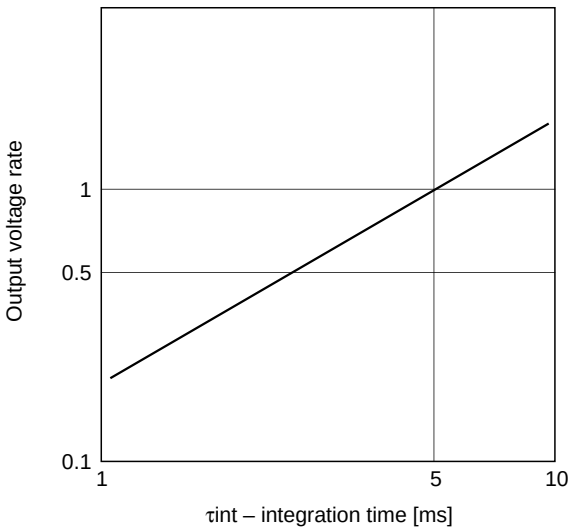
Spectral sensitivity characteristics (Standard characteristics)



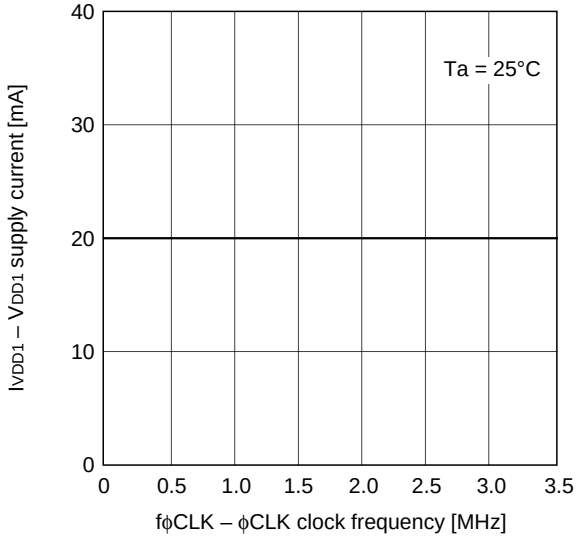
Dark signal output temperature characteristics (Standard characteristics)



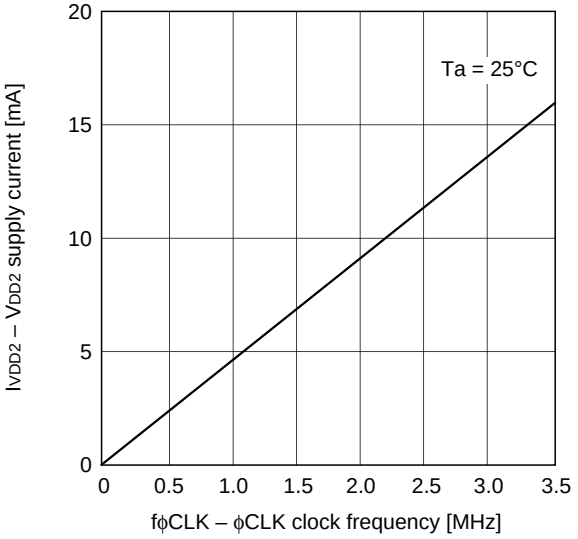
Integration time output voltage characteristics (Standard characteristics)



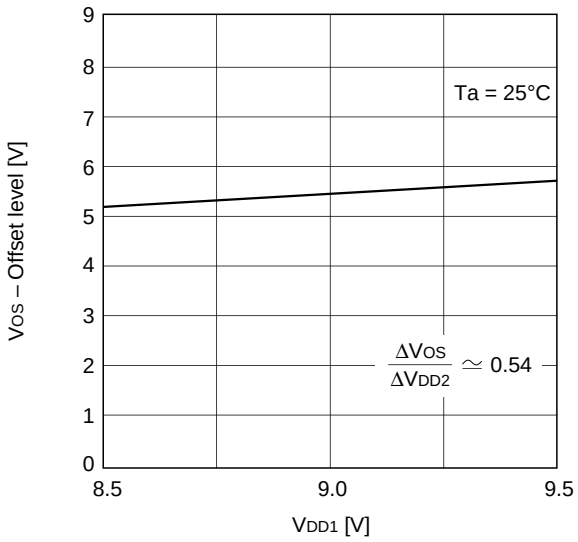
Operational frequency characteristics of the V_{DD1} supply current (Standard characteristics)



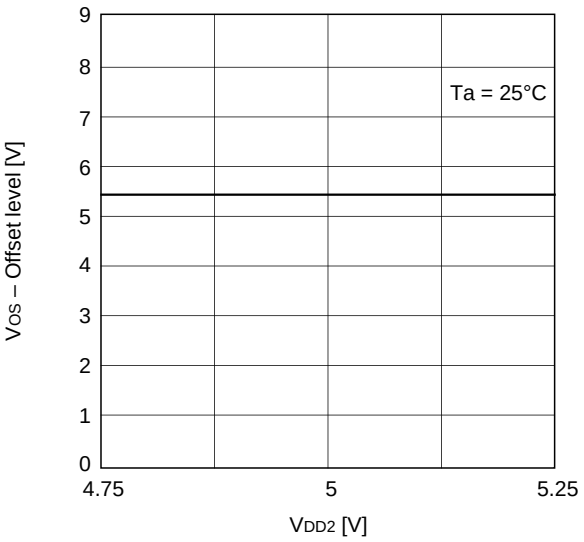
Operational frequency characteristics of the V_{DD2} supply current (Standard characteristics)



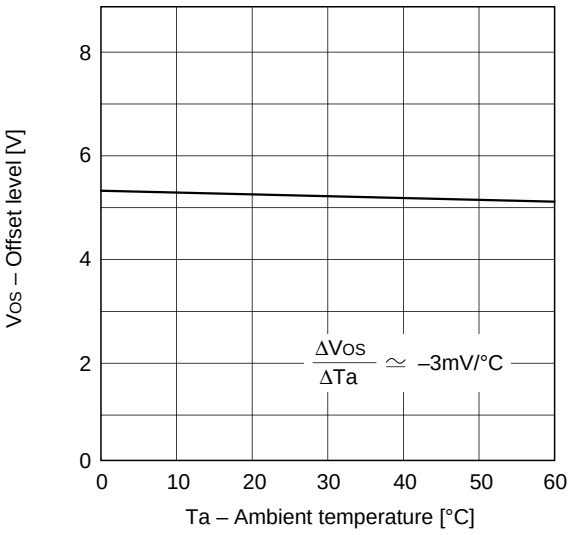
Offset level vs. V_{DD1} characteristics (Standard characteristics)



Offset level vs. V_{DD2} characteristics (Standard characteristics)



Offset level vs. Temperature characteristics (Standard characteristics)



Notes of Handling

1) Static charge prevention

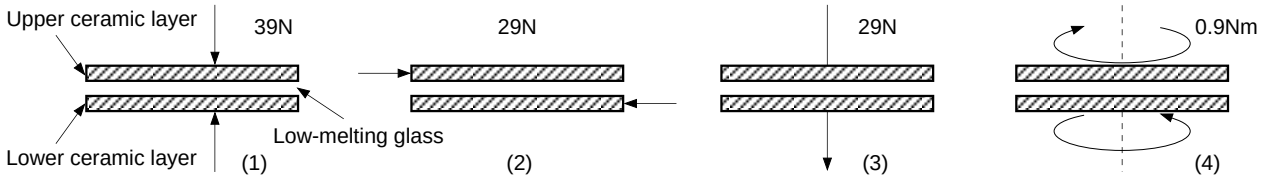
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.

2) Notes on Handling CCD Cer-DIP Packages

The following points should be observed when handling and installing cer-DIP packages.

a) Remain within the following limits when applying static load to the ceramic portion of the package:
   (1) Compressive strength: 39 N/surface (Do not apply load more than 0.7mm inside the outer perimeter of the glass portion.)
   (2) Shearing strength: 29 N/surface
   (3) Tensile strength: 29 N/surface
   (4) Torsional strength: 0.9 Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.
c) Be aware that any of the following can cause the glass to crack: because the upper and lower ceramic layers are shielded by low-melting glass,
   (1) Applying repetitive bending stress to the external leads.
   (2) Applying heat to the external leads for an extended period of time with soldering iron.
   (3) Rapid cooling or heating
   (4) Rapid cooling or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.
   (5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

   Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

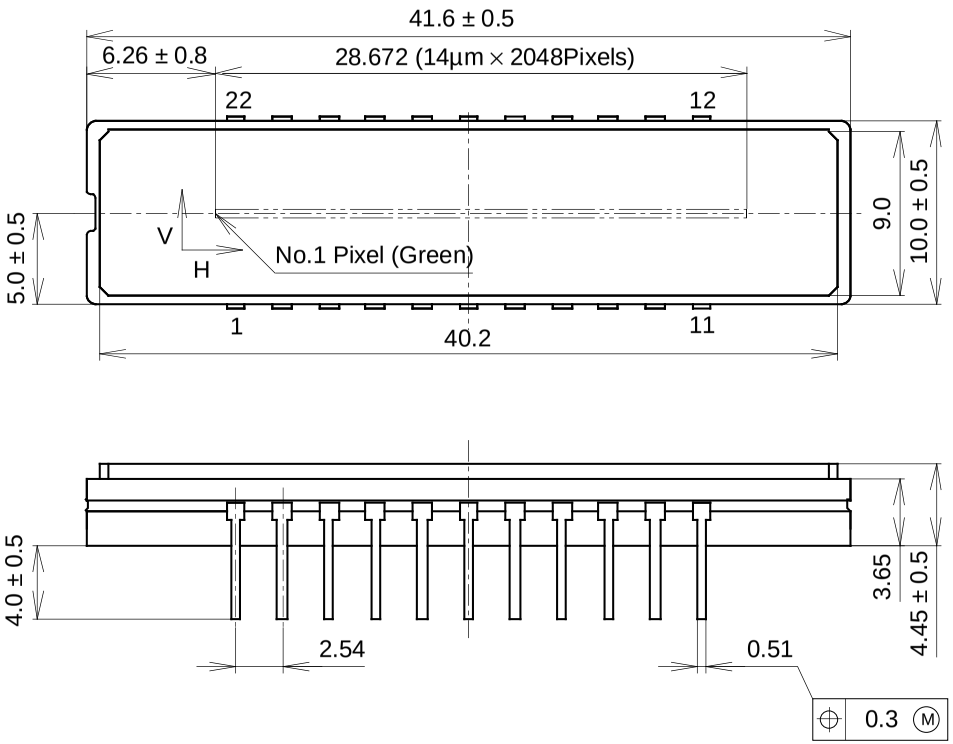
5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

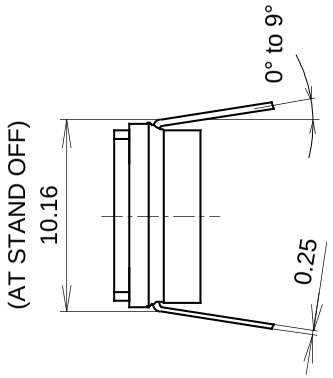
6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

7) Since ILX522K has 2 line memory so that the signal of R/B line is delay, compese the optical system sub-scanning R/B line initially.

Package Outline Unit: mm

22pin DIP (400mil)





1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g