CIPOS™ Mini IPM

IM06B50GC1, 600 V 50 A

Description

The CIPOS™ Mini IPM, IM06B50GC1 offers the chance for integrating various power and control components to increase reliability and optimize PCB size and system cost. It is designed to control 3-phase motors in variable speed drives. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also less EMI and overload protection. To deliver excellent electrical performance, Infineon's leading-edge TRENCHSTOP™ IGBTs and anti-parallel diodes are combined with an optimized SOI gate driver.

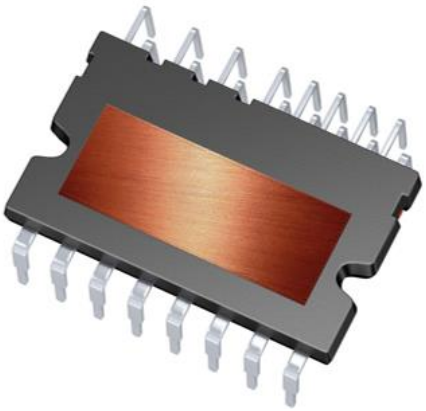
Features

Package

- Fully isolated dual in-line molded module
- Lead-free terminal plating; RoHS compliant

Inverter

- 650 V TRENCHSTOP™ IGBT7 T7
- 600 V Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative V_S potential up to -11 V for signal transmission at V_{BS} = 15 V
- Integrated bootstrap functionality
- Overcurrent shutdown
- Built-in NTC thermistor for temperature monitor
- Undervoltage lockout at all channels
- Low-side emitter pins accessible for phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection



Potential applications

- Air-conditioners
- Heat-pump application
- Home appliances
- Motor drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Table 1 Product Information

Base Part Number	Package Type	Standard Pack		Remarks
		Form	MOQ	
IM06B50GC1	DIP 36x21D	14 pcs / Tube	280 pcs	

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1 Internal electrical schematic

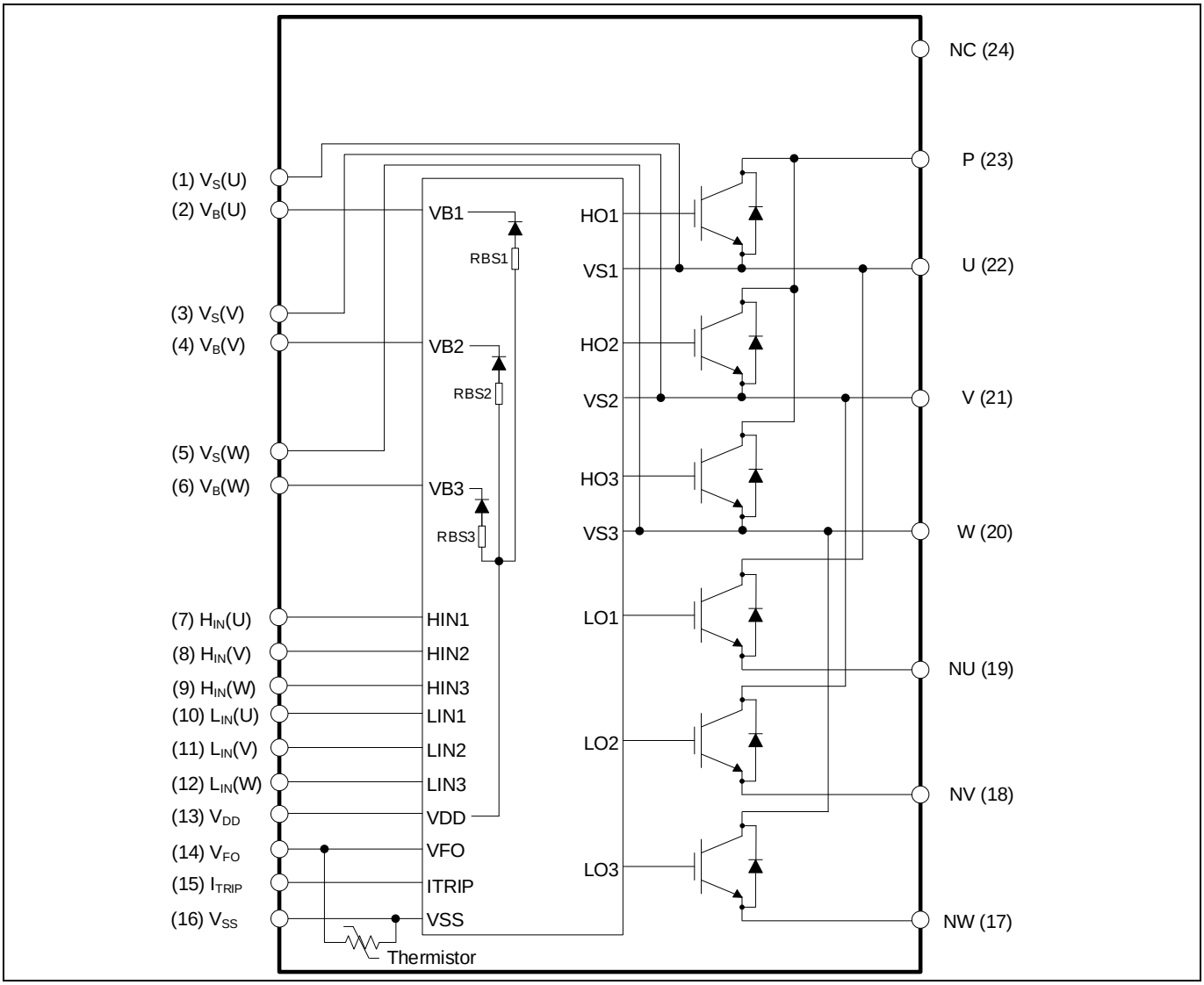


Figure 1 Internal electrical schematic

2 Pin description

2.1 Pin assignment

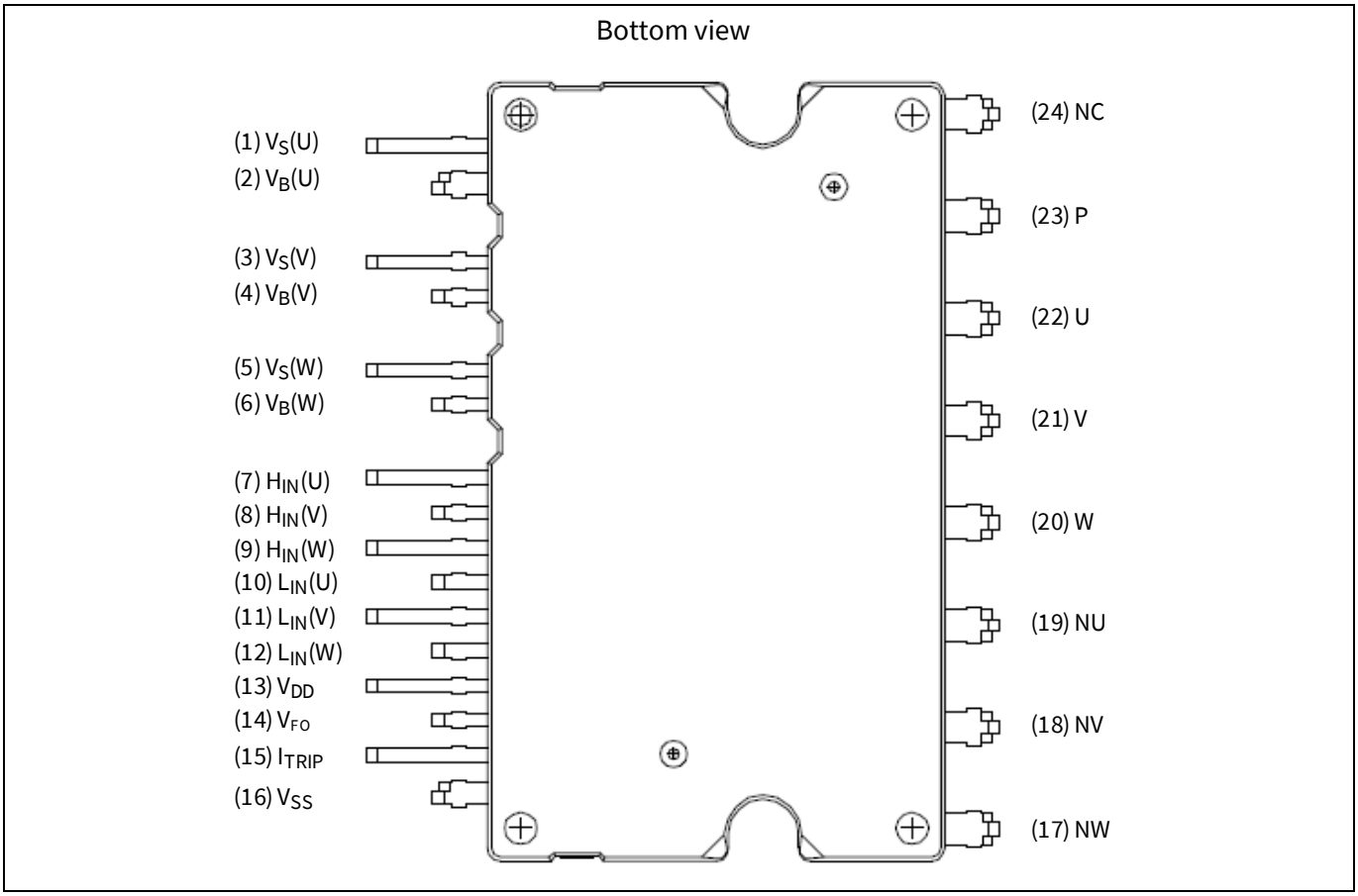


Figure 2 Pin assignment

Table 2 Pin assignment

Pin number	Pin name	Pin description
1	V_S(U)	U-phase high-side floating IC supply offset voltage
2	V_B(U)	U-phase high-side floating IC supply voltage
3	V_S(V)	V-phase high-side floating IC supply offset voltage
4	V_B(V)	V-phase high-side floating IC supply voltage
5	V_S(W)	W-phase high-side floating IC supply offset voltage
6	V_B(W)	W-phase high-side floating IC supply voltage
7	H_{IN}(U)	U-phase high-side gate driver input
8	H_{IN}(V)	V-phase high-side gate driver input
9	H_{IN}(W)	W-phase high-side gate driver input
10	L_{IN}(U)	U-phase low-side gate driver input
11	L_{IN}(V)	V-phase low-side gate driver input
12	L_{IN}(W)	W-phase low-side gate driver input
13	V_{DD}	Low-side control supply
14	V_{FO}	Fault output / temperature monitor
15	I_{TRIP}	Overcurrent shutdown input

Pin number	Pin name	Pin description
16	V_{SS}	Low-side control negative supply
17	NW	W-phase low-side emitter
18	NV	V-phase low-side emitter
19	NU	U-phase low-side emitter
20	W	Motor W-phase output
21	V	Motor V-phase output
22	U	Motor U-phase output
23	P	Positive bus input voltage
24	NC	No connection

2.2 Pin description

H_{IN} (U, V, W) and L_{IN} (U, V, W) (Low-side and high-side control pins, Pin 7 - 12)

These pins are positive logic, and they are responsible for the control of the integrated IGBTs. The schmitt-trigger input thresholds of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. A pull-down resistor of about 5 kΩ is internally provided to pre-bias inputs during supply start-up, and a zener clamp is provided to protect the pins. Negative pulses down to an absolute minimum of -5.5 V are allowed that offers an outstanding robustness. Input schmitt-trigger and noise filter provide noise rejection to short input pulses.

The noise filter suppresses control pulses shorter than the filter time $t_{FIL,\ IN}$. The Figure 4 describes how the filter works. An input pulse-width shorter than 1 µs is not recommended.

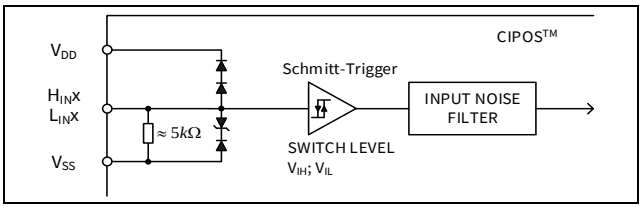


Figure 3 Input pin structure

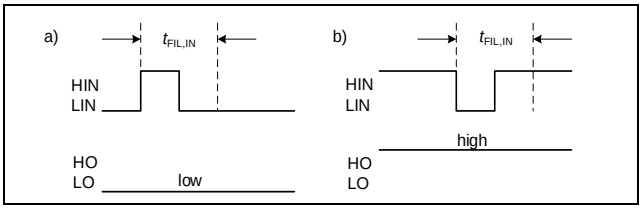


Figure 4 Input filter timing diagram

The integrated gate driver additionally provides a shoot-through prevention capability that avoids the simultaneous on-states of the same leg. When both inputs of the same leg are activated, only formerly activated one remained activated so that the leg is kept steadily in a safe state.
A minimum deadtime insertion of typically 360 ns is also provided by driver, to reduce cross-conduction of the IGBTs.

V_{FO} (Fault-output and NTC, Pin 14)

The V_{FO} pin indicates a module failure in case of undervoltage at pin V_{DD} or in case of triggered overcurrent detection at I_{TRIP}. An external pull-up resistor is required.

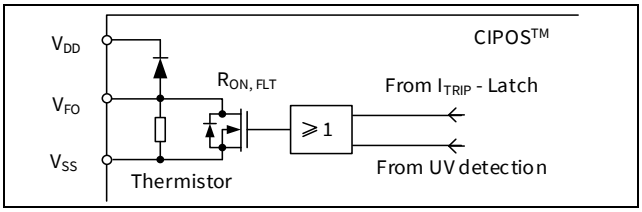


Figure 5 Internal circuit at pin V_{FO}

The sleep function is activated after each trigger of I_{TRIP} or undervoltage lockout. A new edge input signal is mandatory to activate gate drives after falut-clear time.

I_{TRIP} (Overcurrent detection function, Pin 15)

This product family provides an overcurrent detection function by connecting the I_{TRIP} input with the IGBT current feedback. The I_{TRIP} comparator threshold (typ. 0.525 V) is referenced to V_{SS}. An input noise filter (t_{ITRIP} = typ. 530 ns) prevents the driver to detect false overcurrent events.

Overcurrent detection generates a shutdown of outputs of the gate driver. Fast track shutdown function allows low-side outputs to be turned off faster than high side outputs about 200 ns.
The fault-clear time is set to minimum 100 µs.

V_{DD}, V_{SS} (Low-side control supply and reference, Pin 13, 16)

V_{DD} is the control supply, and it provides power both to input logic and to output stage. Input logic is referenced to V_{SS} ground.
The undervoltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of V_{DDUV+} = 12.4 V is present.
The gate driver shuts down all the outputs, when the V_{DD} supply voltage is below V_{DDUV-} = 11.5 V. This prevents the IGBTs from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

V_B (U, V, W) and V_S (U, V, W) (High-side supplies, Pin 1 - 6)

V_B to V_S is the high-side supply voltage. The high-side circuit can float with respect to V_{SS} following the high-side IGBT emitter voltage.
Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The undervoltage detection operates with a rising supply threshold of typical V_{BSUV+} = 11.5 V and a falling threshold of V_{BSUV-} = 10.7 V.
V_S (U, V, W) provide a high robustness against negative voltage in respect of V_{SS} of -50 V transiently. This ensures very stable designs even under harsh conditions.

NW, NV, NU (Low-side emitter, Pin 17 - 19)

The low-side emitters are available for current measurement of each phase leg. It is recommended to keep the connection to pin V_{SS} as short as possible to avoid unnecessary inductive voltage drops.

W, V, U (High-side emitter and low-side collector, Pin 20 - 22)

These pins are connected to motor U, V, W input pins

P (Positive bus input voltage, Pin 23)

The high-side IGBTs are connected to the bus voltage. It is noted that the bus voltage does not exceed 450 V.

3 Absolute maximum ratings

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

3.1 Module section

Description	Symbol	Condition	Value	Unit
Storage temperature range	T_{STG}		-40 ~ 125	°C
Operating case temperature	T_C	Refer to Figure 7	-40 ~ 125	°C
Operating junction temperature	T_J		-40 ~ 150	°C
Maximum junction temperature[1]	$T_{J, switch, max}$		175	°C
Isolation test voltage	V_{ISO}	1 min, RMS, f = 60 Hz	2000	V

3.2 Inverter section

Description	Symbol	Condition	Value	Unit
Max. blocking voltage	V_{CES}		600	V
DC link supply voltage of P-N	V_{PN}	Applied between P-N	450	V
DC link supply voltage (surge) of P-N	$V_{PN (surge)}$	Applied between P-N	500	V
Each IGBT collector current[2]	I_C	T_C = 25°C, T_J < 150°C	35	A
Each IGBTcollector peak current[1]	I_{CP}	T_C = 25°C, T_J < 150°C less than 1 ms	100	A
Maximum peak output current	$I_{O (peak)}$	Sine-wave, T_C = 25°C, $f_O \geq 1$ Hz	50	A
Power dissipation per IGBT	P_{tot}		216	W
Short circuit withstand time	t_{SC}	$V_{DC} \leq 360V$, T_J = 150°C	3	µs

3.3 Control section

Description	Symbol	Condition	Value	Unit
High side offset voltage	V_S		600	V
Repetitive peak reverse voltage of bootstrap diode	V_{RRM}		600	V
Module supply voltage	V_{DD}		-1 ~ 20	V
High-side floating supply voltage (V_B reference to V_S)	V_{BS}		-1 ~ 20	V
Input voltage (L_{IN}, H_{IN}, I_{TRIP})	V_{IN}		-1 ~ V_{DD}+0.3	V

[1]The maximum junction temperature rating of built in power chips is 175℃ under condition: max. 10 sec, every 10 min, max. 1 hrs cumulative over lifetime.

[2] Pulse width and period are limited by junction temperature

4 Thermal characteristics

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Single IGBT thermal resistance, junction to case	R_{thJC}	See Figure 7 for T_C measurement point	-	-	0.6	K/W
Single diode thermal resistance, junction-case	$R_{thJC,D}$		-	-	1.0	K/W

5 Recommended operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified.

Description	Symbol	Value			Unit
		Min.	Typ.	Max.	
DC link supply voltage of P-N	V_{PN}	0	300	400	V
Low-side supply voltage	V_{DD}	13.0	15.0	17.5	V
High-side floating supply voltage (V_B vs. V_S)	V_{BS}	13.0	-	17.5	V
Logic input voltages L_{IN}, H_{IN}, I_{TRIP}	V_{IN} V_{ITRIP}	0	-	5.0	V
Inverter PWM carrier frequency	f_{PWM}	-	-	20	kHz
External deadtime between H_{IN} and L_{IN}	DT	2.0	-	-	µs
Voltage between V_{SS} – N (including surge)	V_{COMP}	-5.0	-	5.0	V
Minimum input pulse width	$PW_{IN(ON)}$ $PW_{IN(OFF)}$	1.0	-	-	µs
Control supply variation	$\Delta V_{BS,}$ ΔV_{DD}	-1.0 -1.0	- -	1.0 1.0	V/µs

6 Static parameters

(V_{DD} = V_{BS} = 15 V and T_J = 25°C, if not stated otherwise)

6.1 Inverter section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Collector-emitter voltage	$V_{CE(Sat)}$	I_C = 50 A, T_J = 25°C I_C = 50 A, T_J = 150°C	- -	1.80 2.15	2.20 -	V
Collector-emitter leakage current	I_{CES}	V_{CE} = 600 V	-	-	1	mA
Diode forward voltage	V_F	I_F = 50 A, T_J = 25°C I_F = 50 A, T_J = 150°C	- -	2.30 2.25	- -	V

6.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Logic "1" input voltage (L_{IN}, H_{IN})	V_{IH}		1.7	2.0	2.3	V
Logic "0" input voltage (L_{IN}, H_{IN})	V_{IL}		0.7	0.9	1.1	V
I_{TRIP} positive going threshold	$V_{IT,TH+}$		475	525	570	mV
I_{TRIP} input hysteresis	$V_{IT,HYS}$		45	70	-	mV
V_{DD} and V_{BS} supply undervoltage positive going threshold	V_{DDUV+}		11.5	12.4	13.1	V
	V_{BSUV+}		10.6	11.5	12.2	
V_{DD} and V_{BS} supply undervoltage negative going threshold	V_{DDUV-}		10.6	11.5	12.3	V
	V_{BSUV-}		9.7	10.7	11.7	
V_{DD} and V_{BS} supply undervoltage lockout hysteresis	V_{DDUVH} V_{BSUVH}		0.5	0.9	-	V
Quiescent V_{Bx} supply current (V_{Bx} only)	I_{QBS}	H_{IN} = 0 V	-	-	300	µA
Quiescent V_{DD} supply current (V_{DD} only)	I_{QDD}	L_{IN} = 0 V, H_{INX} = 5 V	-	-	1.1	mA
Input bias current for L_{IN}, H_{IN}	I_{IN+}	V_{IN} = 5 V	-	1.1	1.7	mA
Input bias current for I_{TRIP}	I_{ITRIP+}	V_{ITRIP} = 5 V	-	68	185	µA
Input bias current for V_{FO}	I_{FO}	V_{FO} = 5 V, V_{ITRIP} = 0 V	-	60	-	µA
V_{FO} output voltage	V_{FO}	I_{FO} = 10 mA, V_{ITRIP} = 1 V	-	0.35	-	V
Bootstrap diode forward voltage	V_{F_BSD}	I_F = 0.3 mA	-	1.0	-	V
Bootstrap diode resistance	R_{BSD}	Between V_{F1} = 4 V and V_{F2} = 5 V	-	37	-	Ω

7 Dynamic parameters

(V_{DD} = 15 V and T_J = 25°C, if not stated otherwise)

7.1 Inverter section

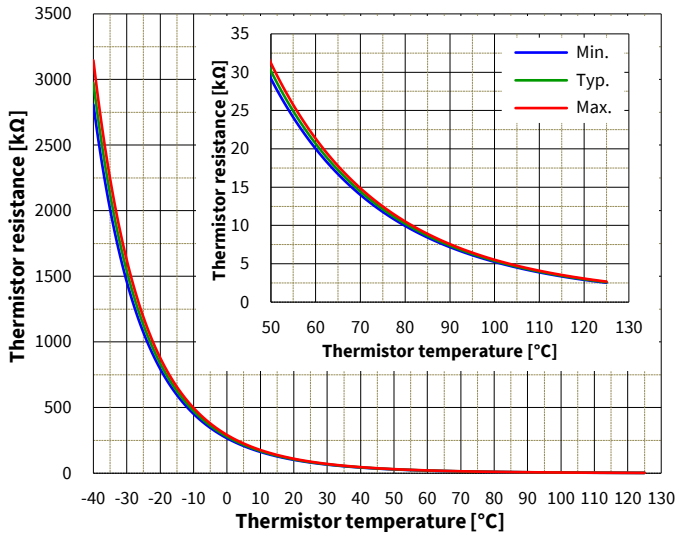
Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Turn-on propagation delay time	t_{on}	$V_{LIN, HIN}$ = 5 V, I_C = 50 A, V_{DC} = 300 V	-	860	-	ns
Turn-on rise time	t_r		-	85	-	ns
Turn-on switching time	$t_{c(on)}$		-	285	-	ns
Reverse recovery time	t_{rr}		-	235	-	ns
Turn-off propagation delay time	t_{off}	$V_{LIN, HIN}$ = 0 V, I_C = 50 A, V_{DC} = 300 V	-	1155	-	ns
Turn-off fall time	t_f		-	35	-	ns
Turn-off switching time	$t_{c(off)}$		-	110	-	ns
Short circuit propagation delay time	t_{SCP}	From $V_{IT, TH+}$ to 10% I_{SC}	-	1430	-	ns
IGBT turn-on energy (includes reverse recovery of diode)	E_{on}	V_{DC} = 300 V, I_C = 50 A T_J = 25°C T_J = 150°C	 - -	 2460 3460	 - -	µJ
IGBT turn-off energy	E_{off}	V_{DC} = 300 V, I_C = 50 A T_J = 25°C T_J = 150°C	 - -	 1080 1525	 - -	µJ
Diode recovery energy	E_{rec}	V_{DC} = 300 V, I_C = 50 A T_J = 25°C T_J = 150°C	 - -	 145 410	 - -	µJ

7.2 Control section

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input filter time I_{TRIP}	t_{ITRIP}	V_{ITRIP} = 1 V	-	530	-	ns
Input filter time at L_{IN}, H_{IN} for turn on and off	$t_{FIL, IN}$	$V_{LIN, HIN}$ = 0 V or 5 V	-	290	-	ns
Fault clear time after I_{TRIP}-fault	t_{FLTCLR}		100	280	-	µs
I_{TRIP} to fault propagation delay	t_{FLT}	$V_{LIN, HIN}$ = 0 or $V_{LIN, HIN}$ = 5 V, V_{ITRIP} = 1 V	-	680	1000	ns
Internal deadtime	DT_{IC}		-	360	-	ns
Matching propagation delay time (on and off) all channels	M_T	External dead time > 500 ns	-	20	-	ns

8 Thermistor

Description	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Resistance	R_{NTC}	T_{NTC} = 25°C	-	85	-	kΩ
B-constant of NTC (Negative temperature coefficient) thermistor	B (25/100)		-	4092	-	K



Temp. [°C]	$R_{Min.}$ [kΩ]	$R_{Typ.}$ [kΩ]	$R_{Max.}$ [kΩ]
50	29.151	30.157	31.178
60	20.018	20.669	21.329
70	13.994	14.424	14.858
80	9.946	10.234	10.523
90	7.177	7.373	7.569
100	5.253	5.388	5.523
110	3.884	3.99	4.096
120	2.908	2.991	3.075
125	2.527	2.601	2.676

Figure 6 Thermistor resistance – temperature curve and table
(For more information, please refer to the application note)

9 Mechanical characteristics and ratings

Description	Condition	Value			Unit
		Min.	Typ.	Max.	
Mounting torque	M3 screw and washer	0.59	-	0.78	Nm
Backside curvature	Refer to Figure 8	0	-	150	µm
Weight		-	6.60	-	g

10 Qualification information

UL certification	File number: E314539	
Moisture sensitivity level	-	
RoHS compliant	Yes (Lead-free terminal plating)	
ESD	HBM (human body model) class	2
	CDM (charged device model) class	C2a

11 Diagrams and tables

11.1 T_C Measurement point (top view)

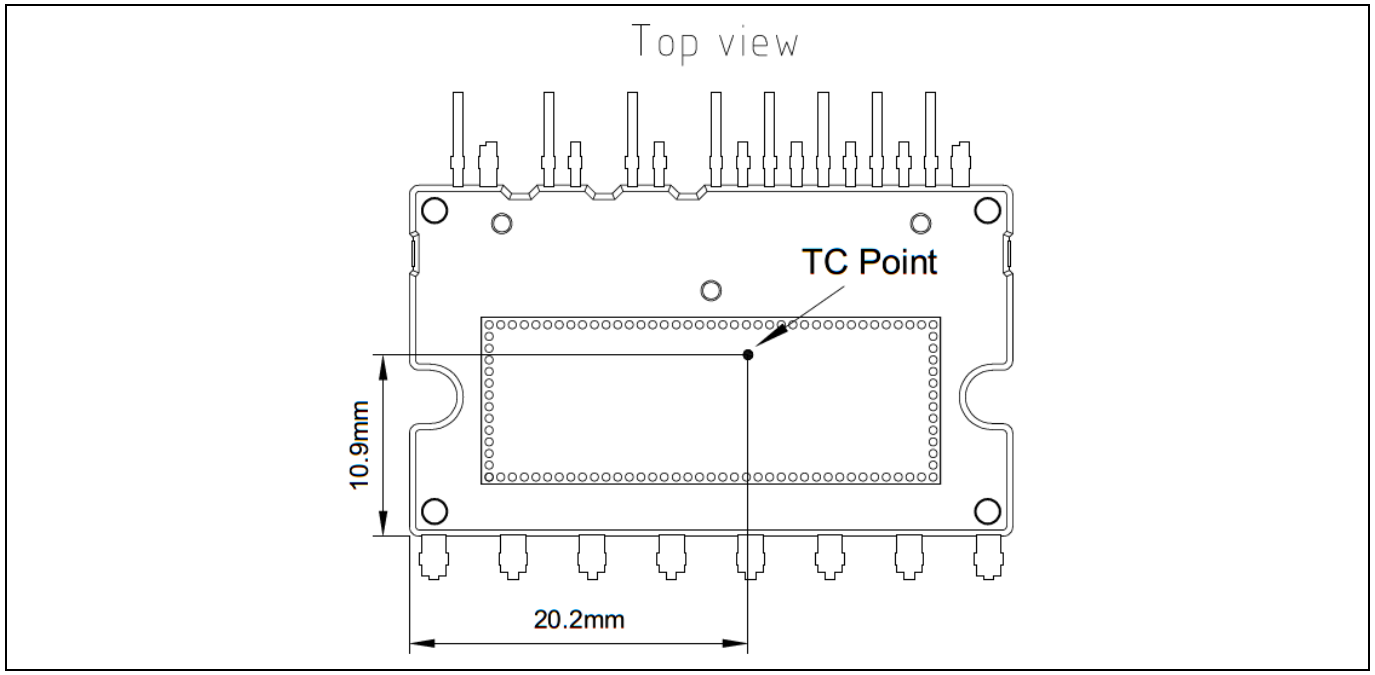


Figure 7 T_C measurement point[1]

11.2 Backside curvature measurment point

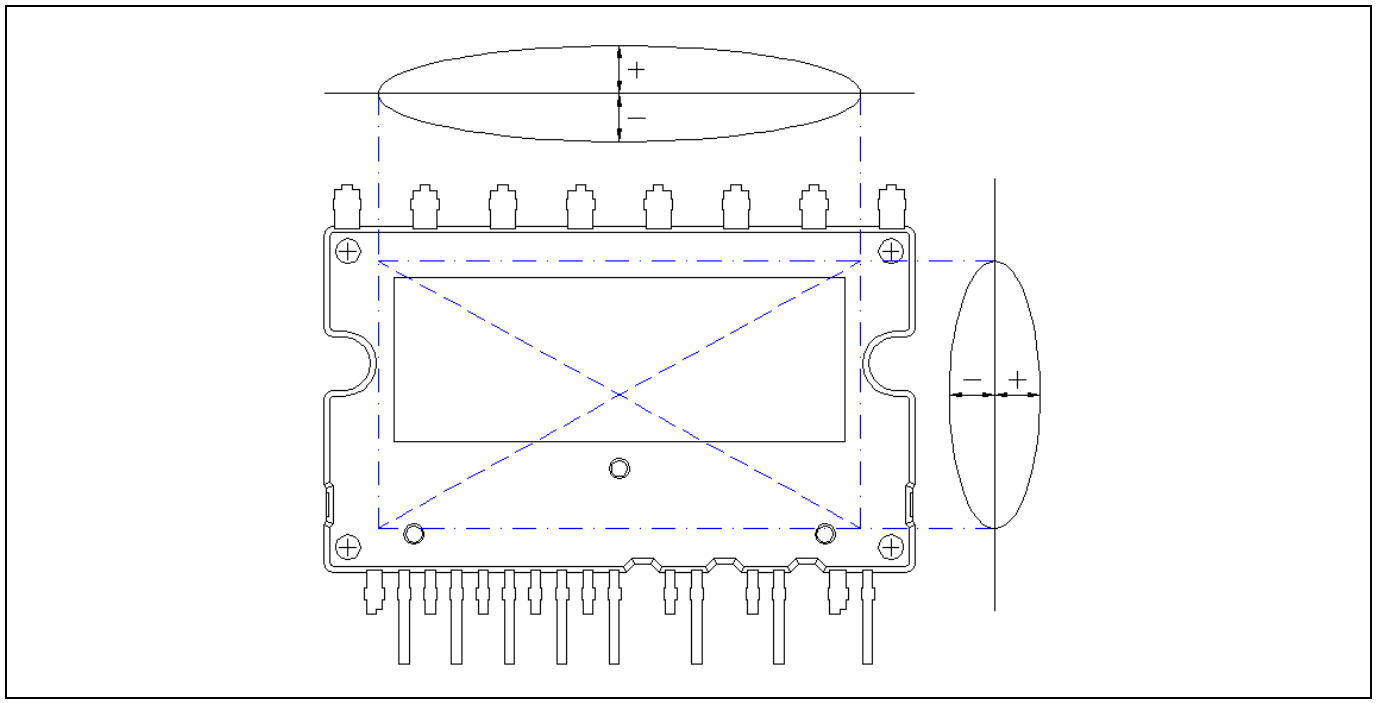


Figure 8 Backside curvature measurement position

[1]Any measurement except for the specified point in Figure 7 is not relevant for the temperature verification and brings wrong or different information.

11.3 Switching test circuit

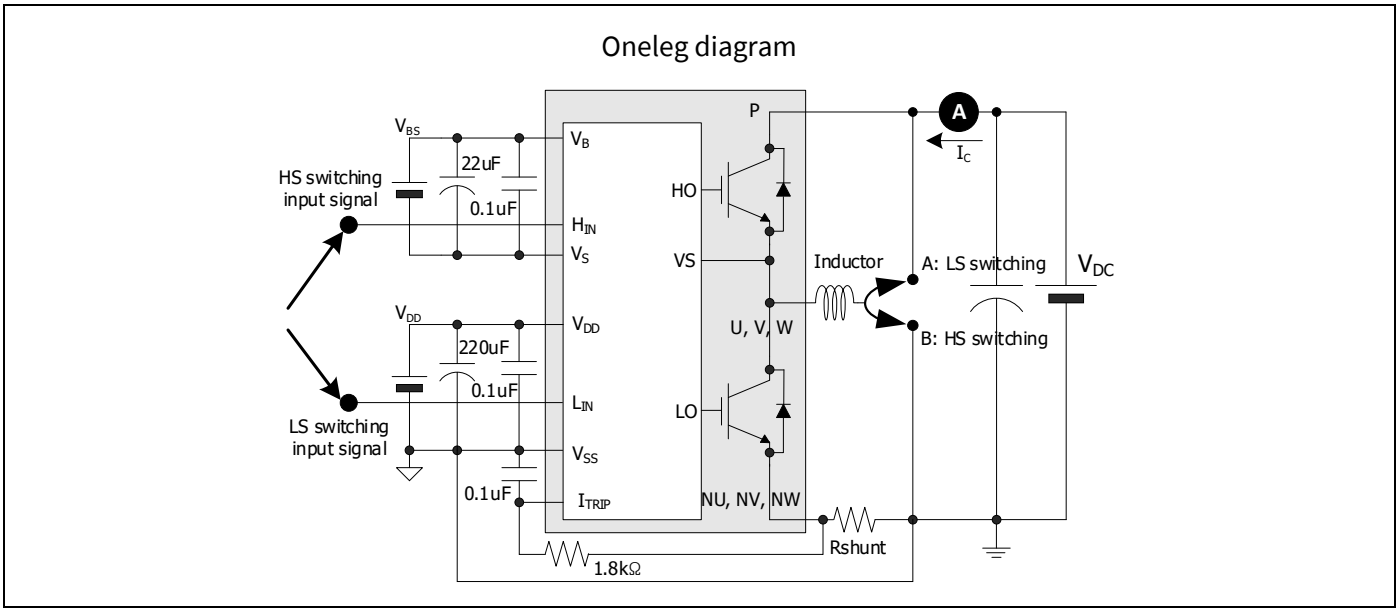


Figure 9 Switching test circuit

11.4 Switching time definition

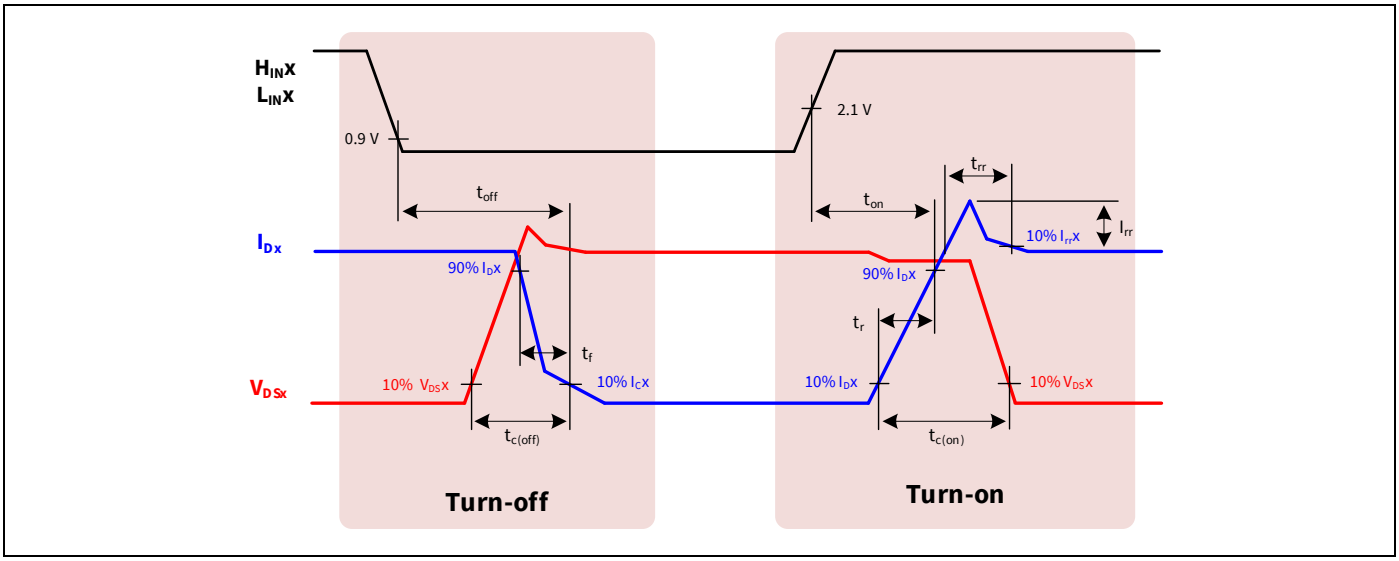


Figure 10 Switching time definition

12 Application guide

12.1 Typical application schematic

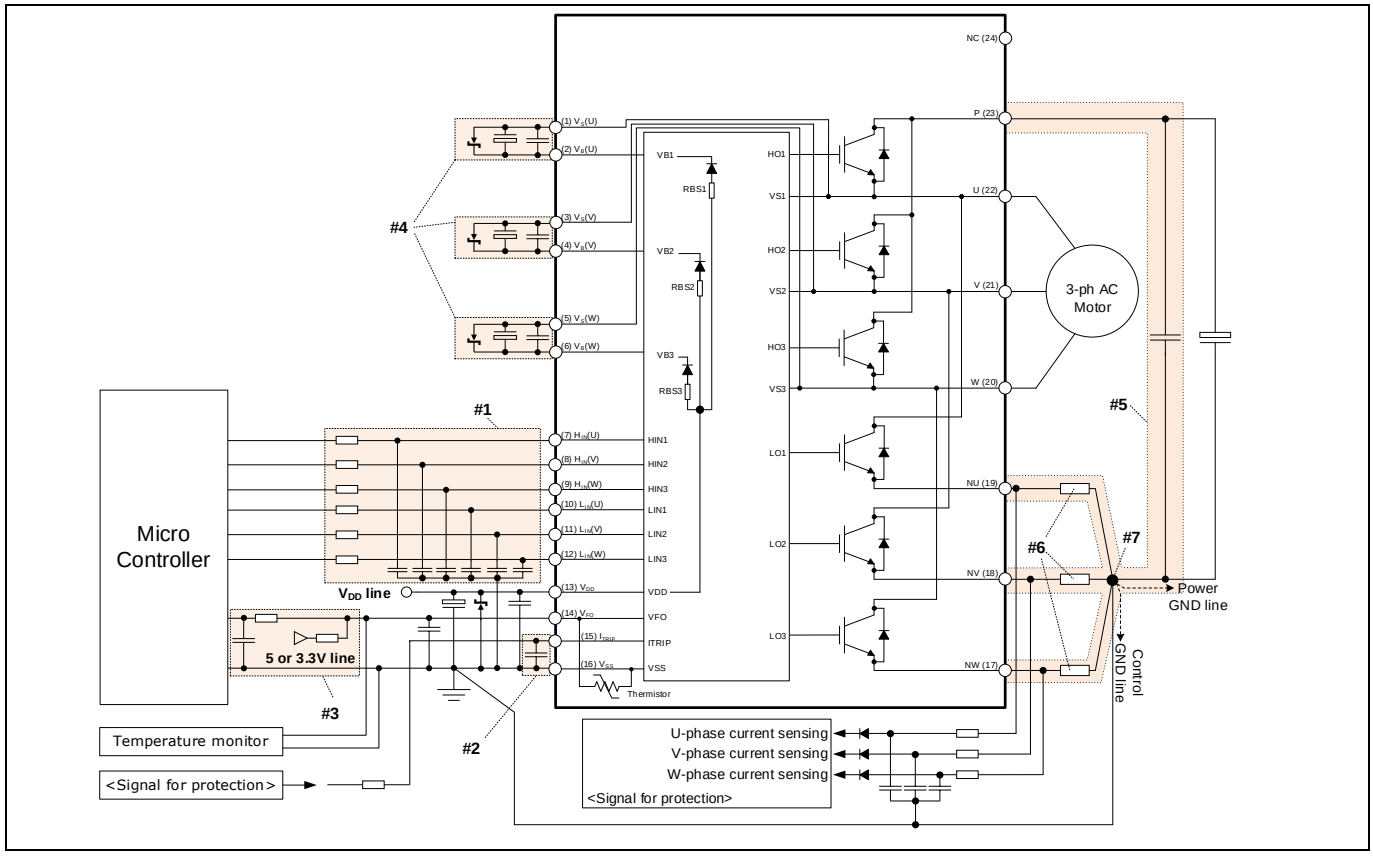


Figure 11 Typical application circuit

- #1 Input circuit
  - RC filter circuit can be used to reduce input signal noise (e.g. 100 Ω, 1 nF).
  - The filter capacitors should be placed close to the IPM (to V_{SS} pin especially).
- #2 I_{TRIP} circuit
  - To prevent protection function errors, RC filter (1.5~ 2.0 µs, e.g. 68 Ω, 22 nF) circuit is recommended.
  - The filter capacitor should be placed close to I_{TRIP} and V_{SS} pins.
- #3 V_{FO} circuit
  - V_{FO} pin is an open-drain output. This signal line should be pulled up to the bias voltage of the 5 V/3.3 V with a proper resistor.
  - It is recommended that RC filter circuit is placed close to the controller.
- #4 V_B-V_S circuit
  - Capacitors for high-side floating supply voltage should be placed close to V_B and V_S pins.
- #5 Snubber capacitor
  - The wiring among the IPM, snubber capacitor and shunt resistors should be short as possible.
- #6 Shunt resistor
  - SMD-type resistors are strongly recommended to minimize stray inductance.
- #7 Ground pattern
  - Power ground and signal ground should be connected at a single point. It is recommended to connect them at the end of shunt resistor.

12.2 Performance chart

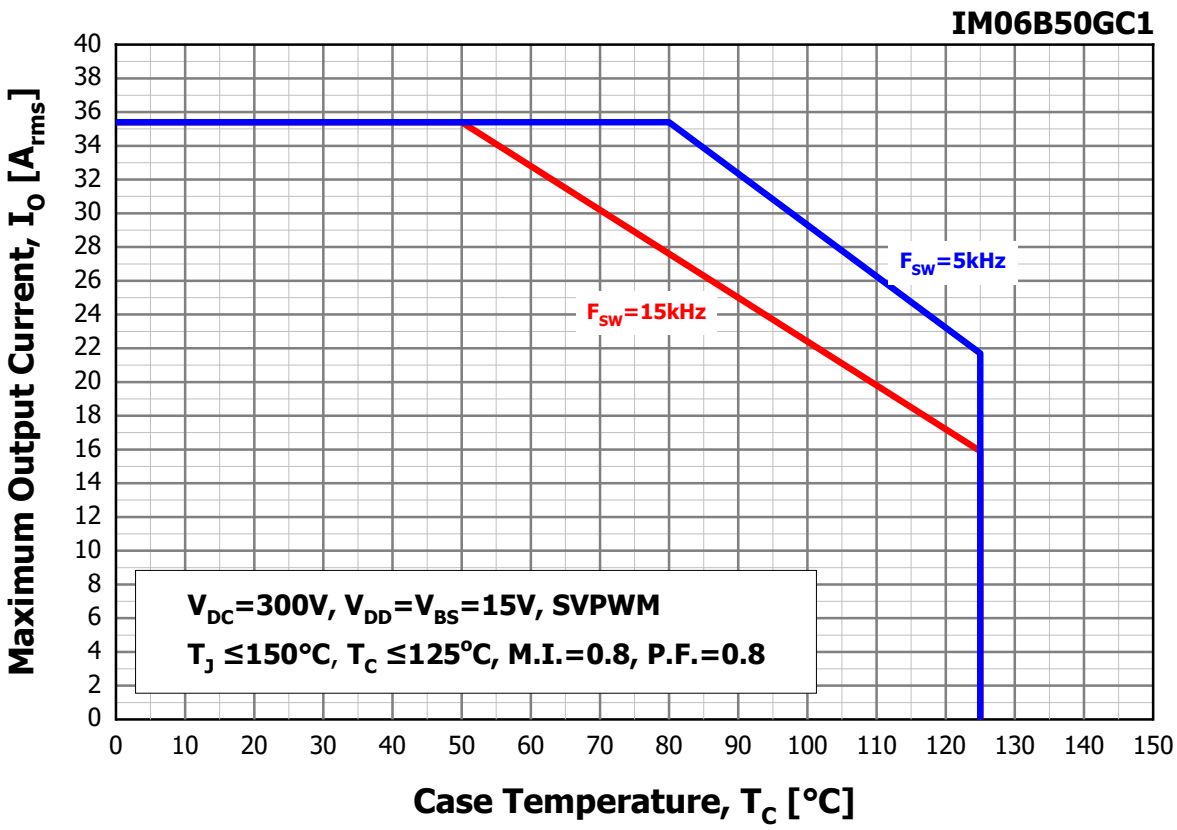


Figure 12 Maximum operating current SOA[1]

[1]This maximum operating current SOA is just one of example based on typical characteristics for this product. It can be changed by each user's actual operating conditions.

13 Package outline

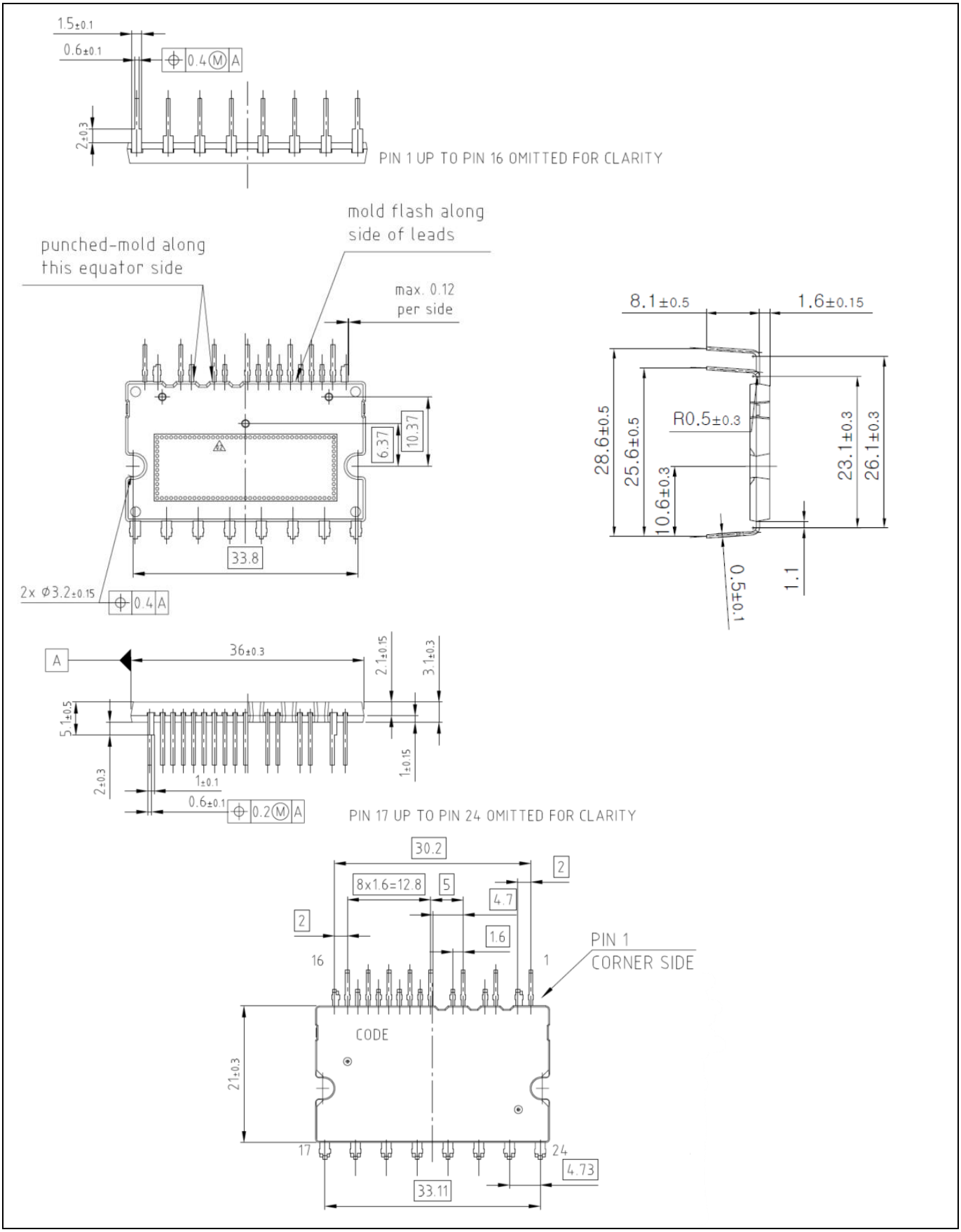


Figure 13 IM06B50GC1

Revision history

Document version	Date of release	Description of changes
1.00	2024-12-10	Initial release
1.10	2025-02-28	Updated UL number and Figure 13 (package outline)

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