MD070SD 7” Bus TFT Module Manual

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1, Description

Applicable CPU：51, AVR, STM32, PIC, MSP430, DSP, ARM, etc.

MD070SD adopts 8080 timing sequence with 16-bit parallel bus interface, resolution of 800 ×480, display panel with 16M color and integrated with 8-page video memory (the remaining memory could be used as extended memory). The interior of module utilizes CPLD + SDRAM mode to drive RGB interface display, which does not only realize conversion between the bus interface and RGB interface, but also provides a range of useful features. For details, please refer to the following register descriptions and Demo program.

With regard to stability, the module is equipped with great anti-interference capability, which is far more powerful than the drive solution SSD1963 on the market, as anti-interference ability of SSD1963 is poor with risk of crashing and white screen.

As to functions, the module provides 8-page video memory which can achieve data writing on the background, a command is enough to switch to full-screen display of data instantly, which is far more functional than drive solution RA8875on the market.

Concerning control, as MD070SD does not need to be initialized, and a resetting operation is enough to make it work, thus those boring initialization codes which general TFT controllers require can be saved. A minimum of five register commands will be enough to make it operate normally, which greatly simplifies the codes and reduces the difficulty of debugging and probability of error.

The control board responds very fast, which can achieve reading and writing cycle up to 200ns and the highest full-screen refreshing speed of 13 frames. The integrated 8MB SDRAM corresponds to 8-page display buffer. The display page register and reading and writing page register are set up independently, and the current display page and reading and writing page can be different pages to facilitate the achievement of full-page fast switching after being written on the background.

TFT drive timing sequence and circuit design have been optimized to ensure accurate color recovery, stable display, to eliminate flickering or cross colors, and to provide LED backlight drive thus brightness can be regulated from 0 (closed) to 16 (full).

2, Interface definition and mounting

Note: SD_ prefixed pins are for SPI interfaces for multiplexing between SD card socket and FLASH, and they can be disconnected if they are not in use. F_CS is for flash potential energy (flash chip is reserved and the factory default is not to be soldered). T_ prefixed pins are for the touch interfaces, and they can be disconnected if they are not in use.

3, Description of work register

Table 2: register list

CS	RS	DATA[15:0]	WR	RD	Function
0	0	0x0001	0	×	Address points to backlight brightness register
0	1	0-16	0	×	Backlight brightness value (default:0)
0	0	0x0002	0	×	Address points to beginning row address register
0	1	0-480	0	×	Write a 9-bit beginning row address
0	0	0x0003	0	×	Address points to beginning column address register
0	1	0-800	0	×	Write a 10-bit beginning column address
0	0	0x0006	0	×	Address points to ending row address register
0	1	0-800	0	×	Write a 9-bit ending row address
0	0	0x0007	0	×	Address points to ending column address register
0	1	0-800	0	×	Write a 10-bit ending column address
0	0	0x0004	0	×	Display page register
0	1	0-max. page N.O.	0	×	Write (set up) the page address (default as page 0 when powering up) of the displayed page
0	0	0x0005	0	×	Reading and writing page register
0	1	0-max. page N.O.	0	×	Write (set up) the current reading and writing page address (default as page 0 when powering up)
0	0	0x000B	0	×	Sleep mode register
0	1	0x0000-0x0001	0	×	0x0001-entering into sleep mode (Sleep mode can be quitted by sending out an arbitrary reading and writing command after entering into sleep mode)
0	0	0x000C	0	×	Display mode register
0	1	0x0000-0x000F	0	×	Bit0: U / D (up-down flip display) Bit1: L / R (left-right flip display) Bit [3:2]: 0 (normal display) Bit [3:2]: 2 (LCD screen self-test mode)
0	0	0x000D	0	×	Address points to address increment direction register
0	1	0x0000-0x0001	0	×	0x0000-row direction address auto increment (default) 0x0001- column direction address auto increment
0	0	0x000F	0	×	Address points to data channel
0	1	0x0000-0xFFFF	0	×	Write data to control board

0	0	0x0000-0x0001	1	0	Read RAM data from control board
1	×	×	×	×	Disabled

4, Work register configuration description

4.1 Backlight Control

Backlight is driven by 300Hz PWM signals with high energy conversion efficiency and no flicker. When the backlight register is set to 0, the backlight turns off. When the backlight register is powered up, the reset value is 0. To avoid blurred screen when powering up, you can clear the screen first when powering up, and then turn on the backlight. The maximum backlight value is 16 (0x10). When the writing value is greater than 16, it will be ignored.

4.2 Writing of row and column addresses

The corresponding RAM address of row and column addresses is obtained by internal arithmetic of the control board, thus users do not need to calculate the correspondence between the row and column addresses and the RAM address, and they can directly enter coordinates addresses.

4.3 Row and column address increment direction

Row and column address increment direction can be achieved by configuring "address increment direction register (0x0D)". The address is automatically incremented by 1 when writing continuously. The control board can be set as the row direction or the column direction address auto increment. When it comes to the end of the row, it will circulate to the beginning of the row.

4.4 Reading and writing data channel

When reading and writing display data, make sure that the work register value is set to 0x0F and selection points to data channel; when reading and writing display data, work register cannot be modified to other values, writing will be failed.

4.5 Resetting and initialization

After the drive board is powered up, RST pin will control resetting. Resetting of low level needs to keep for 1ms to ensure reliable resetting, internal initialization of module can only be done when the resetting pin is pulled to high level and lasts for 1ms, and then data can be written.

5, Color configuration description

Table 3：Color code list

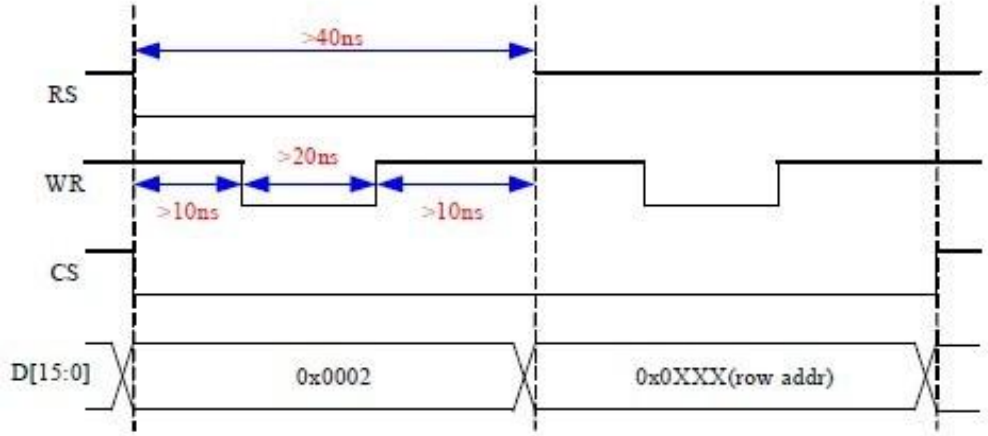
65k	R4	R3	R2	R1	R0	G5	G4	G3
	D15	D14	D13	D12	D11	D10	D9	D8
	G2	G1	G0	B4	B3	B2	B1	B0
	D7	D6	D5	D4	D3	D2	D1	D0

Table 4：Color code list - continued

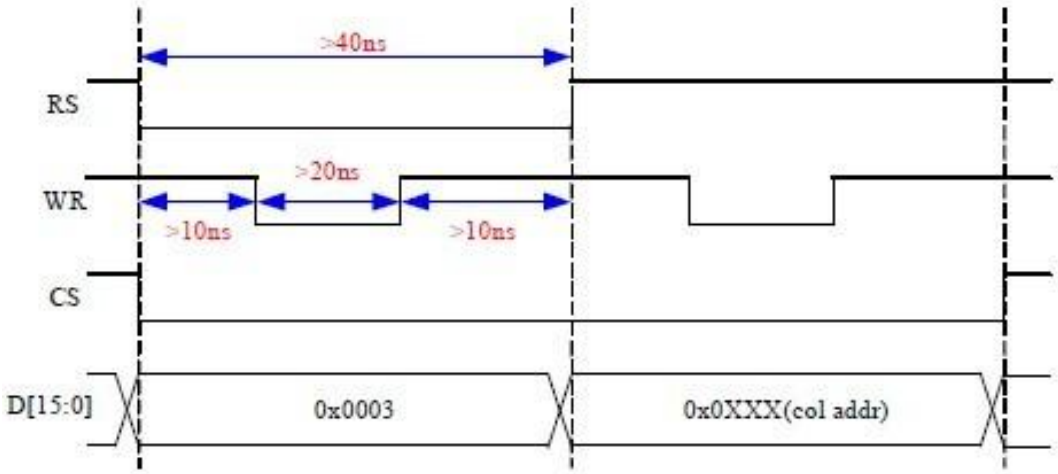
Basic color	Grayscale	R4、R3、R2	G5、G4、G3	B4、B3、B2
	Darkest	000	000	000
	Bright blue	000	000	111
	Bright green	000	111	000
	Bright cyan	000	111	111
	Bright red	111	000	000
	Bright purple	111	000	111
	Bright yellow	111	111	000
	Bright white	111	111	111
Blue grayscale	Darkest	000	000	000
	Darker	000	000	001
	…	…	…	…
	Brighter	000	000	110
	Brightest	000	000	111
Green grayscale	Darkest	000	000	000
	Darker	000	001	000
	…	…	…	…
	Brighter	000	110	000
	Brightest	000	111	000
Red grayscale	Darkest	000	000	000
	Darker	001	000	000
	…	…	…	…
	Brighter	110	000	000
	Brightest	111	000	000

6, Timing sequence description for reading and writing

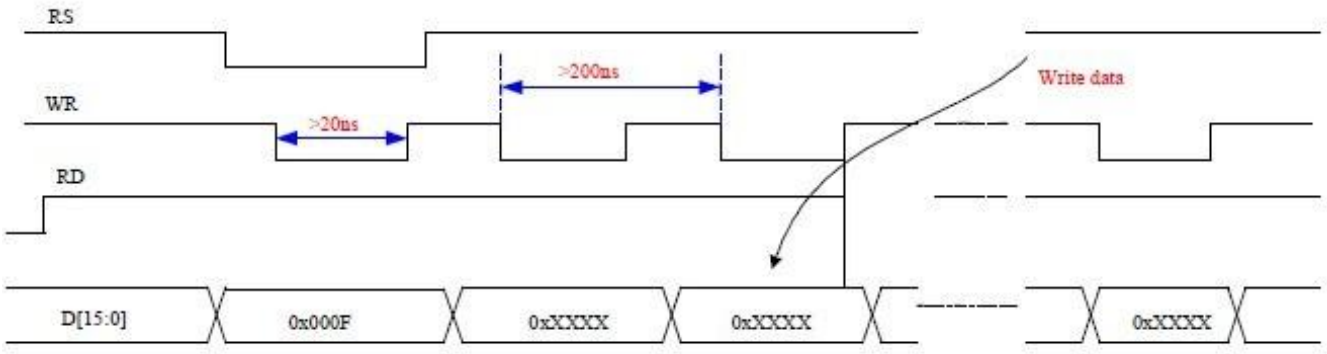
6.1 Timing sequence for writing row address



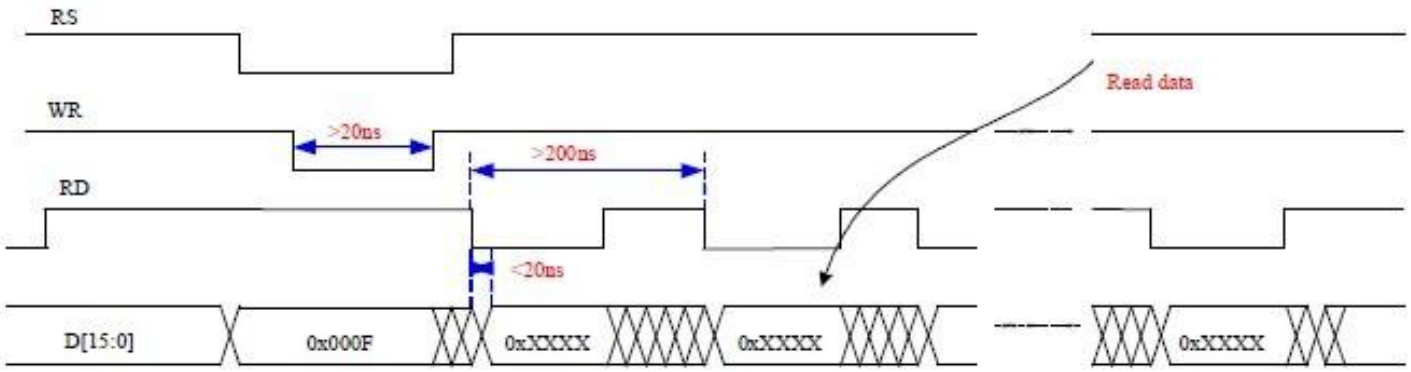
6.2 Timing sequence for writing column address



6.3 Timing sequence for writing display data



6.4 Timing sequence for reading display data



6.5 Timing sequence for writing other command registers

The method is the same with writing row and column addresses.

7, Demo for MCU drive program application

7.1 Demo code (8051)

```
//Set up beginning address and ending address
void Address_set(unsigned int x1,unsigned int y1,unsigned int
x2,unsigned int y2)
{
LCD_WR_REG(0x02);//begin y
LCD_WR_DATA(y1);
LCD_WR_REG(0x03);//begin x
LCD_WR_DATA(x1);
LCD_WR_REG(0x06);//stop y
LCD_WR_DATA(y2);
LCD_WR_REG(0x07);//stop x
LCD_WR_DATA(x2);
LCD_WR_REG(0x0f);
}
void Lcd_Init(void)
{
LCD_RD=1;
LCD_WR=1;
LCD_REST=0;
delayms(1); //here must be kept for more than 1ms
LCD_REST=1;
delayms(1); // here must be kept for more than 1ms
LCD_CS =0; //open chip selection enable
LCD_WR_REG(0x01); //turn on backlight
LCD_WR_DATA(16);
}
//Screen clear function
//Color: Fill color of the screen to be cleared
void LCD_Clear(u16 Color)
{
u8 VH,VL;
u16 i,j;
VH=Color>>8;
VL=Color;
Address_set(0,0,LCD_W-1,LCD_H-1);
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for(i=0;i<LCD_W;i++)
{
for (j=0;j<LCD_H;j++)
```

```
{
LCD_WR_DATA8(VH,VL);
}
}
}
```

If you do not use multi-page memory function, you can ignore operation of memory pages associated register as a normal TFT controller. The default operating page after powering up is page 0 and the display page is also page 0. If you are using a multi-page memory, you can set up the page by adding the following two functions:

```
void WritePage(unsigned char index)//set up the current operating page, the default is page 0 after powering up
{
LCD_WR_REG(0x05);
LCD_WR_DATA(index);
}
void ShowPage(unsigned char index)// set up the current display page, the default is page 0 after powering up
{
LCD_WR_REG(0x04);
LCD_WR_DATA(index);
}__
```