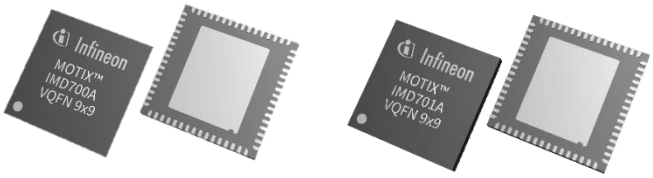
MOTIX™ IMD70xA

BLDC Integrated Controller and Smart 3 Phase Gate Driver



Datasheet

Product Feature Summary

General Features

- Fully programmable drives optimized ARM® Cortex-M0 microcontroller (XMC1404 @ 48MHz main clock) with additional MATH Co-processor (96MHz)
- 3 phase smart gate driver: 1.5A sink/ 1.5A source peak gate driver currents
- 3 current sense amplifiers with integrated gain and offset generation
- Integrated synchronous buck converter controller and LDO for complete BLDC system supply
- 5.5V to 60V operating voltage
- Supports trapezoidal commutation (6 or 12 steps) and FOC algorithms
- 20 GPIOs plus up to 12 analog inputs

ARM® Cortex-M0, 32 bits microcontroller (XMC1404)

- **CPU Subsystem**
  - 32 bit ARM® Cortex-M0 (core clock 48MHz)
  - MATH Co-Processor (96MHz) for optimized 32 bit division and 24 bit trigonometric calculations
  - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
  - Nested Vectored Interrupt Controller (NVIC) with 64 interrupt nodes
  - Internal slow and fast oscillators without the need of PLL
  - Real time clock module
  - Window watchdog
  - Up to 128kB of Flash (with ECC) and 16kB of RAM (with parity)
  - Internal oscillator
- **Serial Communication Modules**
  - Four USIC channels, each of them configurable as UART, SPI, IIC and more
  - MultiCAN module (2 CAN nodes)
- **Analog Frontend Peripherals**
  - 12 bit A/D Converters (up to 12 analog inputs), 2 sample and hold stages up to 1.1MSamples/s with adjustable gain
  - 4 fast, general purpose analog comparators
- **Industrial Control Peripherals**
  - 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
  - 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and 3 phase inverter control
  - 2x POSIF for Hall and quadrature encoders, motor positioning

- **On-Chip Debug Support**
  - 4 hardware breakpoints
  - ARM serial wire debug, single-pin debug interfaces
- **Programming Support**
  - Single-pin bootloader
  - Secure bootstrap loader SBSL (optional)

Three Phase Programmable Gate Driver

- 1.5A sink/ 1.5A source peak gate driver currents
- Programmable driving voltage (7V, 10V, 12V, 15V)
- Independently programmable high side/low side slew rate control
- 100% duty cycle

Integrated Power Supply System

- High efficiency synchronous buck converter with programmable switching frequency.
- Linear regulator (5V or 3.3V) with 300mA current capability supplying XMC1404 and other external components (DVDD)
- Dual charge pump for supplying gate driver even at low supply voltage

Three Current Sense Amplifiers

- Integrated adjustable gain and offset
- Flexible protection and behavior programming
- Configurable for low side R_{DSON} sensing

Protection features:

- Easy brake mode with programmable braking response
- Over-Current Protection (OCP) on current sense amplifiers (programmable)
- Over-Current Protection (OCP) for buck converter and DVDD linear regulator (programmable)
- Under-Voltage Lockouts (UVLO) for all internal/external supplies
- Over-Voltage Fault (OVLO) reporting for buck converter and DVDD linear regulator
- Over-Temperature warning and shutdown (OTW, OTS) in gate driver and microcontroller

Thermally enhanced 64pin VQFN package

Potential Applications

- Battery powered power tools and gardening tools
- Robotic lawn mowers
- E-bikes
- Robotics, RC toys, consumer drones and multi-copters
- Pumps and fans
- Other 3 Phase BLDC and PMSM motors

Product Description

MOTIX™ IMD70xA is a controller specifically designed for 3 phase BLDC or PMSM drives applications. IMD70xA integrates a fully programmable XMC1404 ARM® Cortex®-M0 microcontroller from Infineon XMC1400 family with 6EDL7141, a 60V three phase smart gate driver with integrated power supply. Both devices integrated allow an ultra-compact design for drives applications up to 60V including not only the microcontroller and a flexible 3 phase gate driver, but also the complete power supply required in the system (synchronous buck converter and LDO), 3 current sense amplifiers, protections and a remarkable set of configurations to adjust to specific needs.

XMC1404, ARM® Cortex®-M0 based microcontroller, incorporates dedicated features to improve motor drives control. Features like the MATH Co-Processor, a hardware unit clocked at 96MHz, enhances the calculation of divisions and trigonometric functions like ‘Arctan’, commonly used in Field Oriented Control of PMSM. Additionally, XMC1404 inherits most of the high end peripherals found in XMC4000 family (ARM® Cortex®-M4), like PWM timers-CCU8 and CCU4-, Position interface (POSIF) or serial communication modules including CAN, ensuring best in class control.

With up to 20 dedicated general purpose pins and up to 12 analog inputs, the user has full flexibility to implement specific functions externally like serial communications, security or safety related functions or auxiliary functions like LEDs, buttons or displays.

Internally, XMC1404 and 6EDL7141 are connected to ensure proper operation. These interconnects enable SPI communication between both devices for configurability and status reporting of 6EDL7141, 6 PWM signals for driving the motor, nFAULT reporting pin to inform the microcontroller of any possible fault on the power side, an enable driver pin, and a brake pin that can be also accessed externally for a double brake path.

6EDL7141 smart gate driver provides on the one side a flexible gate driving scheme and on the other side the necessary robustness and protection features to avoid failures in demanding drives systems. The gate driver outputs are placed strategically to allow best layout practices in power circuits.

In 6EDL7141, separate charge pumps for low and high side gate drivers support 100% duty cycle and low voltage supply operation. Supplies for the gate drivers are programmable to one of the following levels: 7V, 10V, 12V or 15V. Additionally, the slew rate of the driving signal can be programmed with fine granularity to reduce EMI emissions.

An integrated synchronous buck converter provides an efficient supply of current to the rest of the system. However, drives systems require high precision current measurements, involving a very precise ADC reference voltage. For that purpose, 6EDL7141 uses a linear voltage regulator (up to 300mA), powered by the buck converter to supply XMC1404 and other components in the system. With this advanced power supply architecture, not only the best possible signal quality is achieved, but also the power efficiency is optimized at any input voltage.

6EDL7141 also integrates three current sense amplifiers for accurate current measurements that support bi-directional low side current sensing with programmable gain. R_{DSON} sensing is supported through internal connection of the phase nodes to the current sense amplifiers inputs. Low noise, low settling times and high accuracy are the main features of the integrated operational amplifiers. An internal buffer can be used to offset the sense amplifier outputs for optimizing the dynamic range. The outputs of the current sense amplifiers can be connected to ADC inputs in XMC1404 for accurate current sensing. Additional signal conditioning is therefore possible with external RC filter. The ADC can on top provide a gain factor that can be combined with the amplifiers one for best performance.

The device provides numerous protection features for improving application robustness during adverse conditions, like monitoring of power supply voltages as well as system parameters. The failure behavior, threshold voltages and filter times of the supervisions of the device are adjustable via SPI. Monitored aspects include motor currents, gate drive voltages and currents and device temperature. When a fault occurs, the

device stops driving and pulls nFAULT pin low, in order to prevent MOSFET damage and motor overheating. Those signals are connected internally to XMC1404 to inform the processor that a fault has happened. The microcontroller can request more information on the fault via SPI commands.

In order to increase robustness in drives applications, inverter, motor and supply related pins in IMD70xA can withstand voltages of up to 90V. Motor related pins can even withstand negative voltage transients down to -8V without compromising functionality allowing faster switching of the inverter MOSFETs, therefore reducing switching losses.

System Block Diagram

Figure 1 shows a simplified system block diagram where MOTIX™ IMD70xA is used as 3-phase BLDC controller Hall-sensored BLDC motor control system.

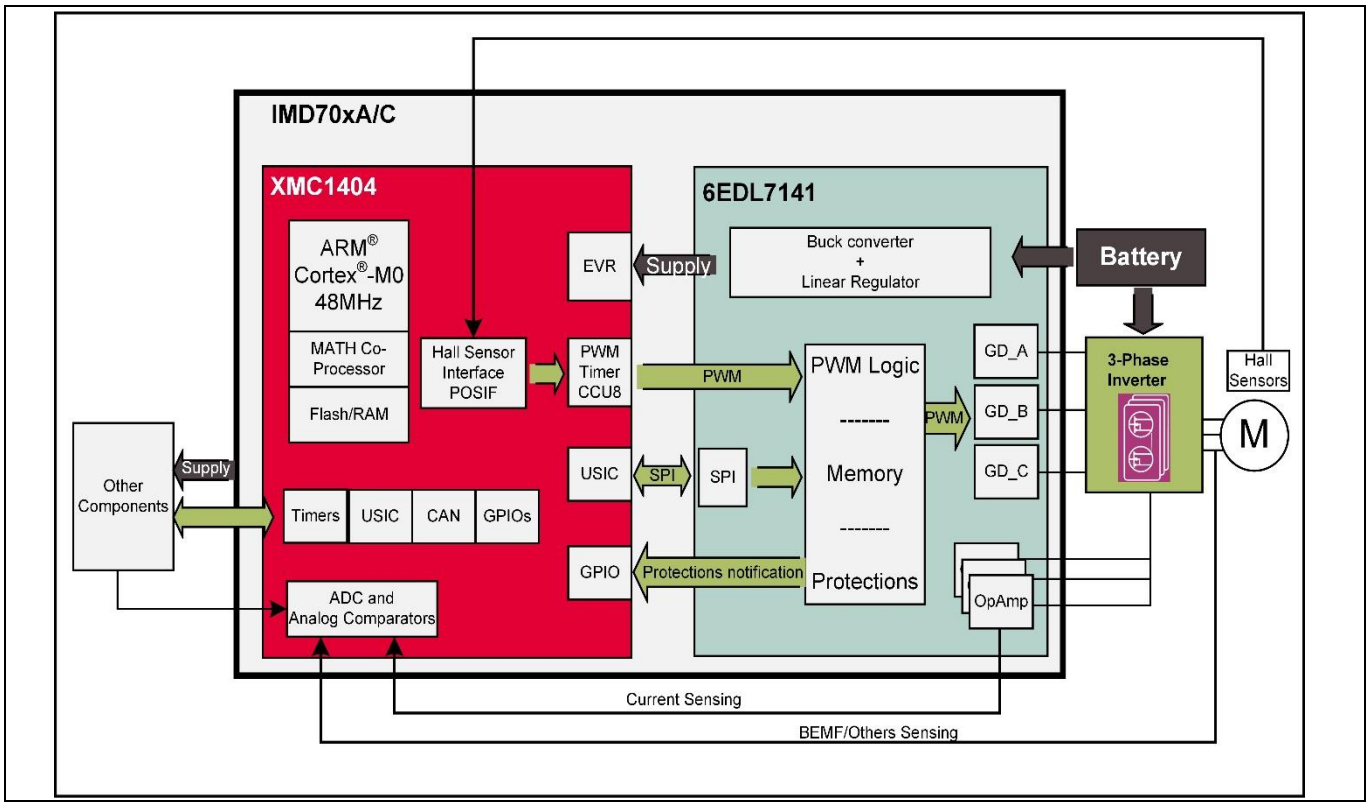


Figure 1 Simplified System Block Diagram

Package Description

MOTIX™ IMD70xA is integrated in a VQFN64 9mm x 9mm package with an exposed pad. The device and package information is shown in Table 1.

Table 1 Device and package information

Part Number	Package	Body Size	Lead Pitch
IMD700A	PG-VQFN-64-8	9.0 mm × 9.0 mm	0.5 mm
IMD701A	PG-VQFN-64-8	9.0 mm × 9.0 mm	0.5 mm

Note: Refer to XMC1400 Reference Manual for full description of the device including registers and interconnects. Latest version can be found at Infineon website (www.infineon.com)

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1 Pin Configuration

1.1 Pin Assignment

In Figure 2, the pinout of MOTIX™ IMD70xA is presented.

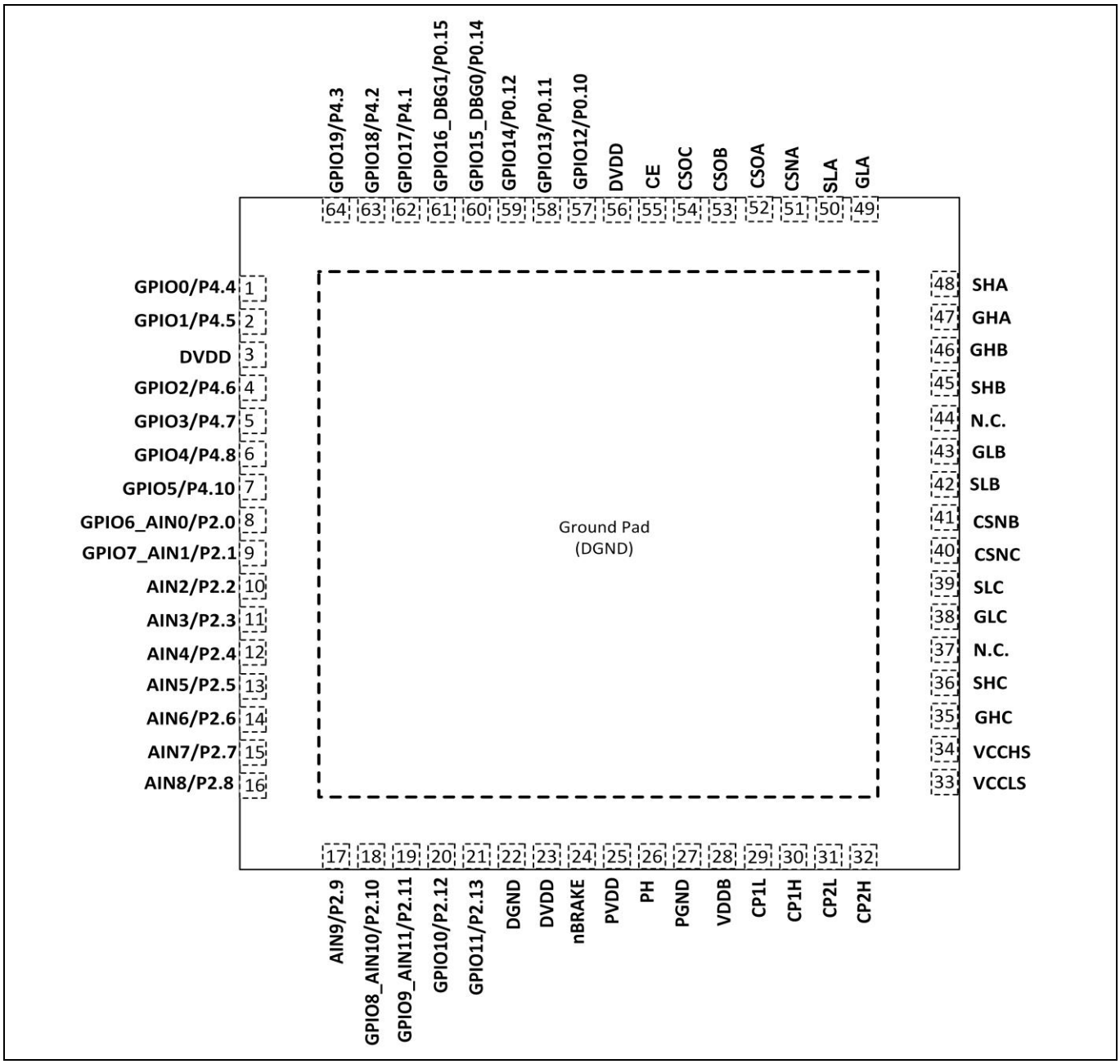

Figure 2 Pin configuration

1.2 Pin Definition and Functions

Details regarding the pins of IMD70xA are shown in Table 1.

I: Input, O: output, IO: Input and/or Output, D: Digital, A: Analog, AD: Analog and/or Digital, P: Power, G: Ground.

Table 1 Pin Definition

Pin #	Pin Name	XMC Port	IO	Type	Description
1	GPIO0/ P4.4	P4.4	IO	D -(STD_INOUT)	General purpose digital I/O. Standard bi-directional pads
2	GPIO1/ P4.5	P4.5	IO	D -(STD_INOUT)	General purpose digital I/O. standard bi-directional pads
3	DVDD	VDD/ VDDP	IO	P	Microcontroller voltage supply. DVDD is generated from DVDD linear regulator in 6EDL7141 (pin 23 and 56) and must be connected to all DVDD pins. This voltage can be used to supply external components as well. Connect a capacitor to DGND in every DVDD pin.
4	GPIO2/ P4.6	P4.6	IO	D -(STD_INOUT)	General purpose digital I/O
5	GPIO3/ P4.7	P4.7	IO	D -(STD_INOUT)	General purpose digital I/O
6	GPIO4/ P4.8	P4.8	IO	D -(STD_INOUT)	General purpose digital I/O
7	GPIO5/ P4.10	P4.10	IO	D -(STD_INOUT)	General purpose digital I/O
8	GPIO6_AIN0/P2.0	P2.0	I	A/D -(STD_INOUT/AN)	Analog input
9	GPIO7_AIN1/P2.1	P2.1	I	A/D -(STD_INOUT/AN)	Analog input
10	AIN2/P2.2	P2.2	I	A - (STD_IN/AN)	Analog input
11	AIN3/P2.3	P2.3	I	A - (STD_IN/AN)	Analog input
12	AIN4/P2.4	P2.4	I	A - (STD_IN/AN)	Analog input
13	AIN5/P2.5	P2.5	I	A - (STD_IN/AN)	Analog input
14	AIN6/P2.6	P2.6	I	A - (STD_IN/AN)	Analog input
15	AIN7/P2.7	P2.7	I	A - (STD_IN/AN)	Analog input
16	AIN8/P2.8	P2.8	I	A - (STD_IN/AN)	Analog input
17	AIN9/P2.9	P2.9	I	A - (STD_IN/AN)	Analog input
18	GPIO8_AIN10/P2.10	P2.10	IO	A/D -(STD_INOUT/AN)	Dual functionality pin. Analog input and general purpose digital I/O

Pin Configuration

Pin #	Pin Name	XMC Port	IO	Type	Description
19	GPIO9_AIN11/P2.11	P2.11	IO	A/D - (STD_INOUT/AN)	Dual functionality pin. Analog input and general purpose digital I/O
20	GPIO10/P2.12	P2.12	IO	A/D - (STD_INOUT/AN)	General purpose digital I/O
21	GPIO11/P2.13	P2.13	IO	A/D - (STD_INOUT/AN)	General purpose digital I/O
22	DGND	VSS/ VSSP		P	Ground connection for digital section. Supply GND, ADC reference GND
23	DVDD	VDD/ VDDP	IO	P	Microcontroller voltage supply. DVDD is generated from DVDD linear regulator in 6EDL7141 (pin 23 and 56) and must be connected to all DVDD pins. This voltage can be used to supply external components as well. Connect a capacitor to DGND in every DVDD pin.
24	nBRAKE	P1.3[1)]	I	D (High Current)	After start-up, pin is used for motor braking. Active low
25	PVDD	-		P	Power supply of the device
26	PH	-	O	P	Buck phase node voltage. Connect to output inductor
27	PGND	-	-	G	Power ground used for buck converter, charge pumps and gate drivers
28	VDDB	-	-	P	Buck output voltage. Connect capacitor between VDDB and PGND.
29	CP1L	-	-	P	Bottom connection of the charge pump flying capacitor 1
30	CP1H	-	-	P	Top connection of the charge pump flying capacitor 1
31	CP2L	-	-	P	Bottom connection of the charge pump flying capacitor 2
32	CP2H	-	-	P	Top connection of the charge pump flying capacitor 2
33	VCCLS	-	-	P	Output of low side charge pump. Connect a capacitor from VCCLS to PGND.
34	VCCHS	-	-	P	Output of high side charge pump. Connect a capacitor from VCCHS to PVDD or PGND.
35	GHC	-	O	A	High side gate driving signal for phase C. Not connected or connected to PVDD if not used
36	SHC	-	IO	A	High side source connection (phase node) for phase C. Positive input of shunt amplifier C for R_{DSON} sensing. Not connected if not used
37	N.C.	-			Not connected

Pin Configuration

Pin #	Pin Name	XMC Port	IO	Type	Description
38	GLC	-	O	A	Low side gate driving signal for phase C. Not connected if not used
39	SLC	-	IO	A	Low side source connection for phase C. Positive input of shunt amplifier C for shunt sensing. Short to PGND if not used
40	CSNC	-	I	A	Current sense amplifier negative input for phase C. Short to PGND or DGND if not used
41	CSNB	-	I	A	Current sense amplifier negative input for phase B. Short to PGND or DGND if not used
42	SLB	-	IO	A	Low side source connection for phase B. Positive input of shunt amplifier B for shunt sensing. Short to PGND if not used
43	GLB	-	O	A	Low side gate driving signal for phase B. Not connected if not used
44	N.C.	-			Not connected
45	SHB	-	IO	A	High side source connection (phase node) for phase B. Positive input of shunt amplifier B for R_{DSON} sensing. Not connected if not used
46	GHB	-	O	A	High side gate driving signal for phase B. Not connected or connected to PVDD if not used
47	GHA	-	O	A	High side gate driving signal for phase A. Not connected or connected to PVDD if not used
48	SHA	-	IO	A	High side source connection (phase node) for phase A. Positive input of shunt amplifier A for R_{DSON} sensing. Not connected if not used
49	GLA	-	O	A	Low side gate driving signal for phase A. Not connected if not used
50	SLA	-	IO	A	Low side source connection for phase A. Positive input of shunt amplifier B for shunt sensing. Short to PGND if not used
51	CSNA	-	I	A	Current sense amplifier negative input for phase A. Short to PGND or DGND if not used
52	CSOA	-	O	A	Current sense amplifier output for phase A. Not connected if not used
53	CSOB	-	O	A	Current sense amplifier output for phase B. Not connected if not used
54	CSOC	-	O	A	Current sense amplifier output for phase C. Not connected if not used
55	CE	-	I	D	Chip Enable. Starts up the device upon rising edge
56	DVDD	VDD/ VDDP	-	P	Microcontroller voltage supply. DVDD is generated from DVDD linear regulator in 6EDL7141 (pins 23 and

Pin Configuration

Pin #	Pin Name	XMC Port	IO	Type	Description
					56) and must be connected to all DVDD pins. This voltage can be used to supply external components as well. Connect a capacitor to DGND in every DVDD pin. XCM1404 I/O port supply
57	GPIO12/P0.10	P0.10	IO	D -(STD_INOUT/clock_IN)	General purpose digital I/O. Can be used as high precision crystal/oscillator input
58	GPIO13/P0.11	P0.11	IO	D -(STD_INOUT/clock_O)	General purpose digital I/O. Can be used as high precision crystal/oscillator input
59	GPIO14/P0.12	P0.12	IO	D -(STD_INOUT)	General purpose digital I/O
60	GPIO15_DBG0/P0.14	P0.14	IO	D -(STD_INOUT)	General purpose digital I/O. This is SWD pin for microcontroller debug I/F
61	GPIO16_DBG1/P0.15	P0.15	IO	D -(STD_INOUT)	General purpose digital I/O. This is SWCLK pin for microcontroller debug I/F
62	GPIO17/P4.1	P4.1	IO	D -(STD_INOUT)	General purpose digital I/O. Can be used as Hall sensor input for POSIF module
63	GPIO18/P4.2	P4.2	IO	D -(STD_INOUT)	General purpose digital I/O. Can be used as Hall sensor input for POSIF module
64	GPIO19/P4.3	P4.3	IO	D -(STD_INOUT)	General purpose digital I/O. Can be used as Hall sensor input for POSIF module
ePad	DGND	VSS	-	G	Ground connection for digital section. Solder to PCB. Exposed Die Pad The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground

1. *Dual path for braking: internal connection of P1.3 through gate driver die*

1.3 Interconnects Pin Description

Table 2 shows a list of details of the interconnected pins between XMC1404 controller and 6EDL7141

Table 2 Interconnects between devices

XMC Port Pin	XMC Pad Type	6EDL7141 Pin	6EDL7141 Pin Description
P0.7	STD_INOUT (standard bi-directional pads)	EN_DRV	Input digital. Enables the gate driver section and internal circuitry based on the configuration. Internal pull-down.
P0.4	STD_INOUT (standard bi-directional pads)	nSCS	Input digital. Active low. Chip select for SPI communication
P0.3	STD_INOUT (standard bi-directional pads)	SCLK	Input digital. Internal pull down. SPI Clock signal from XMC (master)
P0.1	STD_INOUT (standard bi-directional pads)	SDO	Output digital. Internal pull down. SPI data input for XMC (master)
P0.0	STD_INOUT (standard bi-directional pads)	SDI	Input digital. Internal pull down. SPI data output for XMC (master)
P3.4	STD_INOUT (standard bi-directional pads)	nFAULT	Output digital. When low indicates a fault in 6EDL7141. Active low
P3.3	STD_INOUT (standard bi-directional pads)	INHA	Input digital. PWM input high side phase A. Internal pull down
P3.2	STD_INOUT (standard bi-directional pads)	INLA	Input digital. PWM input low side phase A. Internal pull down
P3.1	STD_INOUT (standard bi-directional pads)	INHB	Input digital. PWM input high side phase B. Internal pull down
P3.0	STD_INOUT (standard bi-directional pads)	INLB	Input digital. PWM input low side phase B. Internal pull down
P1.0	High Current (high current bi-directional pads)	INHC	Input digital. PWM input high side phase C. Internal pull down
P1.1	High Current (high current bi-directional pads)	INLC	Input digital. PWM input low side phase C. Internal pull down
P1.2	High Current (high current bi-directional pads)	AZ	Controller can use this pin to control Auto-Zero function.
P1.3 [1)]	High Current (high current bi-directional pads)	nBRAKE	Input digital. Active low. Used for motor braking function in 6EDL7141. Pull up required via XMC P1.3

1. *Dual path for braking: external connection of IMD70xA via pin 24*

1.4 Interconnects Block Diagram

A block diagram showing the interconnection between XMC1404 and 6EDL7141 is given in Figure 3

Pin Configuration

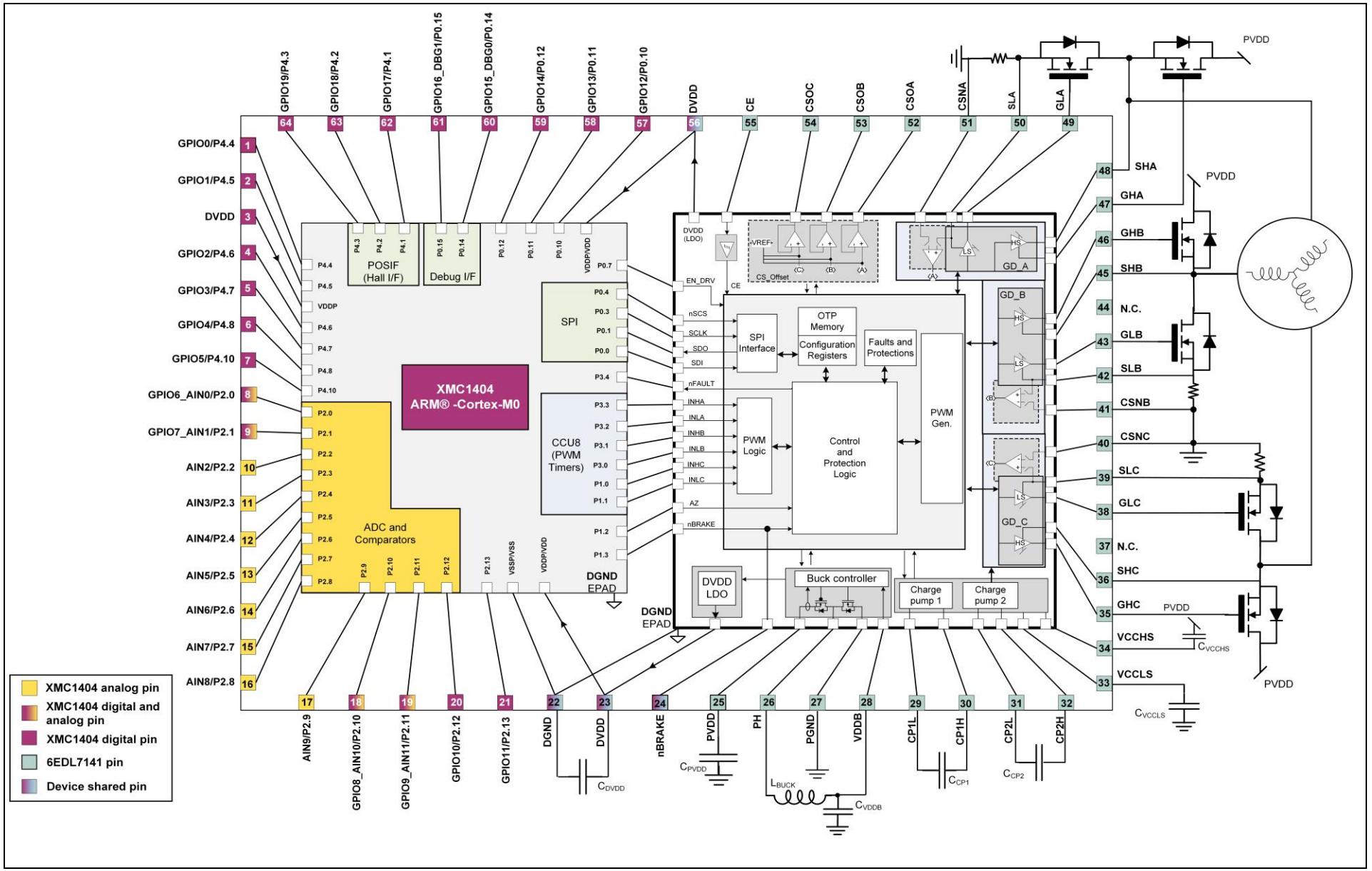

Figure 3 IMD70xA Interconnects block diagram

2 General Product Characteristics

2.1 Device Overview

Table 3 shows the XMC1404 configuration regarding peripherals, core and memory.

Table 3 XMC1404 Feature Overview

Features	IMD700A-Q064x0128	IMD701A-Q064x0128
Controller supply voltage	**3.3V**	**5V**
CPU Clock Frequency	48 MHz	48 MHz
Flash size (Kbytes)	128	128
SRAM size (Kbytes)	16	16
MATH co-processor	1	1
Auxiliary Timers (CCU4 units/timers/outputs)	2/8/8	2/8/8
PWM Timers (CCU8 units/timers/outputs)	2/8/32[1)]	2/8/32[1)]
Hall Sensor/Encoder Interface (POSIF units)	2	2
Serial Communication (channels)	4	4
MultiCAN+ (nodes/MOs)	2/32	2/32
ADC (kernels/inputs)	2/12	2/12
Analog Comparators	4	4
BCCU (units)	1	1
LEDTS (units)	3	3

1. *Depending on pin availability. See Table 13 for possible pin functionality*

2.2 Absolute Maximum Ratings

Table 4 shows the absolute maximum ratings for the device. Ratings are intended in the temperature range T_j=-40°C to T_j=115°C. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), positive currents are flowing into the pin (unless otherwise specified).

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Supply voltage	PVDD	-0.3		70	V	
Supply voltage slew rate	SR_{PVDD}			2	V/µs	During start-up
				0.25		During active mode
CE pin voltage	V_{CE}	-0.3		7	V	
Power ground to digital ground voltage	PGND – DGND	-0.3		0.3	V	

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Low side gate driver supply voltage	VCCLS	-0.3		16.5	V	This is same as PVCC
VCCHS voltage	VCCHS	PVDD-0.3		86.5	V	VCCHS = PVDD + PVCC
VCCHS-V_{SHx} voltage	VCCHS-V_{SHx}			86.5	V	
VCCHS-V_{GHx} voltage	VCCHS-V_{GHx}			86.5	V	
Source high side voltage	V_{SHx}	-8		70	V	DC voltage
		-10		70		500ns pulse max
Source low side voltage/Shunt amplifier positive input voltage	V_{SLx}	-8		8	V	DC voltage
		-10		8		500ns pulse max
Gate high side voltage	V_{GHx}	-8		VCCHS+0.3	V	DC voltage,
		-10		VCCHS+0.3		500ns pulse max,
Gate low side voltage	V_{GLx}	-8		VCCLS+0.3	V	DC voltage
		-10		VCCLS+0.3		500ns pulse max
Gate to Source high side voltage	V_{GHx} - V_{SHx}	-0.3		16	V	DC, T_j = 25 °C
		-2		16		500ns pulse max, T_j = 25 °C
Gate to Source low side voltage	V_{GLx} - V_{SLx}	-0.3		16	V	DC, T_j = 25 °C
		-2		16		500ns pulse max, T_j = 25 °C
Shunt amplifier negative input voltage	V_{CSN}	-0.3		DVDD+0.3		
Flying capacitor 1 voltage	V_{CP1H} - V_{CP1L},	-0.3		9	V	
CP1L pin voltage	V_{CP1L}	-0.3		9	V	
CP1H pin voltage	V_{CP1H}	-0.3		16.5	V	
Flying capacitor 2 voltage	V_{CP2H} - V_{CP2L}	-0.3		70	V	
CP2L pin voltage	V_{CP2L}	-0.3		16.5	V	
CP2H pin voltage	V_{CP2H}	-0.3		86.5	V	
Buck converter output voltage	VDDB	-0.3		9	V	
Buck converter phase voltage continuous	V_{PH}	-0.3		70	V	DC condition
		-5			V	Less than 20 ns pulse
DVDD regulator output voltage	DVDD	-0.3		6	V	
Current sense amplifier output voltage	V_{CSOx}	-0.3		DVDD + 0.3	V	

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Maximum current for 6EDL7141 digital pins	$I_{DIG\_IN\_MAX}$	-1		1	mA	
Maximum current for 6EDL7141 analog inputs	$I_{AN\_IN\_MAX}$	-1		10	mA	
Voltage on GPIOx digital pins with respect to DGND)	V_{GPIO_INx}	-0.5	–	DVDD + 0.5 or max. 6	V	Whichever is lower
Voltage on AINx [1] XMC1404 Port 2 pins with respect to DGND	V_{AINx}	-0.3	–	DVDD + 0.3	V	–
Voltage on other AINx XMC1404 pins [2] with respect to DGND	V_{AINx}	-0.5	–	DVDD + 0.5 or max. 6	V	Whichever is lower
Input current on GPIOx/AINx pin during overload condition	$I_{GPIO/AIN}$	-10	–	10	mA	
Absolute maximum sum of all input currents in GPIOx/ADC_INx pins during overload condition	$I_{GPIO/AIN}$	-50	–	+50	mA	
Maximum current for GPIOx digital pins	$I_{GPIO\_DIG\_IN\_MAX}$	-1		1	mA	
Maximum current for XMC1404 analog inputs (AINx)	$I_{AN\_IN\_MAX}$	-1		10	mA	
Junction temperature range	T_J	-40		115	°C	
Storage temperature range	T_S	-55		125	°C	
Case temperature	T_{CASE}			145	°C	

1. *Excluding port pins P2.[1,2,6,7,8,9,11].*
2. *Applicable to port pins P2.[1,2,6,7,8,9,11].*

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.

Note: Absolute Maximum Ratings are not subject to production test, specified by design.

2.3 Recommended Operating Conditions

Operating at T_A = 25 °C. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), positive currents are flowing into the pin (unless otherwise specified).

Values are design targets to be confirmed after silicon characterization.

Table 5 Recommended operating conditions

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Supply voltage	PVDD	5.5		60	V	
Supply voltage slew rate	SR_{PVDD}			2	V/µs	During start-up
				0.25		During active mode
CE pin voltage range	V_{CE}	0		6	V	
External supply voltage regulator output voltage	DVDD			5.5	V	
Buck phase voltage continuous	V_{PH}	-0.3		60	V	DC condition
		-5				Less than 20 ns pulse
Inverter phase voltage	V_{SHx}	-8		60		
High side gate driver supply voltage	VCCHS	-0.3		75	V	
Gate driver supply voltage (PVCC)	VCCLS, VCCHS-PVDD	7		15	V	Programmable via SPI. This value is equal to PVCC
Gate driver maximum operating frequency	f_{PWM_GD}			200	kHz	
Shunt amplifier input voltage range	V_{SLx}, V_{CSNx}	-0.3		0.3	V	Sense amplifier configured for shunt resistor sensing
Current sense amplifier output pins voltage range	V_{CSOx}	0		DVDD	V	
Digital GPIOx or AIN pin voltage range	$V_{GPIOX/AINx}$	-0.3		DVDD	V	
Short circuit current of all XMC digital outputs	I_{SC}	-5		5	mA	
Absolute sum of short circuit currents of the XMC device	$\sum I_{SC\_D}$			25	mA	
Junction temperature range	T_J	-40		115	°C	

2.3.1 XMC Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 6 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- Full operation life-time is not exceeded
- Operating Conditions are met for
    - pad supply levels (DVDD)
    - temperature

If an XMC pin current is outside of the Recommended Operating Conditions but within the overload conditions, then the parameters of this pin as stated in the Recommended Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 6 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any XMC port pin during overload condition	I_{OV}	-5	–	5	mA	
Absolute sum of all XMC input circuit currents during overload condition	I_{OVS}	–	–	25	mA	

Figure 4 shows the path of the input currents during overload via the ESD protection structures. The diodes against DVDD and ground are a simplified representation of these ESD protection structures.

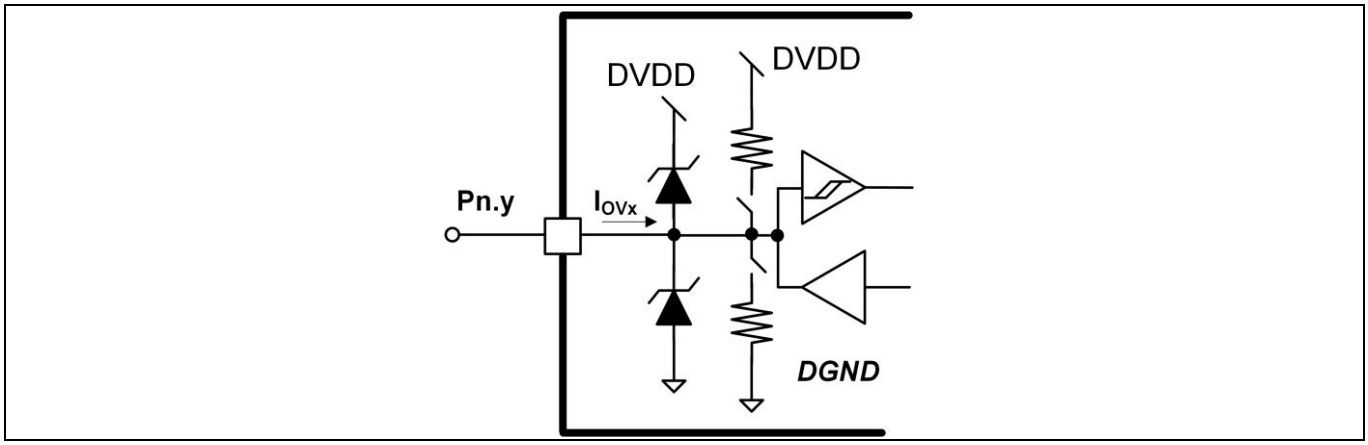

Figure 4 XMC1404 Input Overload Current via ESD structures

Table 7 and Table 8 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute Maximum Ratings must not be exceeded during overload.

Table 7 PN-Junction Characteristics for Positive Overload for XMC1404 pins

Pad Type	I_{OV}=5mA
Standard, High-current, AINx/DIG_IN	$V_{IN} = V_{DVDD} + 0.5V$ $V_{AINx} = V_{DVDD} + 0.5V$ $V_{AREF} = V_{DVDD} + 0.5V$ – XMC1404 analog reference
P2.[1,2,6:9,11]	$V_{AIN\_P2} = V_{DVDD} + 0.3V$

Table 8 PN-Junction Characteristics for Negative Overload for XMC1404 pins

Pad Type	I_{OV}=5mA
Standard, High-current, AINx/DIG_IN	$V_{IN} = V_{DGND} - 0.5V$ $V_{AINx} = V_{DGND} -0.5V$ $V_{AREF} = V_{DGND} -0.5V$ – XMC1404 analog reference
P2.[1,2,6:9,11]	$V_{AINP2} = V_{DGND} +0.3V$

2.4 ESD Robustness

ESD robustness related data is listed in Table 9.

Table 9 ESD robustness data[1)]

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
ESD robustness all pins	$\lvert V_{ESD\_HBM} \rvert$			2000	V	HBM[2)]
ESD robustness all pins	$\lvert V_{ESD\_CDM} \rvert$			500	V	CDM[3)]
ESD robustness (corner pins)	$\lvert V_{ESD\_CDM\_CORNER} \rvert$			750	V	CDM[3)] for cornet pins only

1) Not subject to production test, specified by design

2) ESD robustness, Human Body Model (HBM) according to ANSI/ESDA/JEDEC JS001 (1.5kΩ, 100 pF)

3) ESD robustness, Charge Device Model (CDM) according to ANSI/ESDA/JEDEC JS-002

2.5 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.

Table 10 Thermal resistance parameters

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Junction-to-ambient thermal resistance	$R_{\theta JA}$		29.5		°C/W	Ta = 25 °C, FR4 PCB, size: 76.2 × 114.3 × 1.57 mm³, stack 2S2P
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$		18.9		°C/W	Ta = 25 °C

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Junction-to-case (bottom) thermal resistance	$R_{\theta JC(bot)}$		6.45		°C/W	Ta = 25 °C

2.6 Electrical Characteristics

2.6.1 MOTIX™ 6EDL7141 Electrical Characteristics

PVDD = 5.5 to 60 V, T_A = 25°C, unless specified under test condition. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest), positive currents are flowing into the pin (unless otherwise specified).

Table 11 Electrical characteristics

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Power Supply (PVDD)						
Supply voltage	PVDD	5.5		60	V	
PVDD current, ACTIVE mode including XMC1404[2)]	I_{PVDD_ACTIVE}	15		55	mA	$V_{EN\_DRV} > V_{EN\_DRV\_TH}$, $V_{CE} > V_{CE\_TH\_R}$, PVDD = 40V, typical application.
PVDD current , STANDBY mode including XMC1404[2)]	$I_{PVDD\_STANDBY}$	10.5		15	mA	$V_{EN\_DRV} < V_{EN\_DRV\_TH}$, $V_{CE} > V_{CE\_TH\_R}$, PVDD = 13V, typical application
PVDD current, OFF mode (STOP state) including XMC1404[2)]	I_{PVDD_OFF}	5		20	µA	$V_{EN\_DRV} < V_{EN\_DRV\_TH}$, $V_{CE} < V_{CE\_TH\_R.}$ PVDD = 13V, typical application
Gate Driver Output						
Low side gate driver supply voltage target	VCCLS	7		15	V	Generated from charge pump. Gate driver supply voltage programmable via SPI
High side gate driver supply voltage target	VCCHS	10.8		74.3	V	Generated from charge pump. Gate driver supply voltage programmable via SPI according to VCCLS
High side gate driver output	$V_{GHx-SHx}$	0		VCCLS - 0.7	V	More details in section 2.7
Low side gate driver output	$V_{GLx-SLx}$	0		VCCLS	V	More details in section 2.7
Peak source current (high side and low side drivers)	$I_{GD\_SRC\_PEAK}$		1.5		A	Current flowing from pin. Gate driver current programmable via SPI

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Peak sink current (high side and low side drivers)	$I_{GD\_SNK\_PEAK}$		1.5		A	Current into the pin. Gate driver current programmable via SPI
Hold gate current[1)]	I_{HOLD}		250		mA	Low side gate driver
			50			High side gate driver
Source and sink current accuracy	$I_{GD\_ACCURACY}$	-20		20	%	With respect to gate driver current mean value. Mean value for the different programmed settings can deviate from target value
Charge pump clock frequency	f_{CP_CLK}	190		1600	kHz	Programmable via SPI
Charge pump clock accuracy	$f_{CP\_CLK\_ACC}$	-5		5	%	Charge pump clock accuracy
Charge pump clock frequency spread spectrum[1)]	$f_{CP\_CLK\_SS}$	0		30	%	
High side gate driver average current	I_{GD_VCCHS}			60	mA	PVDD ≥ 9.5 V operation
				30		PVDD < 9.5 V operation
Low side gate driver average current	I_{GD_VCCLS}			60	mA	PVDD ≥ 9.5 V operation
				30		PVDD < 9.5 V operation
Charge pump ramp up time[1)]	t_{CP_START}			250	µs	$C_{CP1/2}$ = 220 nF, C_{VCCLS}=1 µF, I_{LOAD} <50 µA, PVCC = 12 V. PVDD ≥ 10 V. Depends on capacitance values and features like charge pump pre-charge
				1	ms	C_{CPx} = 220 nF, C_{VCCLS}=1 µF, I_{LOAD} <50 µA, PVCC = 12 V. PVDD < 10 V. Depends on capacitance values and features like charge pump pre-charge
Gate driver PWM frequency[1)]	f_{PWM_GD}			200	kHz	
Input pin pulse width	t_{INx_PW}	80			ns	Applies to INHx and INLx pins. Pre-charge current disabled, current setting to 1.5A
Dead-time[1)]	t_{DT_RISE}, t_{DT_FALL}	120			ns	This is the minimum dead time value possible. If input signals have dead time lower than this, this value applies otherwise input PWM signal dead time is used. Value is programmable via SPI.

Parameter	Symbol	Values			Unit	Condition
		Min	Typ	Max		
Gate to Source passive weak pull-down resistor	$R_{GS\_PD\_WEAK}$	70	100	130	kΩ	Always active
Gate to Source active strong pull-down resistor	$R_{GS\_PD\_STRONG}$	0.25	1	2	kΩ	Pull-down resistor enabled when EN_DRV or PVDD are off and $V_{Gxy} - V_{Sxy} \geq 2$ V. Both high side and low side drivers
Propagation delay INHx to GHx	t_{PROP_HS}	80		250	ns	Dead time not considered. From 50% input to 50% output
Propagation delay INLx to GLx	t_{PROP_LS}	80		250	ns	Dead time not considered. From 50% input to 50% output
Propagation delay matching high-low side[1)]	$t_{PROP\_MATCH\_HL}$	0	25		ns	
Channel-to-channel propagation delay matching[1)]	$t_{PROP\_MATCH\_CH}$	0		10	ns	
Channel-to-channel dead time matching[1)]	$t_{DT\_MATCH\_CH}$	0		10	ns	
Gate to source comparator threshold	$V_{GS\_CPM\_TH}$		250		mV	Threshold voltage referred to: For pull down GHx - SHx (resp. GLx-SLx for low side driver). For pull up VCCHS - GHx (resp. VCCLS - GLx for low side driver)
Gate to source comparator deglitch time[1)]	$t_{VGS\_CMP\_DEGLITCH}$		500		ns	

Synchronous Buck Converter

Buck converter output target voltage	$VDDB_{NOM}$		6.5		V	PVCC_SETPT=b'11, PVDD ≥ 8 V, I_{VDDB} = 0 A
			7.0			PVCC_SETPT=b'10, PVDD ≥ 8.5 V, I_{VDDB} = 0 A
			8.0			PVCC_SETPT=b'0x, PVDD ≥ 9.5 V, I_{VDDB} = 0 A
Buck regulator output voltage at low input voltage (PVDD)	$VDDB_{NOM\_LV}$	4.6	6.5	6.65	V	PVCC_SETPT=b'11, 5.5 V ≤ PVDD < 8 V Buck with fixed duty cycle. VDDB dependent on I_{VDDB}. Min value defined at I_{VDDB} = 200mA condition
		4.6	7.0	7.15		PVCC_SETPT=b'10, 5.5 V ≤ PVDD < 8.5 V

						Buck with fixed duty cycle. VDDB depends on I_{VDDB}. Min value defined at I_{VDDB} = 200mA
		4.6	8.0	8.21		PVCC_SETPT=b'0x, 5.5 V ≤ PVDD < 9.5 V Buck with fixed duty cycle. VDDB depends on I_{VDDB}. Min value defined at I_{VDDB} = 200mA
Buck converter output voltage load regulation[1)]	$\Delta VDDB_{LOAD}$	-10		9	%	PVDD > $VDDB_{NOM}$ + 2.5 V, I_{VDDB} transient from 60 mA to 540 mA (10% to 90% load transient), C_{VDDB} = 47 µF, L = 22 µH, f_{BUCK_SW} = 500 kHz
		-9.5		5	%	PVDD > $VDDB_{NOM}$ + 2.5 V, I_{VDDB} transient from 60 mA to 540 mA (10% to 90% load transient), C_{VDDB} = 47 µF, L = 10 µH, f_{BUCK_SW} = 1000 kHz
Buck converter maximum average current	I_{VDDB_MAX}			600	mA	PVDD ≥ 9.5 V. VDDB supplies charge pumps, DVDD linear regulator and VDDB pin
				200	mA	PVDD at low input voltage range ($VDDB_{NOM\_LV}$). VDDB supplies charge pumps, DVDD linear regulator and VDDB pin
Buck converter maximum duty cycle	DC_{BUCK_MAX}		95		%	
Buck converter high side switch R_{DSON}	$R_{DSON\_BUCK\_HS}$	0.7	1.4	2.2	Ω	
Buck converter low side switch R_{DSON}	$R_{DSON\_BUCK\_LS}$	0.3	0.45	1.0	Ω	
Buck switching frequency[1)]	f_{BUCK_SW}	440	500	590	kHz	Configurable via OTP write. May vary during load steps. Valid for the recommended component values L_{BUCK} = 22µH and C_{BUCK} = 47µF. See Table 30
		850	1000	1150		Configurable via OTP write. May vary during load steps. Valid for the recommended component values L_{BUCK} = 10µH and C_{BUCK} = 47µF. See Table 30
Buck converter soft start timing[1)]	$t_{VDDB\_SFT\_START}$			1500	µs	Actual value depends on buck output filter

Linear Regulator DVDD

Regulator target output voltage	DVDD		3.3		V	IMD700A part number
			5.0			IMD701A part number
Output voltage accuracy	$DVDD_{ACC}$	-2.5		2.5	%	
DVDD load current	I_{DVDD}			300	mA	
DVDD load current limit	I_{DVDD_LIM}	50		450	mA	Programmable via SPI
Static line regulation	$\Delta DVDD_{LINE}$			10	mV	VDDB=6.5 V...8 V, I_{DVDD}=300 mA
Static load regulation	$\Delta DVDD_{LOAD}$			40	mV	VDDB=DVDD+1.5 V, I_{DVDD} = 1 mA to 300 mA step
Analog programming pins period[1)]	t_{AN_T}		25		µs	CS_GAIN
DVDD turn on delay[1)]	$t_{DVDD\_TON\_DLY}$	200		800	µs	Programmable via SPI. Delay between VDDB UVLO until DVDD ramp up start
DVDD soft start timing[1)]	$t_{DVDD\_SFT\_START}$	100		1600	µs	Configurable via SPI- Current limited by $I_{DVDD\_I\_LIM}$. If due to larger C_{DVDD} values, programmed timing is not achievable, start-up time is defined by $t_{DVDD\_SFT\_START} = \frac{C_{DVDD} * DVDD}{I_{DVDD\_I\_LIM}}$

Current Sense Amplifier

Closed loop gain	G_{CS}	4		64	V/V	Configured either via external resistor or SPI
Gain error[1)]	G_{CS_ERROR}	-1		1	%	Measured at SLx-CSNx=0.025 V
Offset input referred[1)]	V_{CS_OS}	-600	200	600	µV	Gain=32, inputs shorted
Offset temperature drift[1)]	$\Delta V_{CS\_OS}/\Delta T$		5		µV/°C	
Current sense blanking time[1)]	t_{CS_BLANK}	0		8	µs	Programmable via SPI
Amplifier output settling time [1)]	$t_{CSO\_SETTLING}$		600		ns	Time from input signal step to 1% of final output voltage. Input voltage step of 0.2 V. Gain 4 to 24
			1000			Settling time from input signal step to 1% of final output voltage. Input voltage step of 0.2 V. Gain 32 to 64

Unity gain bandwidth[1)]	GBW	5	8		MHz	
Common mode rejection ratio[1)]	CMRR	60	80		dB	Gain=8, f_{SW} from 0 Hz to 80 kHz
Power supply rejection ratio [1)]	PSRR	60			dB	Gain=8, f<1 MHz
		40				Gain=8, f<10 MHz
Input bias current	I_{CSN}			50	µA	Current drawn into pin
Common mode input range[1)]	V_{CS_COM}	-0.3		0.3	V	
Differential mode input range	V_{CS_DIFF}	-0.3		0.3	V	
Current sense output voltage range	V_{CSO}	0.3		DVDD-0.3	V	
Output voltage slew rate[1)]	SR_{CSO}	-10		10	V/µs	Gain=8, R_L=470 Ω, C_L=330 pF. V_{SLx} = +/-250 mV
Propagation delay from gate driver (Gxy) transition to CSOx activation[1)]	t_{CSAMP_PROP}		130		ns	CSAMP in shunt mode
			400			CSAMP in R_{DSON} mode
Output target voltage reference for current sense amplifier (offset)-VREF	V_{CS_REF}	1/4* DVDD		1/2* DVDD	V	
Output voltage reference for current sense amplifier (offset) –VREF-accuracy[1)]	$V_{CS\_REF\_ACC}$	-2		2	%	CSAMP internal offset voltage error. DVDD error excluded
Output short circuit limit	I_{CS_SC}		20		mA	Pin CSOx shorted to ground
Auto-Zero active time[1)]	t_{AUTO_ZERO}		1.7		µs	Normal mode
			2			Rdson sensing mode
Auto-Zero cycle time[1)]	$t_{AUTO\_ZERO\_CYCLE}$			100	µs	If GHx is switching
				200		If GHx is not switching
AZ external Auto-Zero signal frequency[1)]	$f_{AZ\_CP\_CLK\_OFF}$	5		100	kHz	
AZ external Auto-Zero signal pulse width[1)]	$t_{AZ\_EXT\_PW}$	0.1		3.5	µs	

Current Sense Amplifier Over-Current Protection Comparator and DAC

Current sense over-current comparator hysteresis	$V_{CS\_OC\_HYST}$			5	mV	
Over-current comparator input offset		-12		12	mV	
Over-current deglitch time[1)]	$t_{CS\_OCP\_DEGLITCH}$	0		8	µs	Programmable via SPI
Current Sense Input referred OCP threshold positive target level	$V_{CS\_OCP\_THP}$	20		300	mV	Programmable via SPI
Current sense input referred OCP threshold negative target level	$V_{CS\_OCP\_THN}$	-300		-20	mV	Programmable via SPI
Over-current blanking time[1)]	t_{OCP_BLANK}	0		10	µs	Programmable via SPI:

Gate Driver Analog to Digital Converter (ADC)

ADC resolution	ADC_N		7		bits	
ADC gain error	ε_{GAIN}	-1.05		1.05	%	
ADC offset error	$\varepsilon_{ADC\_OFFS\_ERR}$	2		2	LSB	
ADC conversion time	t_{CONV}		1.28		µs	

Logic Level Digital Inputs (CE, EN_DRV)

Internal pull-down resistor to GND CE	R_{PD_CE}	350	625	850	kΩ	V_{CE} > 2V
Internal pull-down resistor to GND EN_DRV	$R_{PD\_EN\_DRV}$		500		kΩ	
CE threshold voltage rising	$V_{CE\_TH\_R}$	2.7			V	T_A = -40 °C to 125 °C. This is the minimum CE pin voltage above which, any device (operated within recommended conditions) will activate the device operation.
CE threshold voltage falling	$V_{CE\_TH\_F}$			0.6	V	T_A = -40 °C to 125 °C. This is the maximum CE pin voltage below which, any device (operated within recommended conditions) will stop the device operation.
CE pin sink current	I_{CE_SNK}			10	µA	Current flowing into CE pin
EN_DRV threshold voltage	$V_{EN\_DRV\_TH}$		0.5* DVDD		V	

EN_DRV threshold voltage hysteresis	$V_{EN\_DRV\_TH\_HYS}$		4		%	Applies to $V_{EN\_DRV\_TH}$ thresholds

6EDL7141 OTP Programming

OTP programming supply[1)]	$PVDD_{OTP\_PROG}$	13			V	Below this value an OTP blocking will occur
OTP programming temperature[1)]	T_{OTP_PROG}			150	°C	Above this value an OTP blocking will occur

Watchdog

Watchdog buck converter input time	t_{WD_BUCK}		1.5		ms	Applies to buck converter input selection only. Not configurable value

Overload Protections Gate Driver

PVDD UVLO threshold rising	$V_{PVDD\_UVLO\_R}$	4.95	5.1	5.25	V	
PVDD UVLO threshold falling	$V_{PVDD\_UVLO\_F}$	4.85	5.0	5.15	V	
VCCHS UVLO threshold rising	$V_{HS\_UVLO\_R}$	5.6	5.8	6.0	V	
VCCHS UVLO threshold falling	$V_{HS\_UVLO\_F}$	4.3	4.5	4.7	V	
VCCLS UVLO threshold rising	$V_{LS\_UVLO\_R}$	6.1	6.4	6.7	V	
VCCLS UVLO threshold falling	$V_{LS\_UVLO\_F}$	4.3	4.5	4.7	V	

Overload Protections Power Supply System

VDDB UVLO rising threshold	$V_{VDDB\_UVLO\_R}$	4.2	4.3	4.4	V	
VDDB UVLO falling threshold	$V_{VDDB\_UVLO\_F}$	4.1	4.2	4.3	V	
VDDB OVLO rising threshold	$V_{VDDB\_OVLO\_R}$	105	108	111	%	Percentage of target output value
VDDB OVLO falling threshold	$V_{VDDB\_OVLO\_F}$	101	105	107	%	Percentage of target output value
Buck OCP (inductor current) threshold	$I_{BUCK\_OCP\_TH}$		1.0		A	f_{BUCK_SW} = 500kHz
			1.3			f_{BUCK_SW} = 1MHz
Buck OCP hysteresis	$I_{BUCK\_OCP\_HYS}$		50		mA	
DVDD UVLO rising threshold	$V_{DVDD\_UVLO\_R}$		85		%	Percentage of target output value

DVDD UVLO falling threshold	$V_{DVDD\_UVLO\_F}$		75		%	Percentage of target output value
DVDD OVLO rising threshold	$V_{DVDD\_OVLO\_R}$		110		%	Percentage of target output value
DVDD OVLO falling threshold	$V_{DVDD\_OVLO\_F}$		105		%	
DVDD target output current limit	$I_{DVDD\_I\_LIM}$	50		450	mA	Configurable via SPI
DVDD target output current limit accuracy	$I_{DVDD\_I\_ACC}$	-30		10	%	T_J=-40 °C to 125 °C, limit setting to 50mA
		-18		10	%	T_J=-40 °C to 125 °C, for other limit settings

Gate Driver Over-Temperature Protection

Over-temperature shut-down threshold	OTS_{TH}		150		°C	
OTS Hysteresis	OTS_{HYS}		10		°C	
Over-temperature warning threshold	OTW_{TH}		125		°C	Measured via internal ADC
Over-temperature warning hysteresis	OTW_{HYS}		10		°C	

Locked Rotor Protection

Locked rotor detect time[1)]	t_{LOCK}	1		8	s	Programmable via SPI

SPI Timing Requirements[1)]

Clock period	t_{CLK}	77			ns	
Clock high time	t_{CLKH}	20			ns	
Clock low time	t_{CLKL}	20			ns	
SDI input data setup time	t_{SET_SDI}	10			ns	
SDI input data hold time	t_{HD_SDI}	10			ns	
SDO output data delay time	t_{DLY_SDO}	0		20	ns	SCLK high to SDO valid
SDO rise and fall time	t_{RF_SDO}			10	ns	
nSCS enable time	t_{EN_nSCS}			50	ns	nSCS low to SDO transition
nSCS disable time,	t_{DIS_nSCS}			50	ns	nSCS high to SDO high impedance
nSCS hold time	t_{HD_nSCS}	50			ns	Falling SCLK to rising nSCS

nSCS setup time	t_{SET_nSCS}	50			ns	Falling nSCS to rising SCLK
nSCS sequential delay time	t_{SEQ_nSCS}	450			ns	Rising nSCS to falling nSCS

1. *Not subject to production test*
2. *For more details on XMC1404 power consumption, see XMC1400 datasheet. The consumption of XMC1404 is dependent on the specific usage of the device*

2.6.2 XMC1404 Electrical Characteristics

Table 12 provides the characteristics of the input/output pins of the XMC1404.

The parameters listed in this section represents partly the characteristics of the XMC1400 and partly its system requirements. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the“Symbol” column:

- CC: such parameters indicate Controller Characteristics, which are distinctive feature of the XMC1404 and must be regarded for a system design.
- SR: such parameters indicate System Requirements, which must be provided by the application system in which the XMC1404 is designed in.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 12 Input/Output Characteristics (Recommended Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC		1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
				0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	DVDD – 1.0	–	V	I_{OH} = -10 mA
			DVDD-0.4	–	V	I_{OH} = -4.5 mA
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR		0.19 x DVDD	V	CMOS Mode
Input high voltage on port pins (standard hysteresis)	V_{IHPS}	SR	0.7 x DVDD	–	V	CMOS Mode
Input low voltage on port pins (large hysteresis)	V_{ILPL}	SR	–	0.08 xDVDD	V	CMOS Mode
Input high voltage on port pins (large hysteresis)	V_{IHPL}	SR	0.85 xDVDD	–	V	CMOS Mode
Rise/fall time on standard pad[1)]	t_R, t_F	CC	–	12	ns	50 pF, DVDD = 5V [2)]

Input hysteresis on port pin except P2.3 - P2.9[3]	HYS CC	0.08 xDVDD	–	V	CMOS mode standard hysteresis
		0.5 xDVDD	0.75 xDVDD	V	CMOS mode, large hysteresis
Input hysteresis on port pin P2.3 - P2.9[3]	HYS_P2 CC	0.08 xDVDD	–	V	CMOS mode standard hysteresis
		0.35 xDVDD	0.75 xDVDD	V	CMOS mode, large hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-up current on port pins	I_{PUP} CC	–	-80	µA	$V_{IH,min}$
		-95	–		$V_{IL,max}$
Pull-down current on port pins	I_{PDP} CC	–	40	µA	$V_{IL,max}$
		95	–		$V_{IH,min}$
Input leakage current except P0.11[4]	I_{OZP} CC	-1	1	µA	0 < VIN < DVDD, T_A 105 °C
Input leakage current for P0.11[4]	I_{OZP1} CC	-10	1	µA	0 < VIN < DVDD, T_A 105 °C
Voltage on any pin during DVDD power off	V_{PO} SR	–	0.3	V	
Maximum current per pin (excluding P1, DVDD and VSS)[5]	I_{MP} SR	-10	11	mA	–
Maximum current per high current pins	I_{MP1A} SR	-10	50	mA	–

1. *Rise/Fall time parameters are taken with 10% - 90% of supply.*
2. *Additional rise/fall time valid for C_L = 50 pF - C_L = 100 pF @ 0.150 ns/pF at 5 V supply voltage.*
3. *Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.*
4. *An additional error current $_{(IINJ)}$ will flow if an overload current flows through an adjacent pin.*
5. *However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when VDDP is powered off.*

2.7 Electrical Characteristic Graphs

Following graphs provide information on the behavior of the device at different conditions. This data is not subject to production test. T_A = 25°C, unless otherwise specified. All voltages are referred to ground (PGND for buck converter, charge pumps and gate driver related parameters and DGND for the rest).

Note: More details on XMC1404 consumption can be found in XMC1404 Datasheet

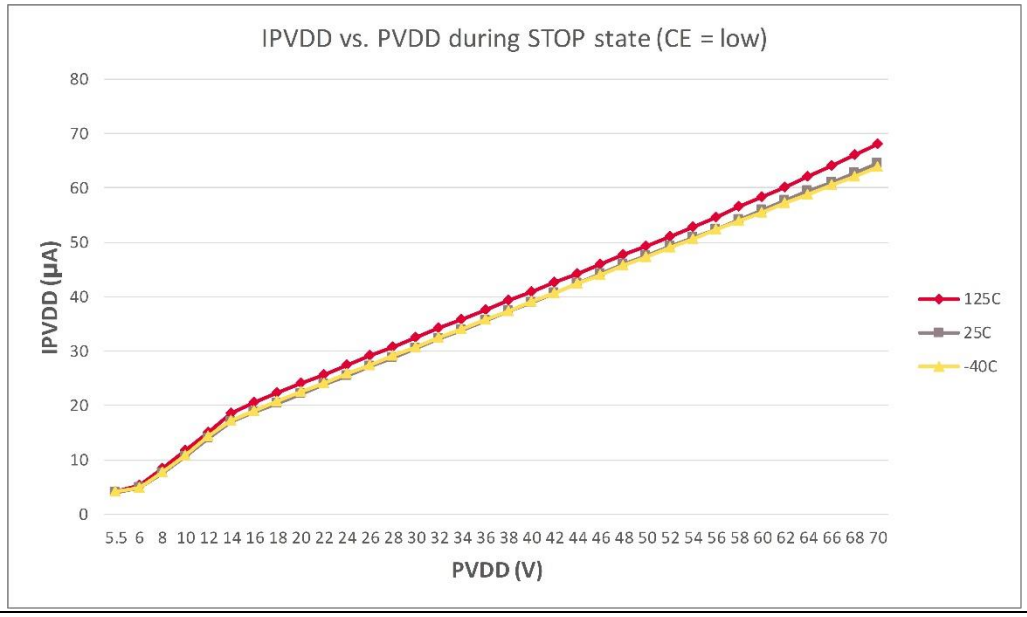

Figure 5 Current consumption on PVDD pin vs PVDD when both CE and EN_DRV are below active thresholds.

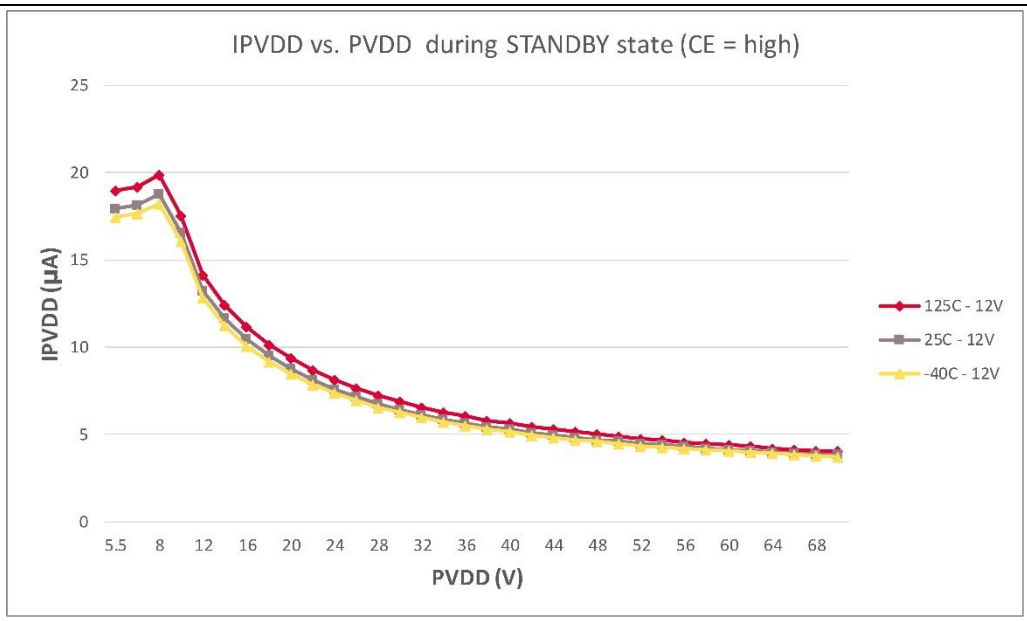

Figure 6 Current consumption on PVDD vs PVDD voltage during STANDBY state - CE is above active threshold and EN_DRV is below

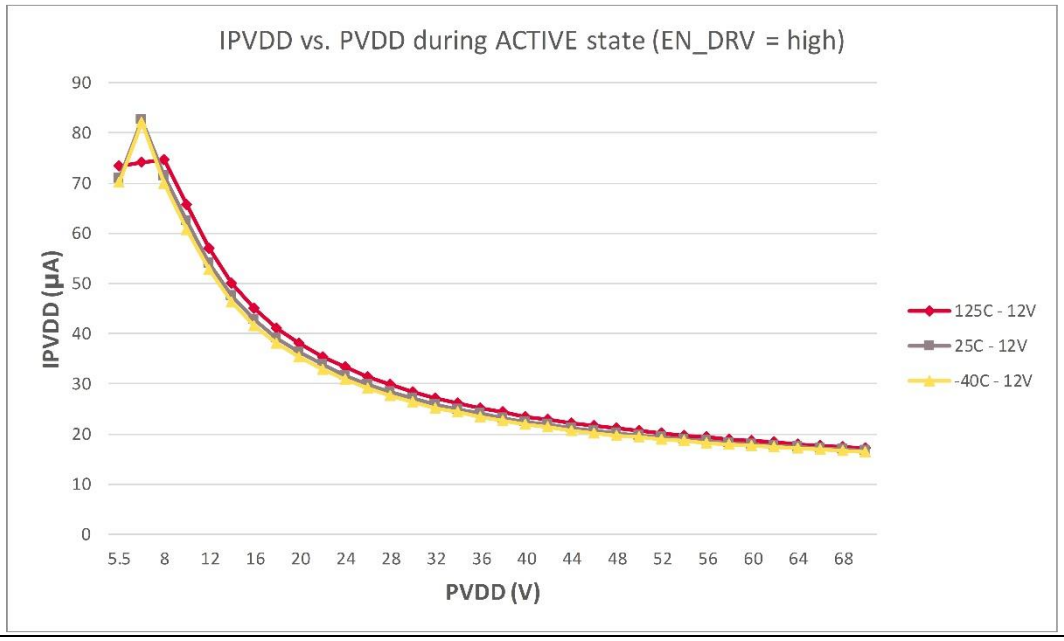

Figure 7 Current Consumption on PVDD vs PVDD voltage during ACTIVE state – CE and EN_DRV are above active threshold

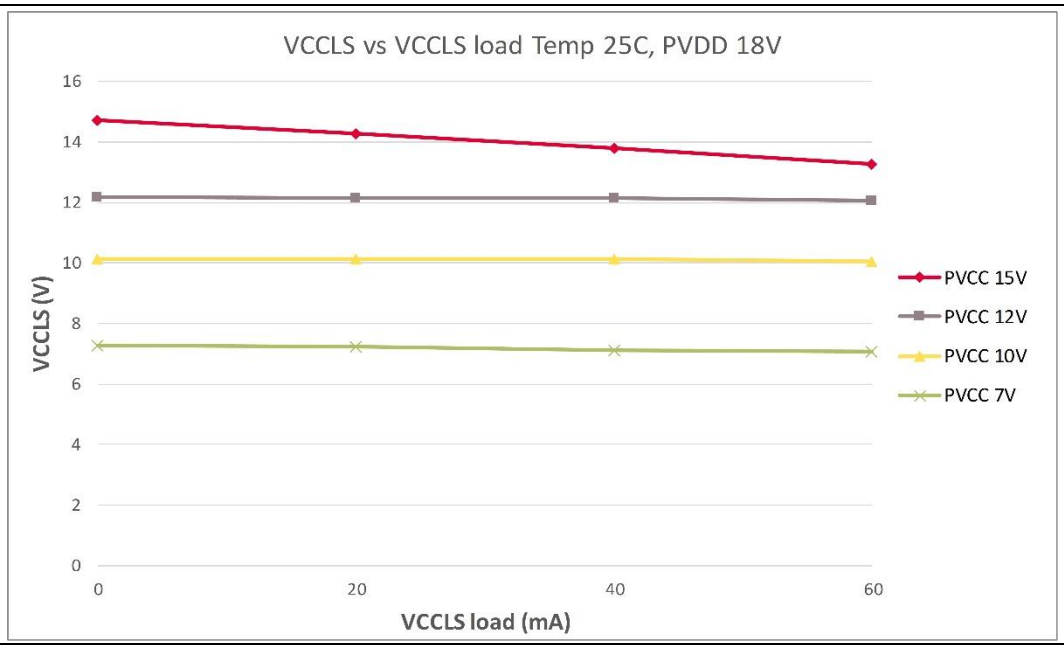

Figure 8 VCCLS average voltage vs VCCLS load (DC) for different PVCC configurations at PVDD 18V. XMC active and executing code. Typical application with $C_{CP1(2)}$ = 220nF and $C_{VCCLS/HS}$ = 1uF. VCCHS load 20mA.

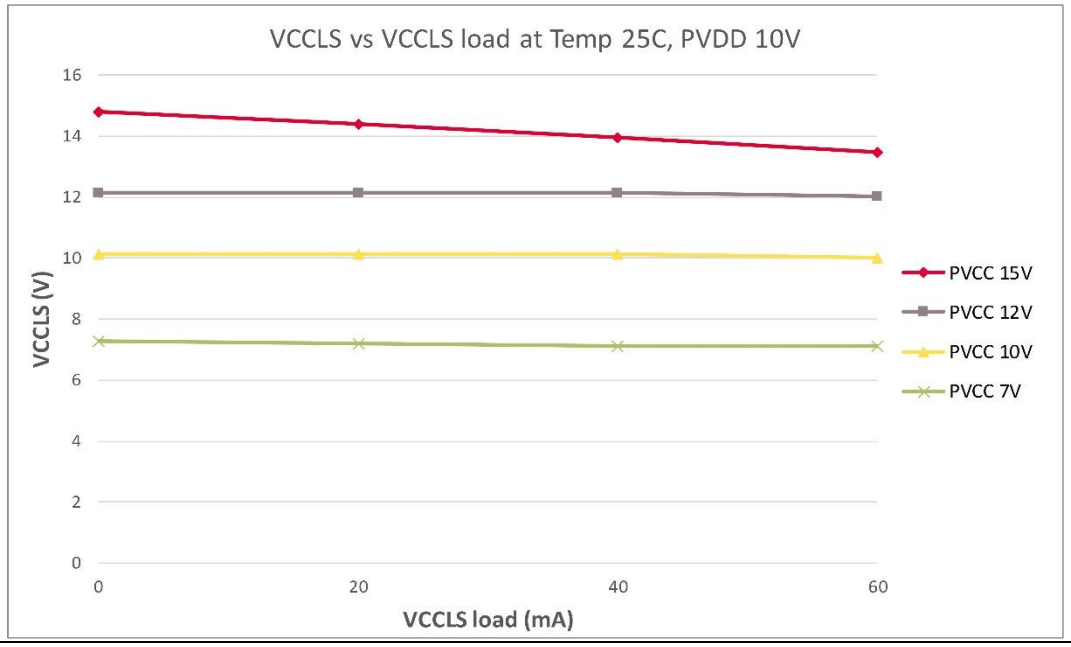

Figure 9 VCCLS average voltage vs VCCLS load (DC) for different PVCC configurations at PVDD 10V. XMC active and executing code. Typical application with $C_{CP1(2)}$ = 220nF and $C_{VCCLS/HS}$ = 1uF. VCCHS load 20mA.

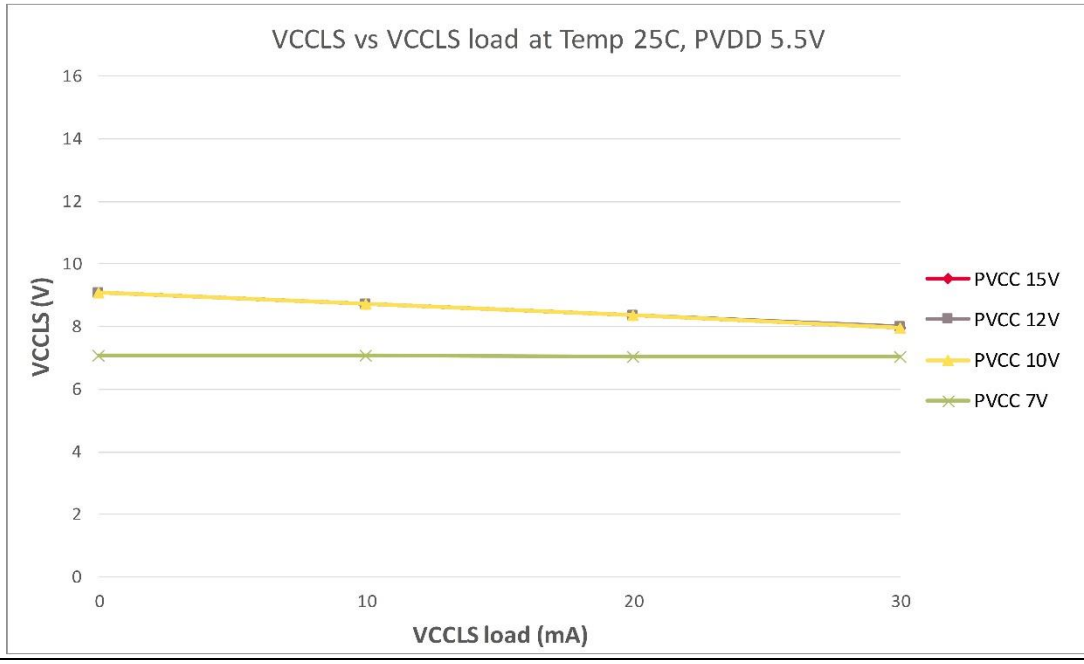

Figure 10 VCCLS average voltage vs VCCLS load (DC) for different PVCC configurations at PVDD 5.5V. XMC active and executing code. Typical application with $C_{CP1(2)}$ = 220nF and $C_{VCCLS/HS}$ = 1uF. VCCHS load 20mA.

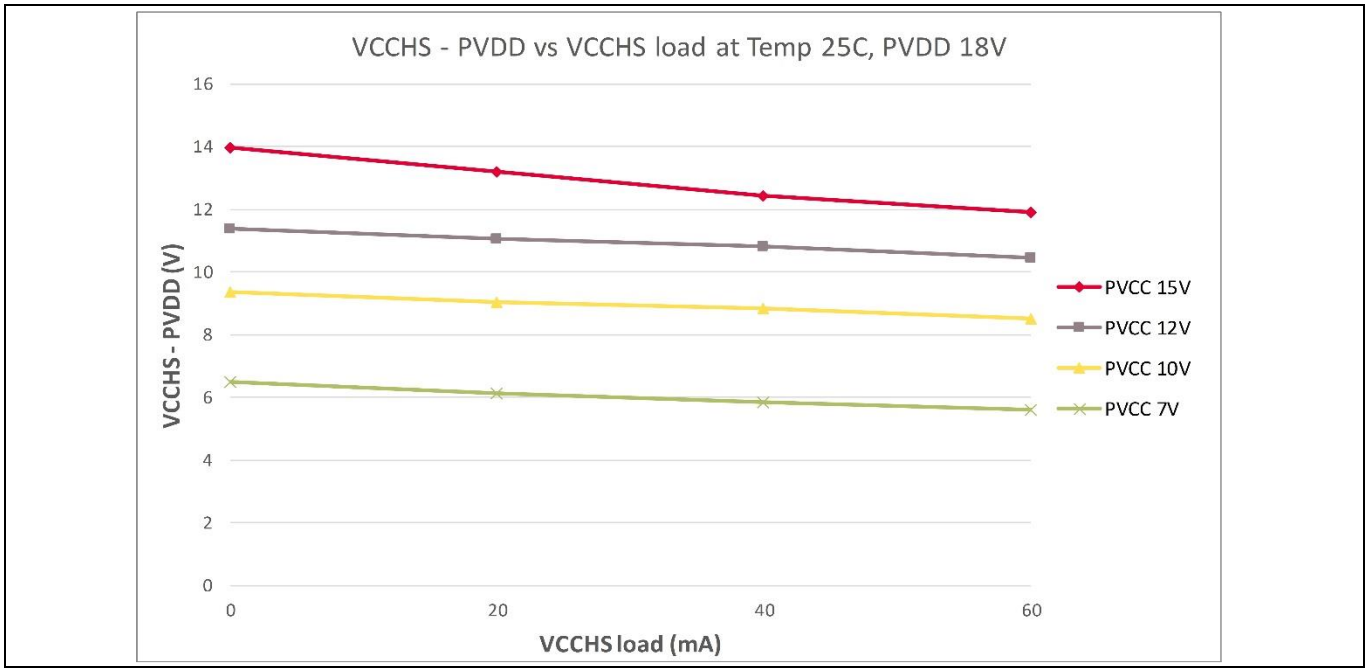

Figure 11 VCCHS average voltage vs VCCHS load (DC) for different PVCC configurations at PVDD 18V. XMC active and executing code. Typical application with $C_{CP1(2)}$ = 220nF and $C_{VCCLS/HS}$ = 1uF. VCCLS load 20mA.

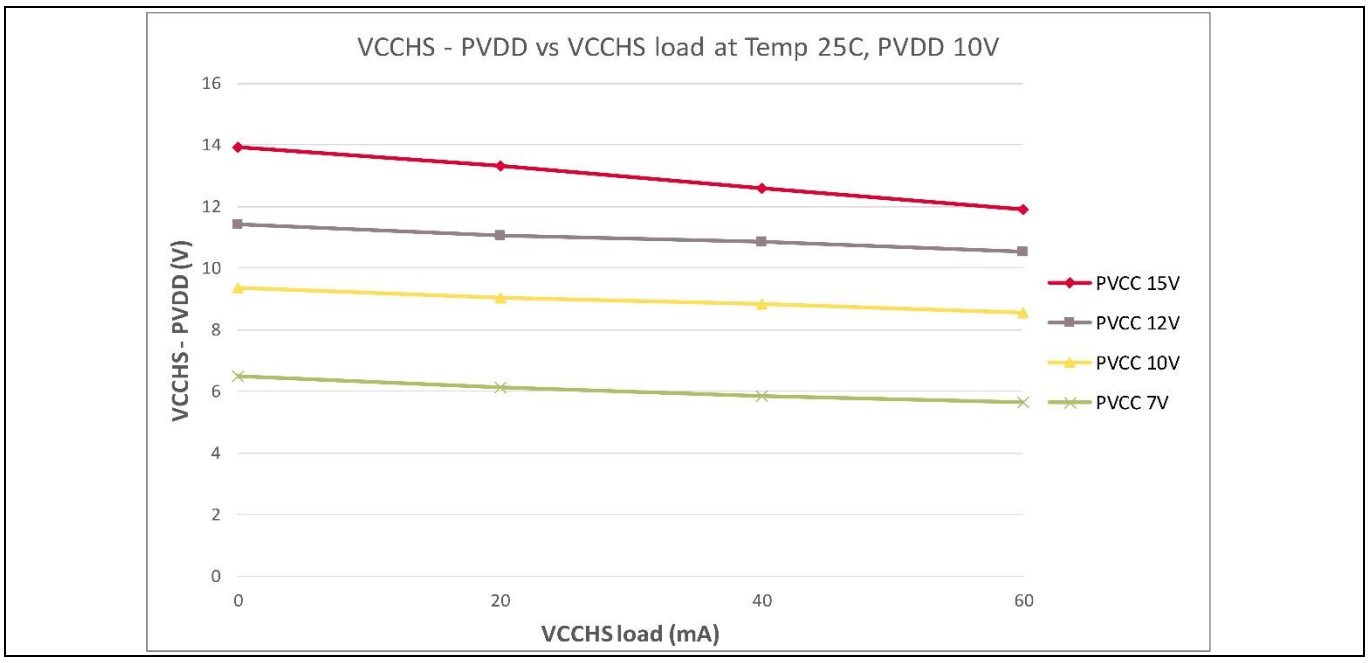

Figure 12 VCCHS average voltage vs VCCHS load (DC) for different PVCC configurations at PVDD 10V. XMC active and executing code. Typical application with $C_{CP1(2)}$ = 220nF and $C_{VCCLS/HS}$ = 1uF. VCCLS load 20mA

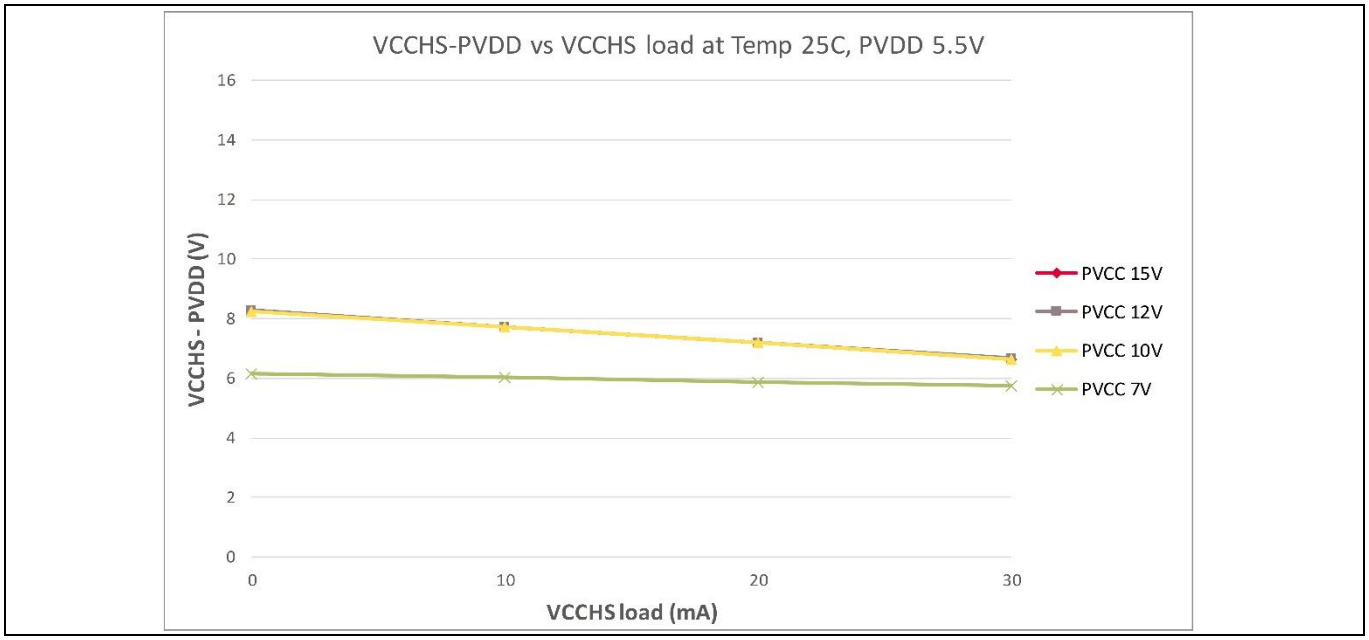

Figure 13 VCCHS average voltage vs VCCHS load (DC) for different PVCC configurations at PVDD 5.5V. XMC active and executing code. Typical application with $C_{CP1(2)}$ = 220nF and $C_{VCCLS/HS}$ = 1uF. VCCLS load 20mA

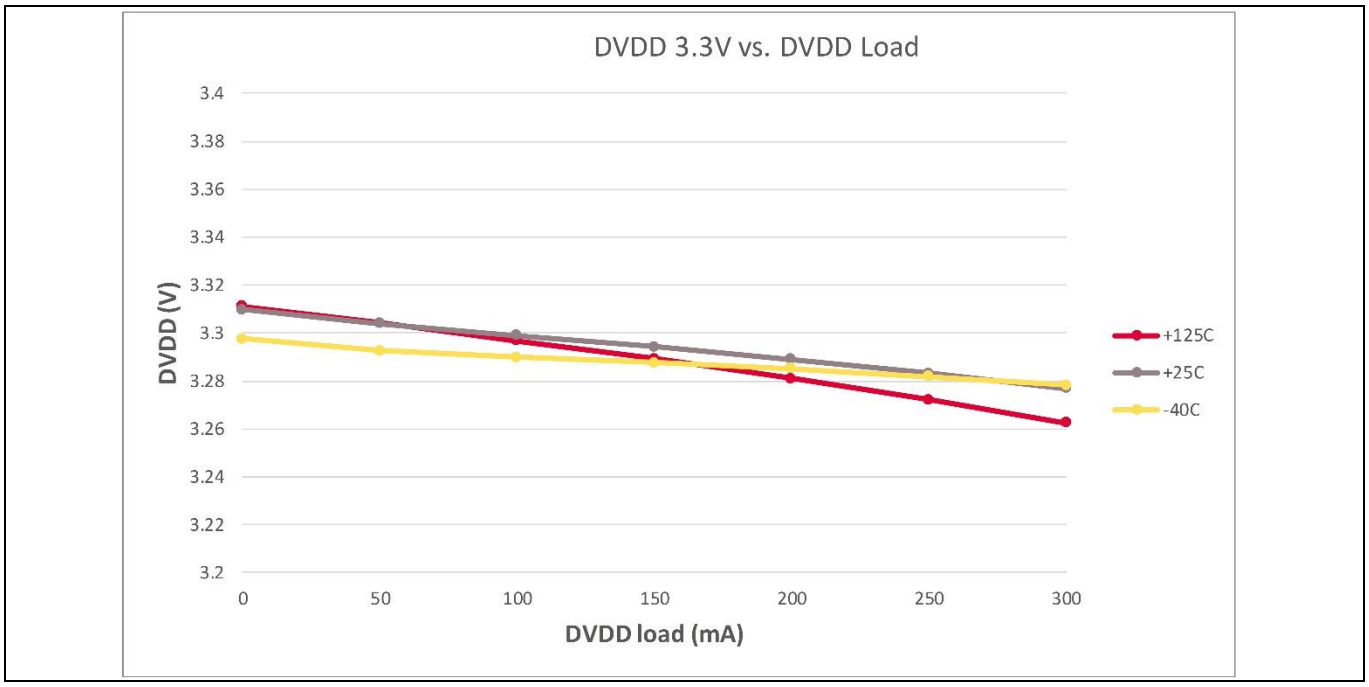

Figure 14 DVDD 3.3V output voltage vs DVDD load for IMD700A

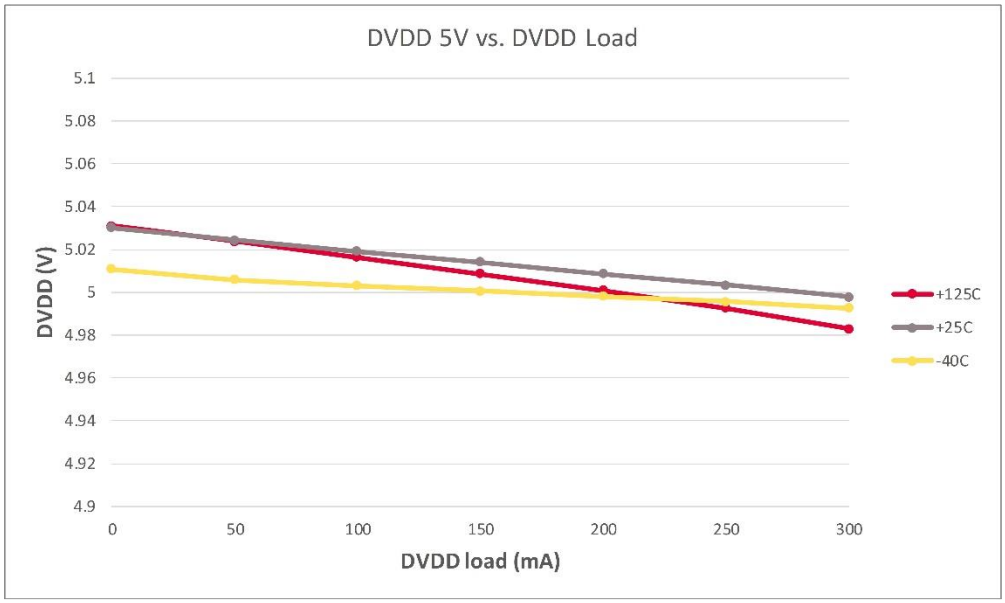

Figure 15 DVDD 5.0V output voltage vs DVDD load for IMD701A

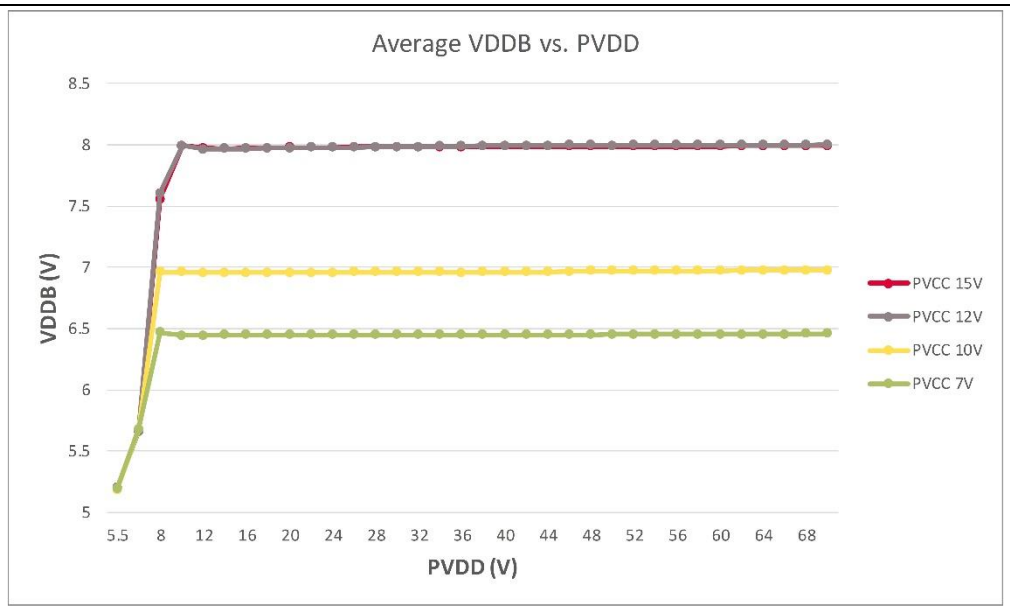

Figure 16 Buck converter average output voltage (VDDB) vs PVDD voltage. Typical configuration, with VDDB load 200mA and DVDD load of 50mA, buck converter switching frequency 500kHz, PVDD 18V.

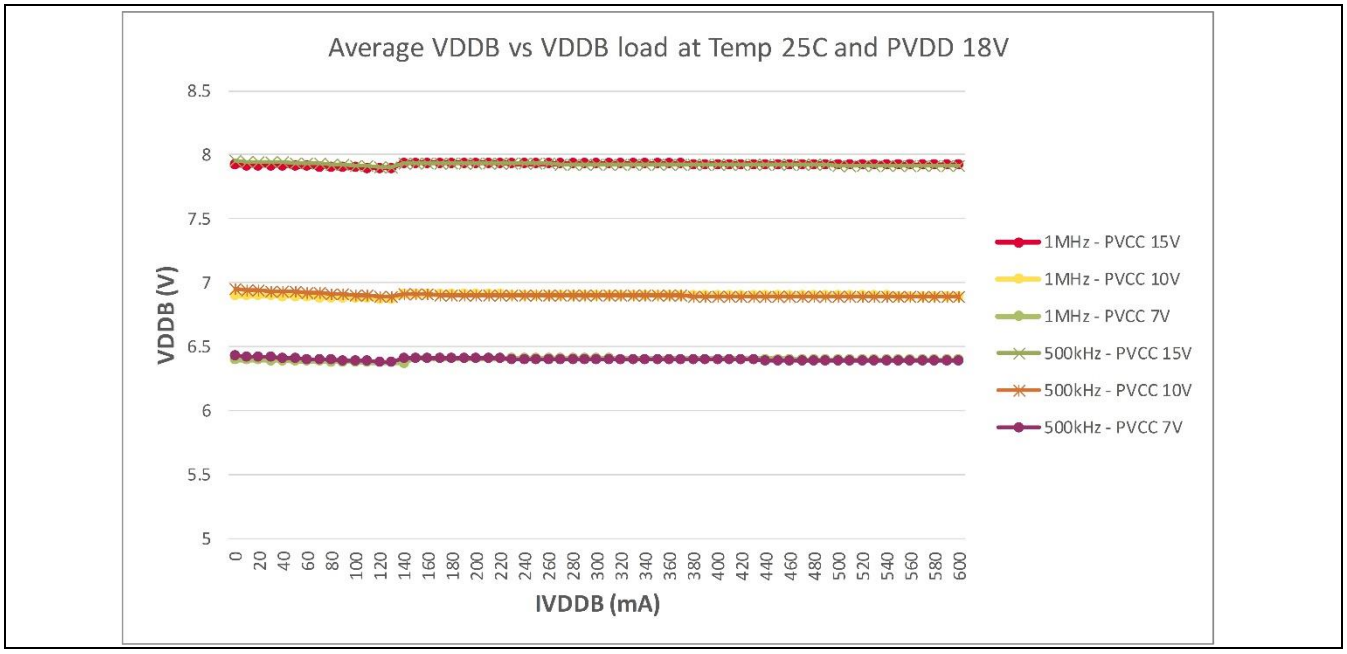

Figure 17 Buck converter average output voltage (VDDB) vs VDDB load (IVDDB) for different PVCC and buck switching frequency operations. Typical configuration with PVDD 18V.

2.8 XMC1404 Port I/O Alternate Functions Description

The method presented in Table 13 is used to describe the I/O functions of each PORT pin:

Table 13 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

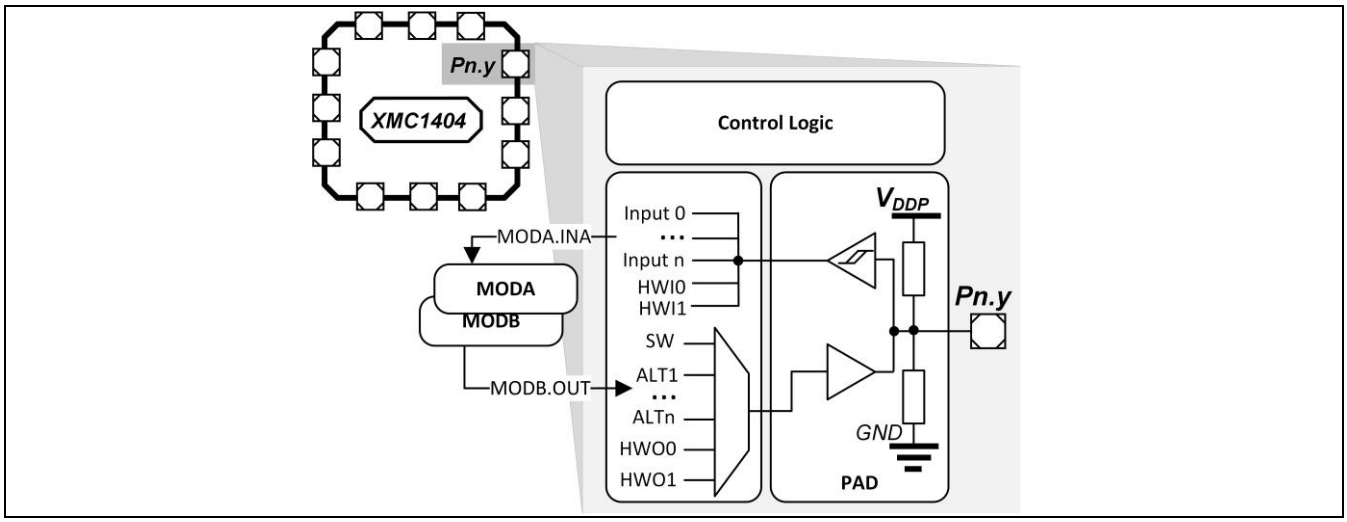

Figure 18 Simplified Port Structure of XMC Pins

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to nine alternate output functions (ALT1 to ALT9) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the Table 14 for the complete Port I/O function mapping.

2.8.1 XMC1404 Pin Definitions and Alternate Functions

In XMC1404 microcontroller, pins can be configured to perform different input and/or output functions. Each pin is connected internally to a de-multiplexer that allows that particular pin to be routed to different peripherals in the microcontroller. Input and/or output configurations are possible on most pins. Table 14 shows the different functions that are possible for XMC1404 pins in IMD70xA.

Table 14 Pin definitions and alternate functions for XMC1404

Functions	Outputs									Inputs										
Pin	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0	LEDTS0.LINE7	ERU0.GOUT0	CCU40.OUT0	CCU80.OUT00	USIC0_CH0.SELO0	USIC0_CH1.SELO0	CCU81.OUT00	USIC1_CH1.DOUT0	BCCU0.TRAPINB	CCU40.IN0AC					USIC1_CH1.DX0A	USIC0_CH0.DX2A		USIC0_CH1.DX2A		
P0.1	ERU0.PDOUT1	LEDTS0.LINE6	ERU0.GOUT1	CCU40.OUT1	CCU80.OUT01	BCCU0.OUT8	SCU.VDROP	USIC1_CH1.SCLKOUT	USIC1_CH1.DOUT0		CCU40.IN1AC					USIC1_CH1.DX0B	USIC1_CH1.DX1A				
P0.3	ERU0.PDOUT3	LEDTS0.LINE4	ERU0.GOUT3	CCU40.OUT3	CCU80.OUT03	VADC0.EMUX01	CCU80.OUT11	USIC1_CH1.SCLKOUT	USIC1_CH0.DOUT0		CCU40.IN3AC					USIC1_CH0.DX0B					
P0.4	BCCU0.OUT0	LEDTS0.LINE3	LEDTS0.COL3	CCU40.OUT1	CCU80.OUT13	VADC0.EMUX00SERVIC	WWDT.E_OUT	USIC1_CH1.SELO0	CAN.N0_TXD			CCU41.IN0AB	CCU80IN0AB							CAN.N0_RXDA	
P0.7	BCCU0.OUT3	LEDTS0.LINE0	LEDTS0.COL0	CCU40.OUT1	CCU80.OUT10	USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0	VADC0.EMUX12OUT1	CCU41.		CCU40.I N1AB	CCU41.I N3AB					USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C		
P0.10/XTAL1	BCCU0.OUT6	LEDTS1.LINE2	LEDTS0.COL5	ACMP0.OUT	CCU80.OUT22	USIC0_CH0.SELO1	USIC0_CH1.SELO1	CCU81.OUT22					CCU80.IN2AB	CCU81.IN2AB			USIC0_CH0.DX2C		USIC0_CH1.DX2C		
P0.11/XTAL2	BCCU0.OUT7	LEDTS1.LINE3	LEDTS0.COL4	USIC0_CH0.MCLKOUT	CCU80.OUT23	USIC0_CH0.SELO2	USIC0_CH1.SELO2	CCU81.OUT23									USIC0_CH0.DX2D		USIC0_CH1.DX2D		
P0.12	BCCU0.OUT6	LEDTS1.LINE4	LEDTS0.COL3	LEDTS1.COL3	CCU80.OUT33	USIC0_CH0.SELO3	CCU80.OUT20		CAN.N1_TXD	BCCU0.TRAPINA	CCU40.IN0AA	CCU40.IN1AA	CCU40.IN2AA	CCU81.IN0AU	CCU40.IN3AA	CCU80.IN0AA	USIC0_CH0.DX2E	CCU80.IN1AA	CCU80.IN2AA	CAN.N1_RXDA	CCU80.IN3AA
P0.14	BCCU0.OUT7	LEDTS1.LINE6	LEDTS0.COL1	LEDTS1.COL1	CCU80.OUT31	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		CAN.N0_TXD					CCU81.IN2AU	POSIF0.IN1B	USIC0_CH0.DX0A	USIC0_CH0.DX1A	USIC1_CH1.DX5B		CAN.N0_RXDC	
P0.15	BCCU0.OUT8	LEDTS1.LINE7	LEDTS0.COL0	LEDTS1.COL0	CCU80.OUT30	USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT		CAN.N0_TXD					CCU81.IN3AU	POSIF0.IN2B	USIC0_CH0.DX0B		USIC1_CH1.DX3B	USIC1_CH1.DX4B	CAN.N0_RXDD	

Functions	Outputs									Inputs											
Pin	**ALT1**	**ALT2**	**ALT3**	**ALT4**	**ALT5**	**ALT6**	**ALT7**	**ALT8**	**ALT9**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P1.0	BCCU0.OUT0	CCU40.OUT0	LEDTS0.COL0	LEDTS1.COLA	CCU80.OUT00	ACMP1.OUT	USIC0_CH0.DOUT0	CCU81.OUT00	CAN.N0_TXD						POSIF0.IN2A	USIC0_CH0.DX0C				CAN.N0_RXDG	
P1.1	ERU1.PDOUT1	CCU40.OUT1	LEDTS0.COL1	LEDTS1.COL0	CCU80.OUT01	USIC0_CH0.DOUT0	USIC0_CH1.SELO0	CCU81.OUT01	CAN.N0_TXD						POSIF0.IN1A	USIC0_CH0.DX0D	USIC0_CH0.DX1D		USIC0_CH1.DX2E	CAN.N0_RXDH	
P1.2	ERU1.PDOUT2	CCU40.OUT2	LEDTS0.COL2	LEDTS1.COL1	CCU80.OUT10	ACMP2.OUT	USIC0_CH1.DOUT0	CCU81.OUT10	CAN.N1_TXD						POSIF0.IN0A			USIC0_CH1.DX0B		CAN.N1_RXDG	
P1.3	ERU1.PDOUT3	CCU40.OUT3	LEDTS0.COL3	LEDTS1.COL2	CCU80.OUT11	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0	CCU81.OUT11	CAN.N1_TXD									USIC0_CH1.DX0A	USIC0_CH1.DX1A	CAN.N1_RXDH	
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3	LEDTS1.COL5	CCU80.OUT20	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT	CCU81.OUT20	CAN.N0_TXD		VADC0.G0CH5					USIC0_CH0.DX0E	USIC0_CH0.DX1E		USIC0_CH1.DX2F	CAN.N0_RXDE	ERU0.0B0
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2	LEDTS1.COL6	CCU80.OUT21	USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT	CCU81.OUT21	CAN.N0_TXD	ACMP2.INP	VADC0.G0CH6					USIC0_CH0.DX0F		USIC0_CH1.DX3A	USIC0_CH1.DX4A	CAN.N0_RXDF	ERU0.1B0
P2.2										ACMP2.INN	VADC0.G0CH7		ORC0.AIN	USIC1_CH0.DX5E		USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A			ERU0.0B1
P2.3												VADC0.G1CH5	ORC1.AIN	USIC1_CH0.DX3E	USIC1_CH0.DX4E	USIC1_CH1.DX5C	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C		ERU0.1B1
P2.4												VADC0.G1CH6	ORC2.AIN	USIC1_CH1.DX3C	USIC1_CH1.DX4C	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC1_CH0.DX5F	USIC0_CH1.DX5B		ERU0.0A1
P2.5												VADC0.G1CH7	ORC3.AIN	USIC1_CH1.DX5D		USIC0_CH0.DX5D		USIC0_CH1.DX3E	USIC0_CH1.DX4E		ERU0.1A1
P2.6										ACMP1.INN	VADC0.G0CH0		ORC4.AIN	USIC1_CH1.DX3E	USIC1_CH1.DX4E	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D			ERU0.2A1
P2.7										ACMP1.INP		VADC0.G1CH1	ORC5.AIN	USIC1_CH1.DX5E		USIC0_CH0.DX5C		USIC0_CH1.DX3D	USIC0_CH1.DX4D		ERU0.3A1
P2.8										ACMP0.INN	VADC0.G0CH1	VADC0.G1CH0	ORC6.AIN			USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C			ERU0.3B1

Functions	Outputs									Inputs											
Pin	**ALT1**	**ALT2**	**ALT3**	**ALT4**	**ALT5**	**ALT6**	**ALT7**	**ALT8**	**ALT9**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P2.9										ACMP0.INP	VADC0.G0CH2	VADC0.G1CH4	ORC7.AIN			USIC0_CH0.DX5A		USIC0_CH1.DX3B	USIC0_CH1.DXB		ERU0.3B0
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1	LEDTS1.COL4	CCU80.OUT30	ACMP0.OUT	USIC0_CH1.DOUT0		CAN.N1_TXD		VADC0.G0CH3	VADC0.G1CH2				USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F		CAN.N1_RXDE	ERU0.2B0
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0	LEDTS1.COL3	CCU80.OUT31	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0		CAN.N1_TXD	ACMP.REF	VADC0.G0CH4	VADC0.G1CH3						USIC0_CH1.DX0E	USIC0_CH1.DX1E	CAN.N1_RXDF	ERU0.2B1
P2.12	BCCU0.OUT3	VADC0.EMUX00	USIC1_CH0.SCLKOUT	USIC1_CH1.SCLKOUT		ACMP2.OUT	USIC1_CH1.DOUT0	LEDTS2.COL6		ACMP3.INN						USIC1_CH0.DX3A	USIC1_CH0.DX4A	USIC1_CH1.DX0C	USIC1_CH1.DX1B		ERU1.3A2
P2.13	BCCU0.OUT4	CCU40.OUT3	USIC1_CH0.MCLKOUT	CCU81.OUT31		VADC0.EMUX01	USIC1_CH1.DOUT0	CCU81.OUT33	CCU41.OUT3	ACMP3.INP						USIC1_CH0.DX5A		USIC1_CH1.DX0D			ERU1.3A3
P3.0	BCCU0.OUT0	USIC1_CH1.DOUT0	USIC1_CH1.SCLKOUT	LEDTS2.COLA	CCU80.OUT21	ACMP1.OUT	USIC1_CH0.SELO1	CCU81.OUT21	CCU41OUT0	BCCU0.TRAPINC	CCU41.IN0AA	CCU41.IN1AA	CCU41.IN2AA	CCU41.IN3AA	CCU81.IN0AA	CCU81.IN1AA	CCU81.IN2AA	USIC1_CH1.DX0E	USIC1_CH1DX1D	CCU81.IN3AA	ERU1.0A1
P3.1	BCCU0.OUT1	USIC1_CH1.DOUT0		LEDTS2.COL0	CCU80.OUT20	ACMP3.OUT	USIC1_CH0.SELO0	CCU81.OUT20	CCU41.OUT1								USIC1_CH0.DX2F	USIC1_CH1.DX0F			ERU1.1A1
P3.2	BCCU0.OUT2	USIC1_CH1.SCLKOUT		LEDTS2.COL1	CCU80.OUT11	ACMP2.OUT	USIC1_CH0.SCLKOUT	CCU81.OUT11	CCU41.OUT2							USIC1_CH0.DX3C	USIC1_CH0.DX4C	USIC1_CH1.DX3D	USIC1_CH1.DX4D		ERU1.2A1
P3.3	BCCU0.OUT5	USIC1_CH0.DOUT0		LEDTS2.COL2	CCU80.OUT10	ACMP0.OUT	USIC1_CH1.SELO0	CCU81.OUT10	CCU41.OUT3							USIC1_CH0.DX0E			USIC1_CH1.DX2A		ERU1.1A3
P3.4	BCCU0.OUT6	USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT	LEDTS2.COL3	CCU80.OUT01	USIC1_CH1.MCLKOUT	USIC1_CH1.SELO1	CCU81.OUT01								USIC1_CH0.DX0F	USIC1_CH0.DX1E		USIC1_CH1.DX2B		ERU1.2A3
P4.1	BCCU0.OUT8	ERU1.PDOUT1	LEDTS2.COL4	ERU1.GOUT1	CCU40.OUT1	ACMP3.OUT	USIC1_CH1.SELO2	CCU81.OUT11	CCU41.OUT1		CCU40.IN1BA	CCU41.IN1AC	CCU80.IN1AU		POSIF1.IN0B	USIC1_CH0.DX5C					
P4.2	BCCU0.OUT4	ERU1.PDOUT2	CCU81.OUT20	ERU1.GOUT2	CCU40.OUT2	ACMP2.OUT	USIC1_CH1.SELO3	CCU81.OUT12	CCU41.OUT2		CCU40.IN2BA	CCU41.IN2AC	CCU80.IN2AU	CCU81.IN1AB	POSIF1.IN1B	USIC1_CH0.DX5D					
P4.3	BCCU0.OUT5	ERU1.PDOUT3	CCU81.OUT21	ERU1.GOUT3	CCU40.OUT3	ACMP0.OUT	USIC1_CH0.SCLKOUT	CCU81.OUT13	CCU41.OUT3		CCU40.IN3BA	CCU41.IN3AC	CCU80.IN3AU		POSIF1.IN2B		USIC1_CH0.DX1B				

Functions	Outputs									Inputs										
Pin	**ALT1**	**ALT2**	**ALT3**	**ALT4**	**ALT5**	**ALT6**	**ALT7**	**ALT8**	**ALT9**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P4.4	BCCU0.OUT0	LEDTS2.LINE0		LEDTS1.COLA	CCU80.OUT00	USIC1_CH0.DOUT0		CCU81.OUT00	CCU41.OUT0			CCU41.IN0AV				USIC1_CH0.DX0C		USIC1_CH1.DX5F			ERU1.0A2
P4.5	BCCU0.OUT8	LEDTS2.LINE1		LEDTS1.COL6	CCU80.OUT01	USIC1_CH0.DOUT0	USIC1_CH0.SCLKOUT	CCU81.OUT01	CCU41.OUT1			CCU41.IN1AV				USIC1_CH0.DX0D	USIC1_CH0.DX1C				ERU1.1A2
P4.6	BCCU0.OUT2	LEDTS2.LINE2	CCU81.OUT10	LEDTS1.COL5	CCU80.OUT10		USIC1_CH0.SCLKOUT	CCU81.OUT02	CCU41.OUT2			CCU41.IN2AV		CCU81.IN0AB			USIC1_CH0.DX1D				ERU1.2A2
P4.7	BCCU0.OUT5	LEDTS2.LINE3	CCU81.OUT11	LEDTS1.COL4	CCU80.OUT11		USIC1_CH0.SELO0	CCU81.OUT03	CCU41.OUT3			CCU41.IN3AV					USIC1_CH0.DX2A				ERU1.0A3
P4.8	BCCU0.OUT7	LEDTS2.LINE4	LEDTS2.COL3	LEDTS1.COL3	CCU80.OUT30	CCU40.OUT0	USIC1_CH0.SELO1	CCU81.OUT30	CAN.N1_TXD		CCU40.IN0AV	CCU41.IN0BA					USIC1_CH0.DX2B			CAN.N1_RXDC	
P4.10		LEDTS2.LINE6	LEDTS2.COL1	LEDTS1.COL1	CCU80.OUT00	CCU40.OUT2	USIC1_CH0.SELO3	CCU81.OUT32	CCU81.OUT00	BCCU0.TRAPIND	CCU40.IN2AV	CCU41.IN2BA		CCU81.IN3AB			USIC1_CH0.DX2D	USIC1_CH1.DX5A			

2.8.2 Port Pins for Boot Modes

Port functions can be overruled by the boot mode selected. The type of boot mode is selected via BMI (Refer to latest reference manual for the complete description at Infineon website: www.infineon.com. At the time of creation of this document, latest version can be found here: XMC1400 Reference Manual). Table 15 shows the port pins used for the various boot modes.

Table 15 XMC1404 Port Pin for Boot Modes in IMD70xA

XMC1404 Pin	IMD70xA Pin	Boot	Boot Description
P0.14	GPIO15_DBG0/P0.14	SWDIO_0	Debug mode (SWD)
		SPD_0	Debug mode (SPD)
		RX/TX	ASC BSL half-duplex mode
		RX	ASC BSL full-duplex mode
		RX	CAN BSL mode
P0.15	GPIO16_DBG1/P0.15	SWDCLK_0	Debug mode (SWD)
		TX	ASC BSL full-duplex mode
		TX	CAN BSL mode
P4.6	GPIO2/P4.6	HWCON0	Boot Pins (Boot from pins mode must be selected)
P4.7	GPIO3/P4.7	HWCON1	

2.9 XMC1404 Chip Identification Number

The Chip Identification Number in XMC1404 allows embedded software to identify the device and its features. It is an 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location: 1000 0F00$_H$ (MSB) - 1000 0F1B$_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 16 Device Identification Number

Derivative Part Number	XMC1404 Flash Size	DVDD Supply Voltage (V)	Value	Marking
IMD700A - Q064x128	128kB	3.3	2700100A 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083H	AA
IMD701A - Q064x128	128kB	5.0	2701100A 07FF00FF 1E071FF7 30BFF00F 00000D00 00001000 00021000 10204083H	AA

3 Drives Optimized Microcontroller Features: XMC1404 Overview

IMD70xA integrates a fully programmable XMC1404 device. Following are the main features of this device:

ARM® Cortex-M0 32 bits microcontroller (XMC1404)

- **CPU Subsystem**
  - 32 bit ARM® Cortex-M0 (core clock 48MHz)
  - MATH Co-Processor (96MHz) for optimized 32 bit division and 24 bit trigonometric calculations
  - 0.84 DMIPS/MHz (Dhrystone 2.1) at 48 MHz
  - Nested Vectored Interrupt Controller (NVIC) with 64 interrupt nodes
  - Internal slow and fast oscillators without the need of PLL
  - Real time clock module
  - Window watchdog
  - Up to 128kB of Flash (with ECC) and 16kB of RAM (with parity)
  - Internal oscillator
- **Serial Communication Modules**
  - Four USIC channels, each of them configurable as UART, SPI, IIC and more
  - MultiCAN module (2 CAN nodes)
- **Analog Frontend Peripherals**
  - 12 bit A/D Converters (up to 12 analog inputs), 2 sample and hold stages up to 1.1MSamples/s with adjustable gain
  - 4 fast, general purpose analog comparators
- **Industrial Control Peripherals**
  - 2x4 16-bit 96 MHz CCU4 timers for signal monitoring and PWM
  - 2x4 16-bit 96 MHz CCU8 timers for complex PWM, complementary high/low side switches and 3 phase inverter control
  - 2x POSIF for Hall and quadrature encoders, motor positioning
- **On-Chip Debug Support**
  - 4 hardware breakpoints
  - ARM serial wire debug, single-pin debug interfaces
- **Programming Support**
  - Single-pin bootloader
  - Secure bootstrap loader SBSL (optional)

Note: Refer to XMC1400 Reference Manual for full description of the XMC1400 including register map and descriptions. For latest version, refer to Infineon website (www.infineon.com)

4 MOTIX™ 6EDL7141 Three Phase Integrated Smart Gate Driver

6EDL7141 main core block is comprised of a complete three phase gate driver optimized for motor control applications. This gate driver is a floating driver capable of driving with configurable slew rate and driving voltage, a 3 phase 2 level inverter with up to 1.5A of both sourcing and sinking peak currents.

Programmable charge pumps supply the gate drivers ensuring 100% duty cycle and configurable driving voltage for maximum optimization of the gate driver.

Numerous protections are included to ensure safe operation of the gate driver system under stress conditions including a best in class phase node (V_{SHx}) tolerance to negative voltage spikes (see Absolute Maximum Ratings table). This is of great importance for example during high side MOSFET turn off transition.

Configurations and settings are shared by all three half bridge drivers. This section describes the following features of the integrated three phase gate driver:

- PWM Modes
- Gate Driver Architecture
- Slew Rate Control
- Gate Driver Voltage Programmability
- Charge Pump Configurations
- Gate Driver and Charge Pump Protections

4.1 PWM Modes

MOTIX™ 6EDL7141 implements additional intelligence that allows the user to simplify the PWM generation on the XMC1404 side. That together with integrated protection features results in a highly robust and faster development for drives applications. An intelligent dead time unit will ensure no shoot through happens at any condition. A highly configurable braking mode provides safe reaction to motor or system events.

Following PWM modes can be selected via bitfield PWM_MODE:

1. 6PWM
2. 3PWM
3. 1PWM and commutation pattern
4. 1PWM with Hall sensor commutation

Note: Given the interconnection between 6EDL7141 and XMC1404, PWM Mode '1PWM with Hall sensors inputs' as provided in standalone 6EDL7141 is not possible. However, XMC1404 can create a copy of the Hall sensor inputs via firmware and benefit from some of the 6EDL7141 provided features like dead time insertion or rotor locked detection if necessary. Possible delays or mismatches are user (firmware) responsibility.

Note: It is possible to use only one or two phases instead of the 3 phases, like for instance in a full bridge configuration. In such case, it is recommended to keep INHx and INLx signals of the unused phases shorted to DGND and the GHx, GLx, SHx and SLx signals open.

The PWM signals need to be generated in pins P1.0, P1.1, P3.0, P3.1, P3.2, P3.3 according to Figure 3, by XMC1404 timer CCU8 which is a dedicated PWM timer for motor control. Thanks to the alternate functions, both CCU80 and CCU81 are possible to be used providing further flexibility in terms of connectivity, as an example, input signals for both units are different, so start, stop, load or other timer commands can be triggered by

different sources depending on the unit selection. A CTRAP function (setting to passive all timer output) can be connected via GPIOP14/P0.12 to input section of CCU80 timer as well as to other CCU4 timers.

Following subsections provide further details on each of the PWM modes and sub-modes.

4.1.1 PWM with 6 Independent Inputs – 6PWM

When the PWM_MODE register in 6EDL7141 is set to b'0 then the device is configured for 6 independent PWM inputs. In this mode XMC1404 must provide 3 pairs of complementary PWM signals with dead time between high side and low side PWM. A minimum dead time will be observed for safety reasons in the gate driver, in order to avoid strong shoot through condition.

nBRAKE pin can be used for braking the motor in a controlled manner. See 4.1.6 for more information on braking modes.

Table 17 shows the truth table for 6PWM mode while Figure 19 shows a system diagram for this mode.

Table 17 Truth table for 6PWM mode.

INHx	INLx	nBRAKE	GHx	GLx	SHx
1	1	1	LOW	LOW	High-Z
1	0	1	HIGH	LOW	HIGH
0	1	1	LOW	HIGH	LOW
0	0	1	LOW	LOW	High-Z
X	X	0	Brake cfg.	Brake cfg.	Brake cfg.

Note: X means any level

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

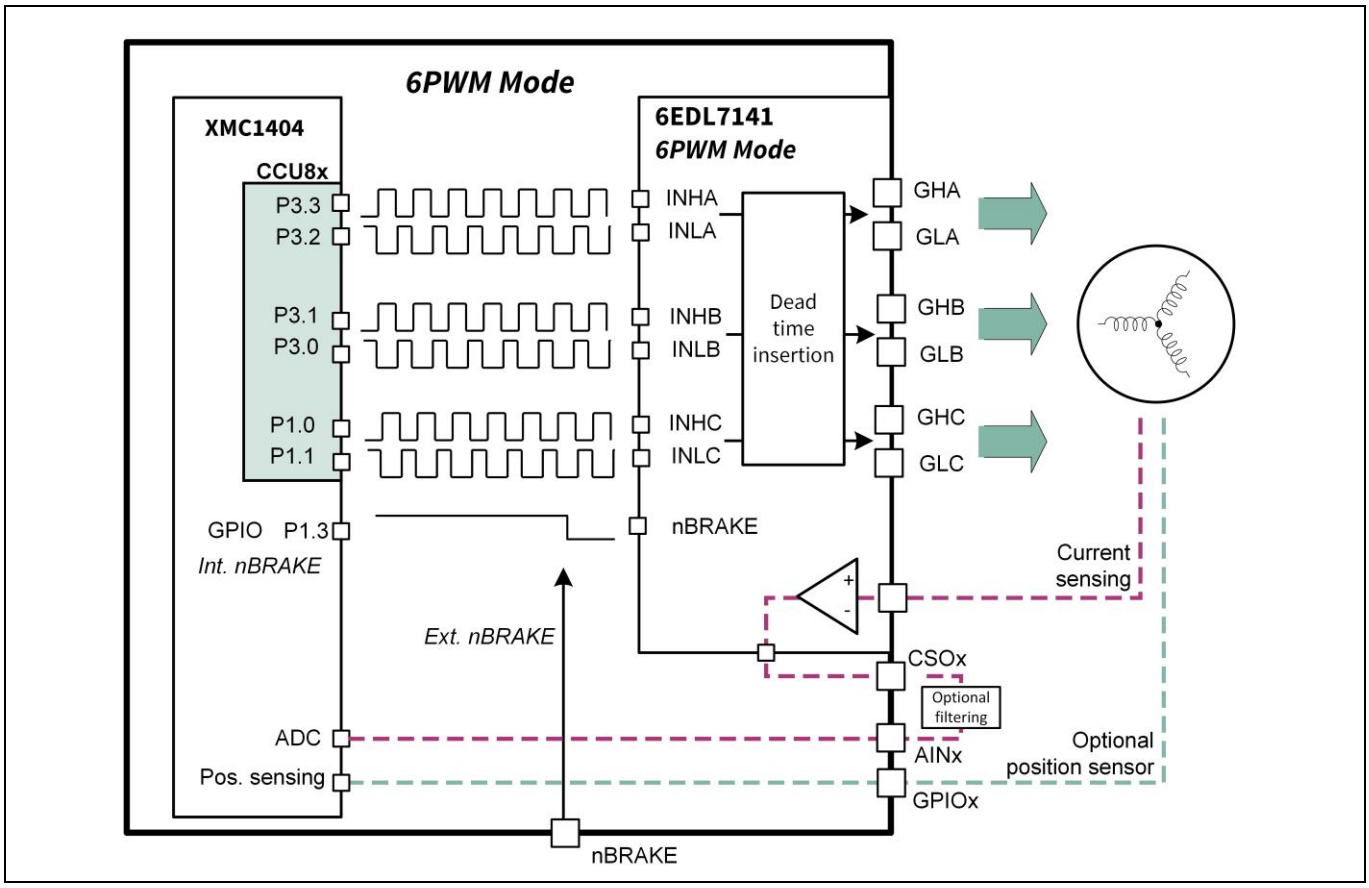

Figure 19 6PWM mode scheme

4.1.2 PWM with 3 Independent Inputs – 3PWM

MOTIX™ 6EDL7141 can be configured to 3PWM mode by setting PWM_MODE bitfield to value b'001. In such case, only 1 PWM signal (high side) per phase is necessary. The device will automatically generate the low side signals according to Table 18 and will insert a configurable dead time. Dead time is independently programmable for high to low (fall of phase node voltage) and low to high (rise of phase voltage) transitions through bitfields DT_RISE and DT_FALL.

INLx signals are ignored in this mode.

nBRAKE pin can be used for braking the motor. See 4.1.6 for more information on braking modes.

Figure 20 depicts a system diagram for this PWM mode.

Table 18 Truth table for 3PWM mode.

INHx	INLx	nBRAKE	GHx	GLx	SHx
1	0	1	HIGH	LOW	HIGH
0	0	1	LOW	HIGH	LOW
X	1	1	LOW	LOW	High-Z
X	X	0	Brake cfg.	Brake cfg.	Brake cfg.

Note: X means any level

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

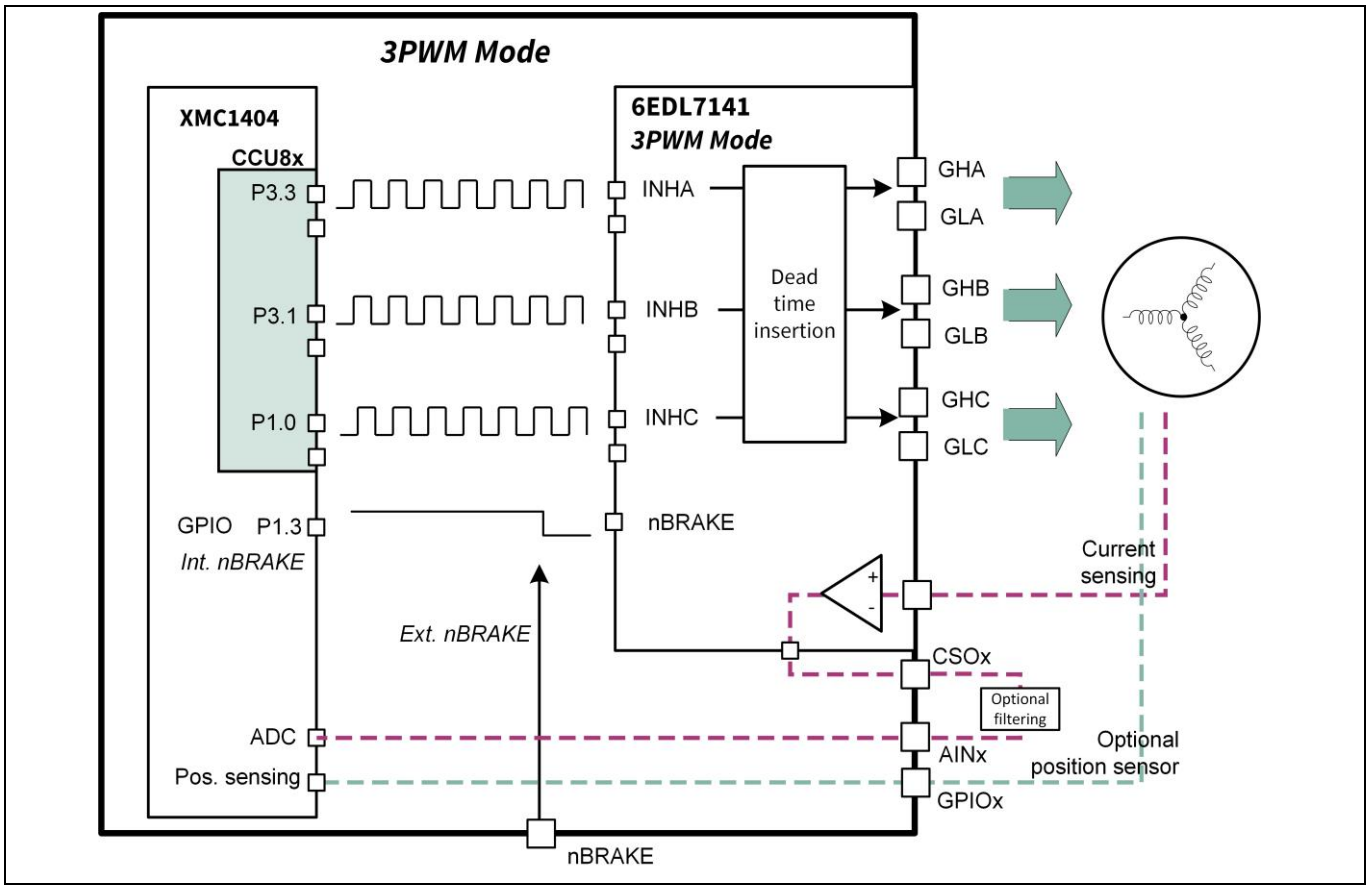

Figure 20 3PWM mode scheme

4.1.3 PWM with 1 Input and Commutation Pattern – 1PWM

When the PWM_MODE register is set to b'010 then the PWM section in 6EDL7141 is configured to 1PWM mode. In this case, the duty cycle and frequency of signal INHA is used to determine the duty cycle (or amplitude) and the frequency of the PWM outputs generated. The rest of inputs are captured to decide the commutation pattern or state of the outputs. INHC signal can be used to implement 12 step trapezoidal commutation. Dead time is automatically inserted according to programmed values in bitfields DT_RISE and DT_FALL.

Figure 21 shows a schematic diagram of 1PWM mode.

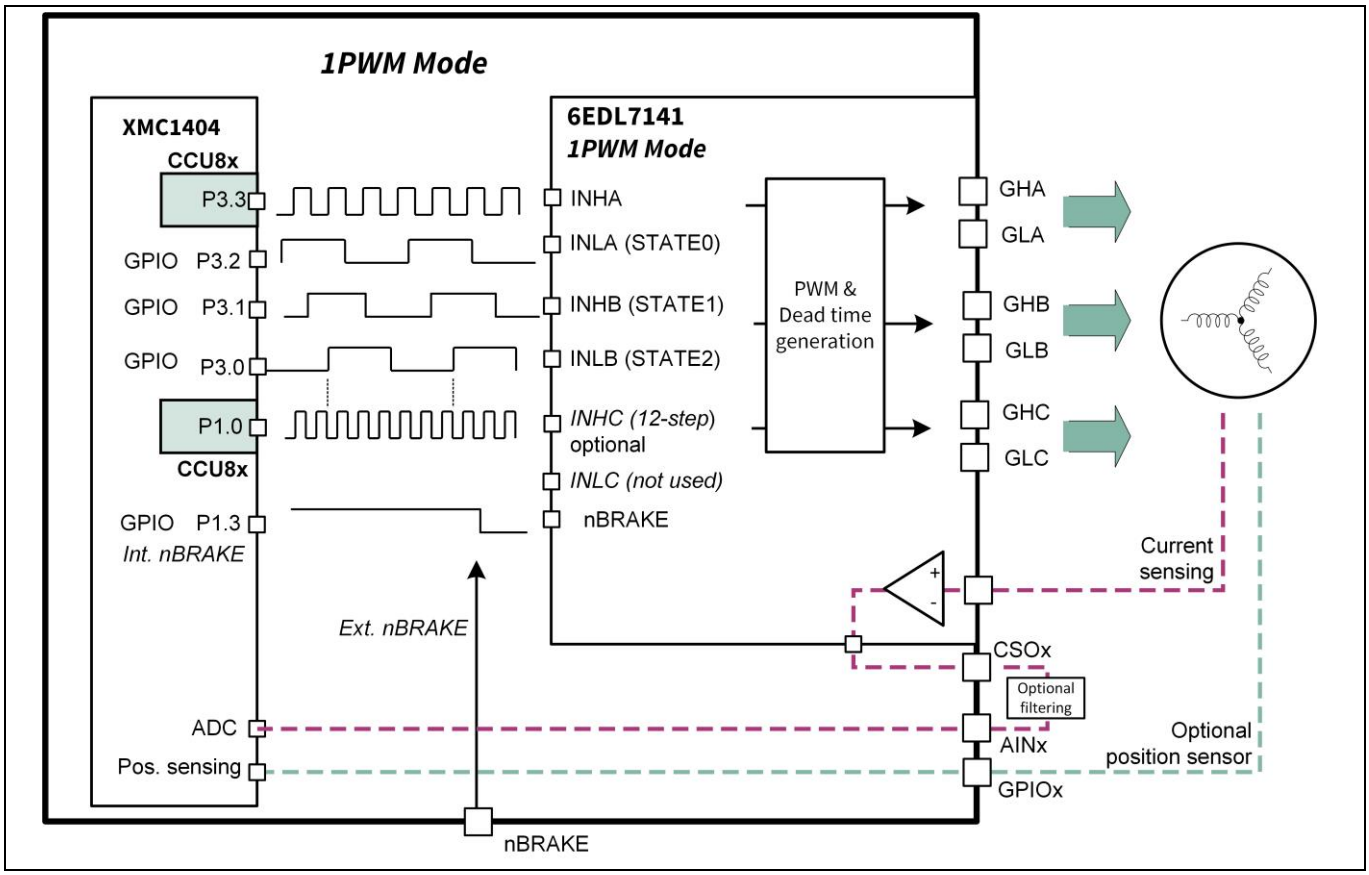

Figure 21 1PWM mode scheme

Additionally, the user has the option to select between two main commutation schemes programmable via register bitfield PWM_FREEW_CFG:

- **Diode freewheeling** – bitfield PWM_FREEW_CFG =b'1: in this case, the freewheeling current will flow through the low side MOSFETs body diodes. The truth table for this mode is shown in Table 19.
- **Active freewheeling** – bitfield PWM_FREEW_CFG =b'0: in this case the low side MOSFETs will be switched synchronously to reduce conduction losses on the body diode conduction. The truth table for this mode is shown in Table 20.Note:

12 Step Trapezoidal Commutation

Input INHC can be optionally used to create a 12 step trapezoidal or block commutation. This method energizes up to two phases at the same time in contrast to 6 step, where only one is active at any time. In 12 step trapezoidal commutation, torque ripple is improved and the angle created between stator and rotor flux vectors can be controlled within 30 degree accuracy instead of 60degree in 6 step trapezoidal commutation. This method improves motor efficiency and torque ripple, however requires additional position information. This information can be processed by a the integrated XMC1404 to produce signals INHA, INLA, INHB, INLB and INHC according to Table 19 or Table 20. As can be seen, from a system perspective, the INHC signal must toggle at every 30degree rotation (electrical).

In case the INHC signal is not toggled, the device will apply the commutation as shown in to Table 19 or Table 20. As an example, if INHC is left low, a classic 6 step trapezoidal commutation pattern will be produced. In case INHC is pulled high, the pattern will show a 30 degree advanced with respect to a standard 6 step trapezoidal commutation. The user can use this variants or toggle the INHC pin every 30 degree of rotation to create a 12 step commutation pattern.

nBRAKE pin can be used for braking the motor. See 4.1.6 for more information on braking modes.

Here is a summary of inputs and output functionalities:

- INHA - PWM input, defines PWM output duty cycle and frequency
- INLA, INHB, INLB - Provide timing for modulation pattern changes
- INHC – Signalizes 12 step states. Must toggle every electrical 30degree
- INLC – This input is ignored in this mode. Recommended pull down.
- nBRAKE signal – When active, will force the motor to brake.
- GHA, GLB, GHB, GLB, GHC, GLC – Complementary PWM Output signals

Table 19 shows the possible states for this PWM mode using diode freewheeling while Table 20 shows the states in case of active freewheeling.

Table 19 Truth table for 1PWM mode with diode freewheeling.

	INPTUS									OUTPUTS		
State	**INLA, INHB, INLB,**	**INHC**	**nBRAKE**	**GHA**	**GLA**	**GHB**	**GLB**	**GHC**	**GLC**	**SHA**	**SHB**	**SHC**
AB	011	0	1	PWM	LOW	LOW	HIGH	LOW	LOW	HIGH	LOW	-
AB_CB	*010*	*1*	*1*	*PWM*	*LOW*	*LOW*	*HIGH*	*PWM*	*LOW*	*HIGH*	*LOW*	*HIGH*
CB	010	0	1	LOW	LOW	LOW	HIGH	PWM	LOW	-	LOW	HIGH
CB_CA	*110*	*1*	*1*	*LOW*	*HIGH*	*LOW*	*HIGH*	*PWM*	*LOW*	*LOW*	*LOW*	*HIGH*
CA	110	0	1	LOW	HIGH	LOW	LOW	PWM	LOW	LOW	-	HIGH
CA_BA	*100*	*1*	*1*	*LOW*	*HIGH*	*PWM*	*LOW*	*PWM*	*LOW*	*LOW*	*HIGH*	*HIGH*
BA	100	0	1	LOW	HIGH	PWM	LOW	LOW	LOW	LOW	HIGH	-
BA_BC	*101*	*1*	*1*	*LOW*	*HIGH*	*PWM*	*LOW*	*LOW*	*HIGH*	*LOW*	*HIGH*	*LOW*
BC	101	0	1	LOW	LOW	PWM	LOW	LOW	HIGH	-	HIGH	LOW
BC_AC	*001*	*1*	*1*	*PWM*	*LOW*	*PWM*	*LOW*	*LOW*	*HIGH*	*HIGH*	*HIGH*	*LOW*
AC	001	0	1	PWM	LOW	LOW	LOW	LOW	HIGH	HIGH	-	LOW
AC_AB	*011*	*1*	*1*	*PWM*	*LOW*	*LOW*	*HIGH*	*LOW*	*HIGH*	*HIGH*	*LOW*	*LOW*
Align	111	X	1	PWM	LOW	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Stop	000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
Brake	XXX	X	0	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.

Note: X means any level

Note: SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage according to PWM signals. '-' represents floating state, meaning both high side and low side MOSFETs are OFF

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

Table 20 Truth table for 1PWM mode with active freewheeling.

	INPTUS									OUTPUTS		
State	INLA, INHB, INLB,	INHC	nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
AB	011	0	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
AB_CB	*010*	*1*	*1*	PWM	!PWM	LOW	HIGH	PWM	!PWM	HIGH	LOW	HIGH
CB	010	0	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
CB_CA	*110*	*1*	*1*	LOW	HIGH	LOW	HIGH	PWM	!PWM	LOW	LOW	HIGH
CA	110	0	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
CA_BA	*100*	*1*	*1*	LOW	HIGH	PWM	!PWM	PWM	!PWM	LOW	HIGH	HIGH
BA	100	0	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
BA_BC	*101*	*1*	*1*	LOW	HIGH	PWM	!PWM	LOW	HIGH	LOW	HIGH	LOW
BC	101	0	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
BC_AC	*001*	*1*	*1*	PWM	!PWM	PWM	!PWM	LOW	HIGH	HIGH	HIGH	LOW
AC	001	0	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
AC_AB	*011*	*1*	*1*	PWM	!PWM	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Align	111	X	1	PWM	!PWM	LOW	HIGH	LOW	HIGH	HIGH	LOW	LOW
Stop	000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
Brake	XXX	X	0	Brake cfg.	Brake cfg	Brake cfg	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.

Note: X means any level

Note: SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. '-' is floating state, meaning both high side and low side MOSFETs are OFF.

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z.

4.1.4 PWM with 1 Input and Commutation with Hall Sensor Inputs – 1PWM with Hall Sensors

MOTIX™ 6EDL7141 integrates three Hall sensor comparators to detect pattern of movement in the motor. This can be used for rotor locked detection but can also be utilized to drive the PWM commutation pattern automatically. In order to use this mode, user could use Hall sensor inputs connected to XMC1404 and replicate those signals, e.g. via GPIO handling in firmware, into 6EDL7141 inputs. This will enable usage of 6EDL7141 logic for PWM pattern generation as well as locked rotor detection.

To enable this PWM_MODE bitfield needs to be configured to value b'011.The truth table presented in Table 21 dictates the commutation pattern. In this mode, Hall sensor inputs decide the switching pattern of the PWM output signals. The duty cycle and frequency of the output signals is determined by INHA duty cycle and frequency.

Dead time is inserted automatically according to programmed values in DT_RISE and DT_HALL.

In a similar way as in other PWM modes, the user has the option to select between two main commutation schemes programmable via bitfield PWM_FREEW_CFG in PWM_CFG register: diode and active freewheeling. No

truth table is shown for diode mode. This can be constructed by substituting “!PWM” cells in Table 21 by “LOW”.

Similarly to other PWM modes, nBRAKE pin can be used for braking the motor. See 4.1.6 for more information on braking modes.

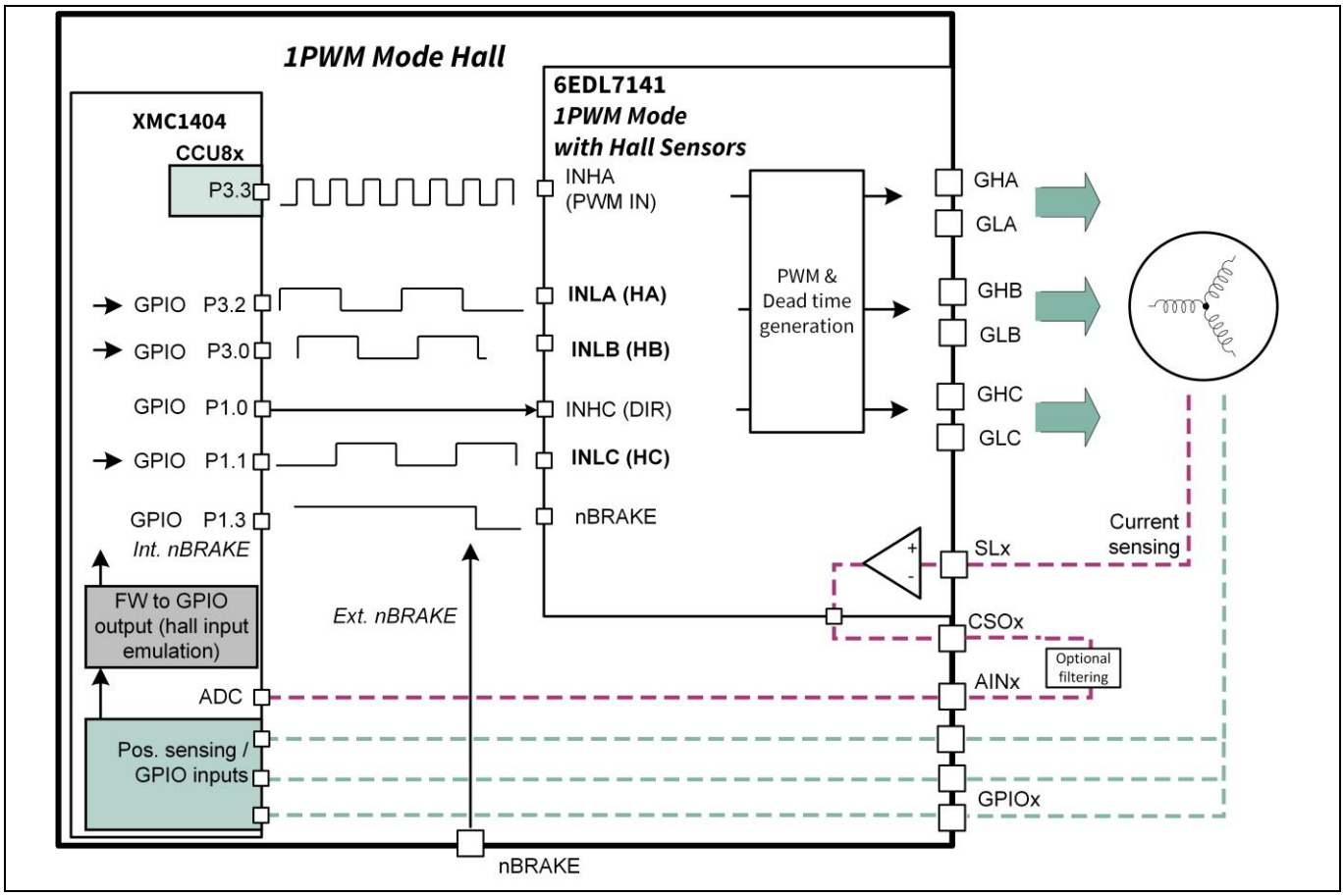

Figure 22 1PWM mode with hall sensors. Self-controlled pattern switching

Table 21 Truth table for 1 PWM mode with active freewheeling.

INPUTS			OUTPUTS								
INLx [A,B,C]	INHC-Dir	nBRAKE	GHA	GLA	GHB	GLB	GHC	GLC	SHA	SHB	SHC
101	1	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
100	1	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
110	1	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
010	1	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
011	1	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
001	1	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
101	0	1	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
100	0	1	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
110	0	1	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
010	0	1	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW

INPUTS			OUTPUTS								
INLx [A,B,C]	**INHC-Dir**	**nBRAKE**	**GHA**	**GLA**	**GHB**	**GLB**	**GHC**	**GLC**	**SHA**	**SHB**	**SHC**
011	0	1	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
001	0	1	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
XXX	X	0	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.
111	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
000	X	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-

Note: X means any level. XXX means any other combination on inputs not shown

Note: Grey cells represent forbidden states and should be avoided

Note: SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. '-' represents floating state, meaning both high side and low side MOSFETs are OFF

Note: For diode freewheeling mode, substitute "!PWM" cells by "LOW"

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

These are the signals functionality for this mode:

- INHA - PWM input, defines duty cycle and frequency of PWM output signals
- INLA, INLB, INLC - Hall Sensor Inputs (HA, HB, HC) will define the PWM output pattern depending on motor position.
- nBRAKE signal – when active, the device will force a brake event.
- INHC - Direction control. Provided by a microcontroller, will define direction of motor rotation.
- GHA, GLA, GHB, GLB, GHC, GLC – PWM output signals, high side and low sides.

A schematic representation of the commutation states is presented in Figure 23.

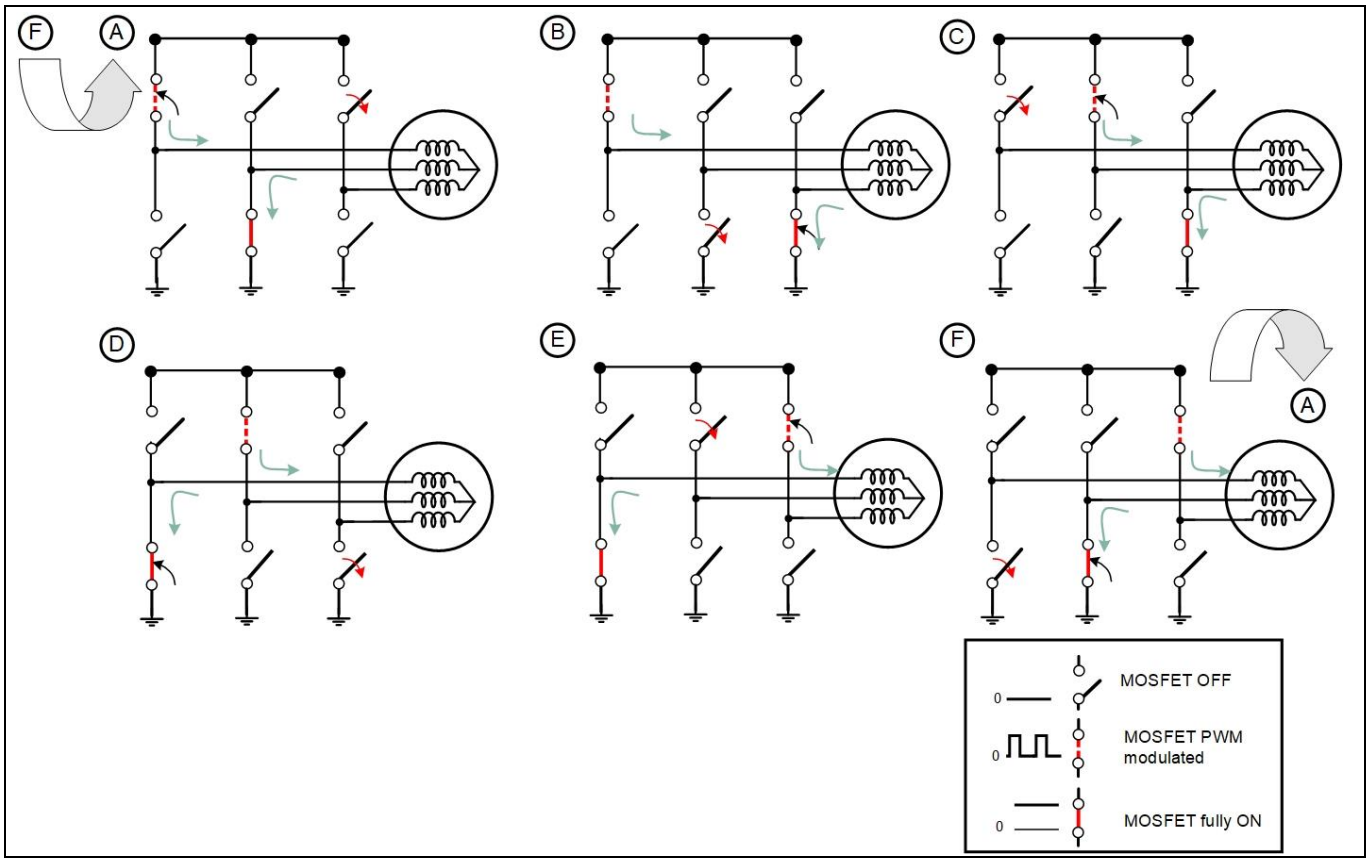

Figure 23 **6 states switching overview. Diode freewheeling mode is represented here for simplification. Single direction considered.**

4.1.5 PWM with 1 Input and Commutation with Hall Sensor Inputs and Alternating Recirculation – 1PWM with Hall Sensors and Alternating Recirculation

Thermal management in power tools systems is a key factor for achieving higher power densities. A more advance thermal management might allow smaller heat sink components or smaller PCB area. This PWM mode focuses on distributing the MOSFET stress more evenly between all MOSFETs in the inverter. This concept alternates the recirculation of the freewheeling current between high side and low side MOSFETs. This is achieved by extending the truth table shown in Table 21 into Table 22.

On the first rotation (electrical), the inverter will recirculate the current through the high side MOSFETS (PWM modulated MOSFET) and the low side MOSFET will be always ON. In the second electrical rotation, the low side MOSFETs will recirculate the freewheeling current (PWM modulated MOSFET), and therefore, the high side is the one fully ON. This cycle repeats in further rotations. A graphical representation for the switching states is presented in Figure 24. In this figure, states A to F represent high side modulation while states G to L represent the low side modulation. The state machine will return to state A after state L, starting over again the cycle.

PWM_FREEW_CFG configures this mode as well either as diode or active freewheeling. No truth table is shown for diode mode. This can be constructed by substituting “!PWM” cells with LOW in Table 22.

Table 22 Truth table for 1 PWM mode with active freewheeling and alternating recirculation

INPUTS			OUTPUTS								
INLx [A,B,C]	**nBRAKE**	**Fully ON**	**GHA**	**GLA**	**GHB**	**GLB**	**GHC**	**GLC**	**SHA**	**SHB**	**SHC**
INHC (Dir)=1											
101	1	Low side	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
100	1	Low side	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
110	1	Low side	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
010	1	Low side	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
011	1	Low side	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
001	1	Low side	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
101	1	High side	HIGH	LOW	LOW	LOW	!PWM	PWM	HIGH	-	LOW
100	1	High side	LOW	LOW	HIGH	LOW	!PWM	PWM	-	HIGH	LOW
110	1	High side	!PWM	PWM	HIGH	LOW	LOW	LOW	LOW	HIGH	-
010	1	High side	!PWM	PWM	LOW	LOW	HIGH	LOW	LOW	-	HIGH
011	1	High side	LOW	LOW	!PWM	PWM	HIGH	LOW	-	LOW	HIGH
001	1	High side	HIGH	LOW	!PWM	PWM	LOW	LOW	HIGH	LOW	-
INHC (Dir)=0											
101	1	Low side	LOW	HIGH	LOW	LOW	PWM	!PWM	LOW	-	HIGH
100	1	Low side	LOW	LOW	LOW	HIGH	PWM	!PWM	-	LOW	HIGH
110	1	Low side	PWM	!PWM	LOW	HIGH	LOW	LOW	HIGH	LOW	-
010	1	Low side	PWM	!PWM	LOW	LOW	LOW	HIGH	HIGH	-	LOW
011	1	Low side	LOW	LOW	PWM	!PWM	LOW	HIGH	-	HIGH	LOW
001	1	Low side	LOW	HIGH	PWM	!PWM	LOW	LOW	LOW	HIGH	-
101	1	High side	!PWM	PWM	LOW	LOW	HIGH	LOW	LOW	-	HIGH
100	1	High side	LOW	LOW	!PWM	PWM	HIGH	LOW	-	LOW	HIGH
110	1	High side	HIGH	LOW	!PWM	PWM	LOW	LOW	HIGH	LOW	-
010	1	High side	HIGH	LOW	LOW	LOW	!PWM	PWM	HIGH	-	LOW
011	1	High side	LOW	LOW	HIGH	LOW	!PWM	PWM	-	HIGH	LOW
001	1	High side	!PWM	PWM	HIGH	LOW	LOW	LOW	LOW	HIGH	-
XXX	0	X	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.	Brake cfg.
111	1	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-
000	1	1	LOW	LOW	LOW	LOW	LOW	LOW	-	-	-

Note: X means any level. Grey cells represent forbidden states and should be avoided

Note: SHx when HIGH means that SHx pin is switching between GND and the DC bus voltage or battery voltage. '-' represents floating state, meaning both high side and low side MOSFETs are OFF

Note: For diode freewheeling mode, substitute "!PWM" cells by "LOW"

Note: Brake function can be configured to switch on all low side MOSFETs, all high side MOSFETs, alternate between these two options or set all outputs to high Z

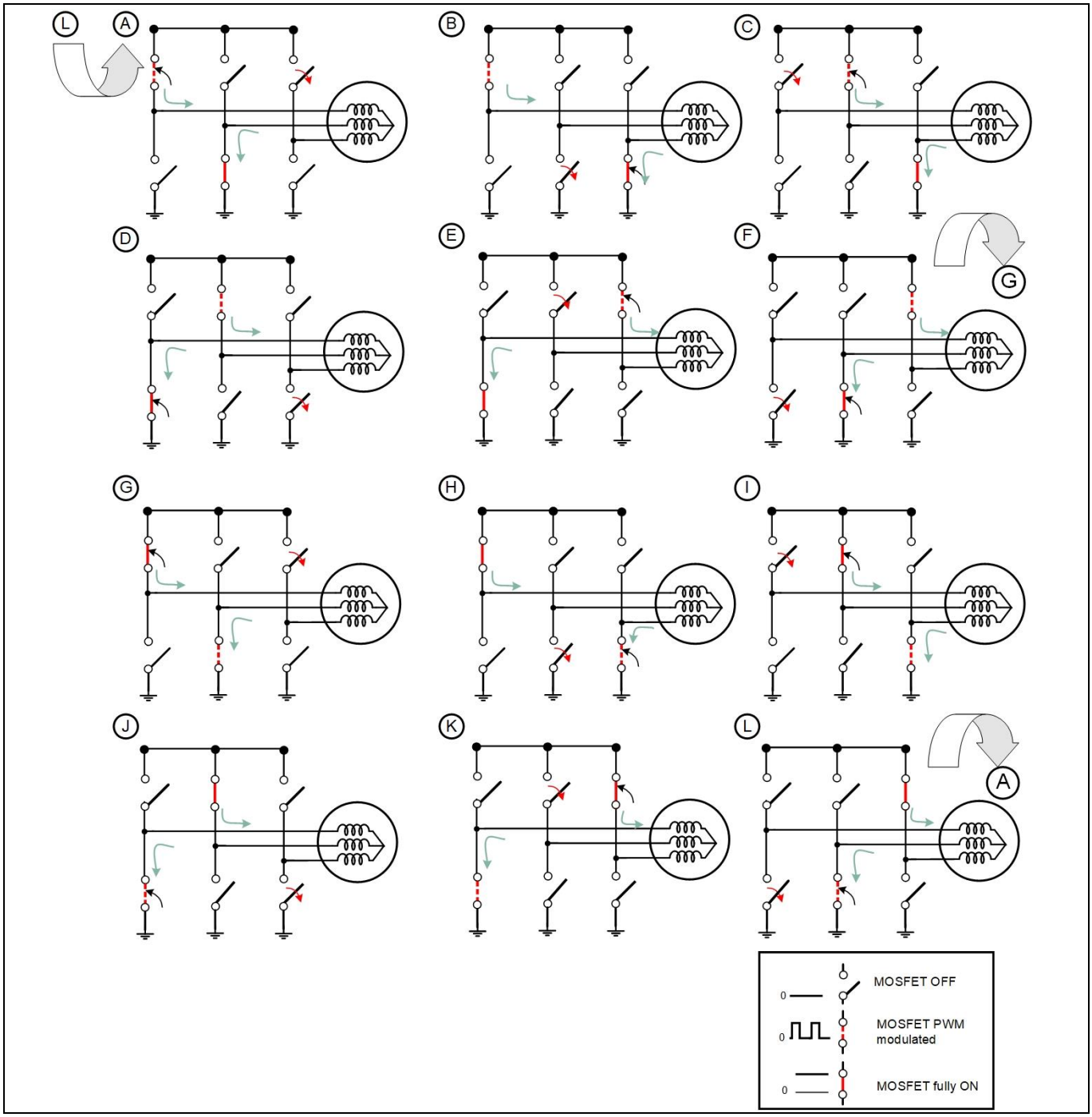

Figure 24 12 states switching overview for alternating recirculation. 6 new states are included (G to L) compared to other 1PWM modes. Diode clamping is represented here for simplification. Single direction considered

4.1.6 PWM Braking Modes

In all PWM modes presented in section 4.1, the device can go into a controlled braking mode. This braking mode will drive PWM signals in a way that the motor goes to a safe state in a controlled manner. This is of critical importance for some power tools applications where a sudden or uncontrolled braking can destroy elements of the tool or become a hazard to the user safety. Following events can trigger the braking action:

- Pull down of pin nBRAKE

- Overcurrent protection (OCP) fault on current sense amplifiers -programmable
- Watchdog timer fault-programmable

From them, pin nBRAKE is the only that can be actively used by, for example an additional microcontroller to start a braking event. All other 3 are the reaction to a fault-detection.

Pin nBRAKE shall be high for normal operation of the motor. However, as soon as low level is detected in it, the gate driver logic will activate high side MOSFETs or low side MOSFETs therefore braking the motor actively.

Braking circuitry can be configured as illustrated in Figure 25 in the following modes by programming bitfield BRAKE_CFG in register PWM_CFG:

- **Low side MOSFET braking**: upon a braking event, all low side MOSFET will be activated and all high side MOSFET switched off.
- **High side MOSFET braking**: upon a braking event, all high side MOSFET will be activated and all low side MOSFET switched off
- **Alternate braking mode**: upon every new braking event, the system alternates between high side MOSFET braking and low side MOSFET braking. With alternate braking, stress on MOSFETs is distributed equally, therefore improving system robustness.
- **Non-power braking**-high impedance (high Z) outputs: upon a braking event all switches are forced to high Z mode. Currents present in motor windings will recirculate through MOSFET body diodes or other available structures in the inverter. This mode is recommended if a MOSFET short occurs in the inverter.

In IMD70xA, XMC1404 can modify brake related bitfields during run time of the system to adapt to given conditions.

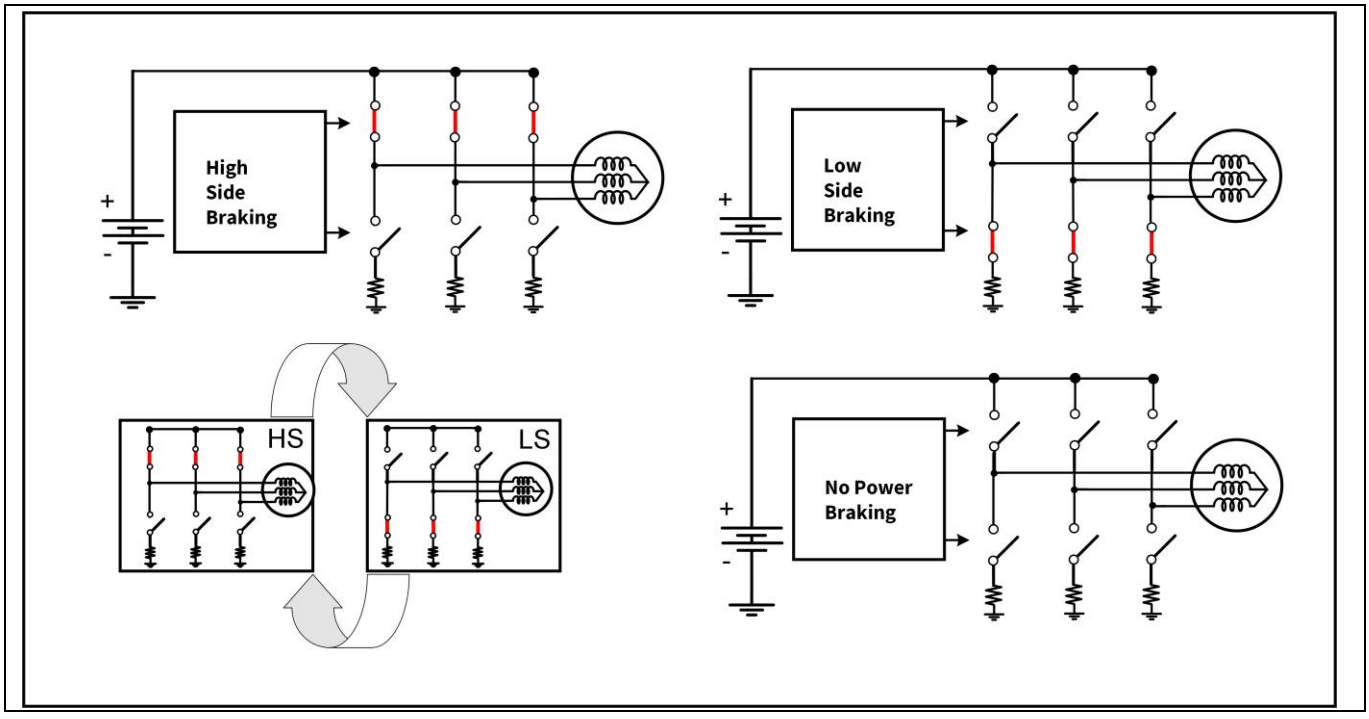

Figure 25 System overview for the different braking modes supported

Before the braking action starts, the gate driver prepares the inverter as fast as possible for a safe braking. Depending on the inverter state at the moment of the braking request, the device will need to switch off some MOSFETs and insert dead times. For example, if the braking signal arrives when phase A is, high side switched-off and low side switched-on, and assuming a high side braking configuration, then will immediately switch off

the low side MOSFET, insert the configured dead time and finally switch on the high side MOSFET of phase A with the rest of high side MOSFETs.

4.1.6.1 Double nBRAKE Path

During normal operation (after UVLO DVDD), the pin nBRAKE is an input (inverted logic) that can be pulled down to initiate a brake event, bringing the motor to a standstill in a controlled way. If the pin is set high, the PWM will resume and propagate normally the PWM inputs to the outputs. There are two sources for activating the brake events in IMD70xA:

- XMC1404 internal connection (P1.3--> nBRAKE): integrated XMC1404 can toggle the GPIO to activate or deactivate the braking action.
- IMD70xA pin 24 (nBRAKE): an external source like another controller or some logic, can trigger in parallel the braking event.

This is done to support increased flexibility in the braking scheme. Internally, both sources are electrically connected. A possible system diagram making use of the double braking path is shown Figure 26.

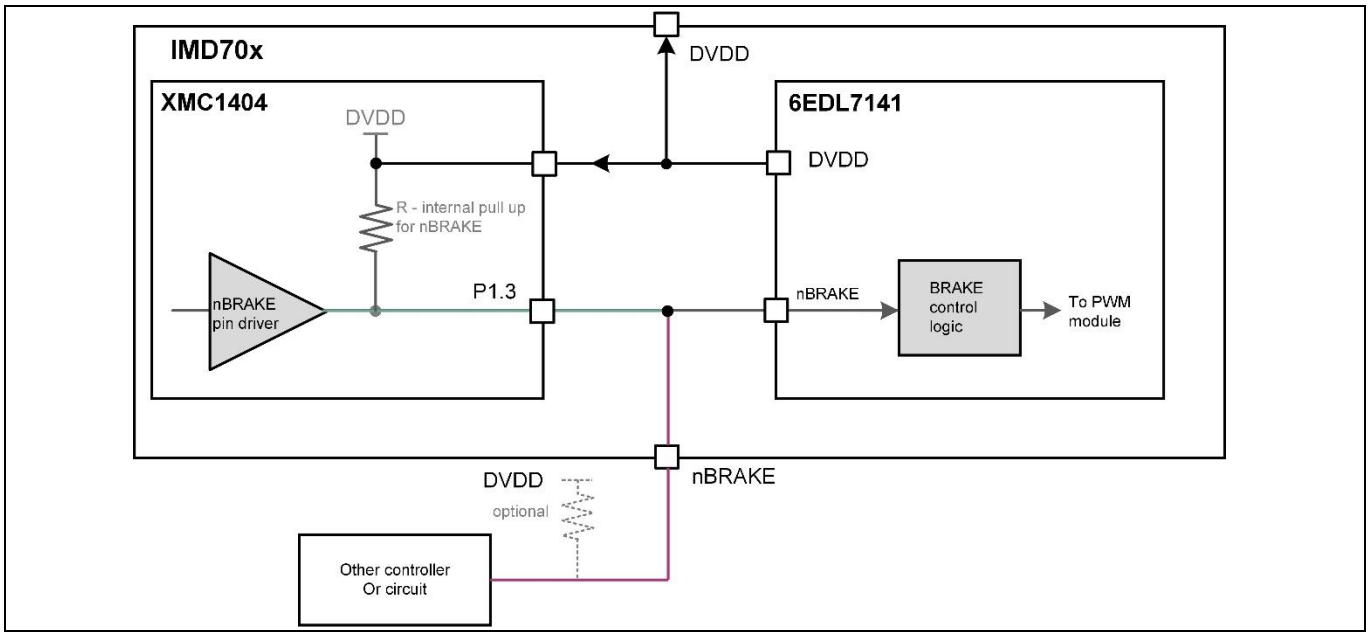

Figure 26 nBRAKE double path pin usage example: internal via XMC1404 controller P1.3 pin, and external via pin nBRAKE

4.1.7 Dead Time Insertion

The PWM unit in 6EDL7141 inserts automatically a dead time between complementary signals (GHx –GLx). DT_RISE bitfield defines the dead time period for rising transition (of phase node voltage) while DT_FALL defines independently the period for the falling transition. A minimum dead time (see Electrical Characteristics table for detailed values and conditions) will always be observed to avoid strong shoot through condition.

Figure 27 shows a detailed signal diagram of a 1PWM mode dead time insertion including the timing definitions. A propagation time (t_{PROP_HS} and t_{PROP_LS}) elapses between the input signal and the actual gate driver output signals. These timing definitions are applicable to all other PWM modes.

Dead time and slew rate control features are designed in a safe way so that a change in slew rate will update in a synchronous manner to the PWM switching. This hinders any possible shoot through during the possible update of the slew rate during operation due to miss-alignment of timings.

Note: The application software, must ensure that dead time is sufficient for the slew rate configuration and the MOSFETs selection. Current sense amplifier OCP can be used to detect excessive current in the system.

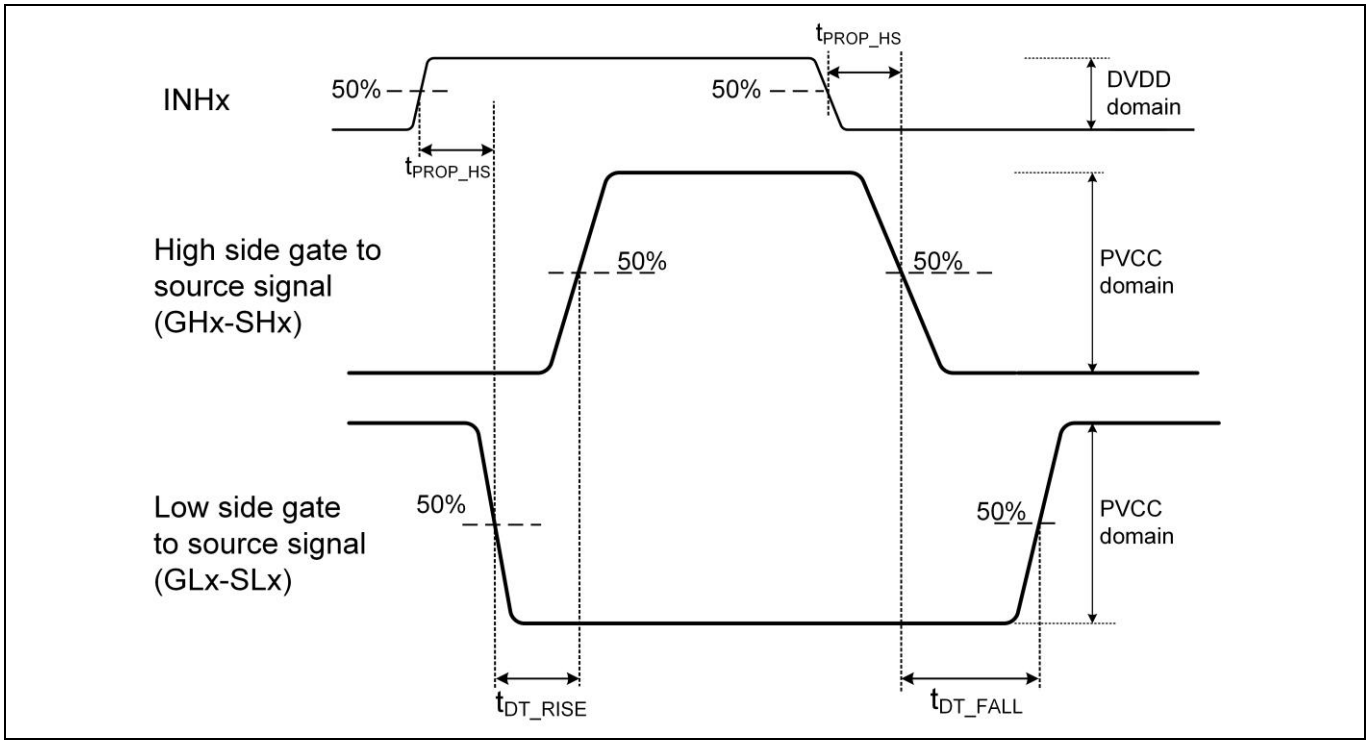

Figure 27 PWM insertion ideal timing diagram for 1PWM mode.

4.2 Gate Driver Architecture

Three identical pairs of high side and low side drivers are integrated. High and low side drivers are designed with the same architecture. However, supply domains for both sections are developed differently. Precise charge pumps are utilized to supply both drivers, VCCLS to the low side gate drivers, and VCCHS to the high side gate drivers. An overview of the general architecture is shown in Figure 28.

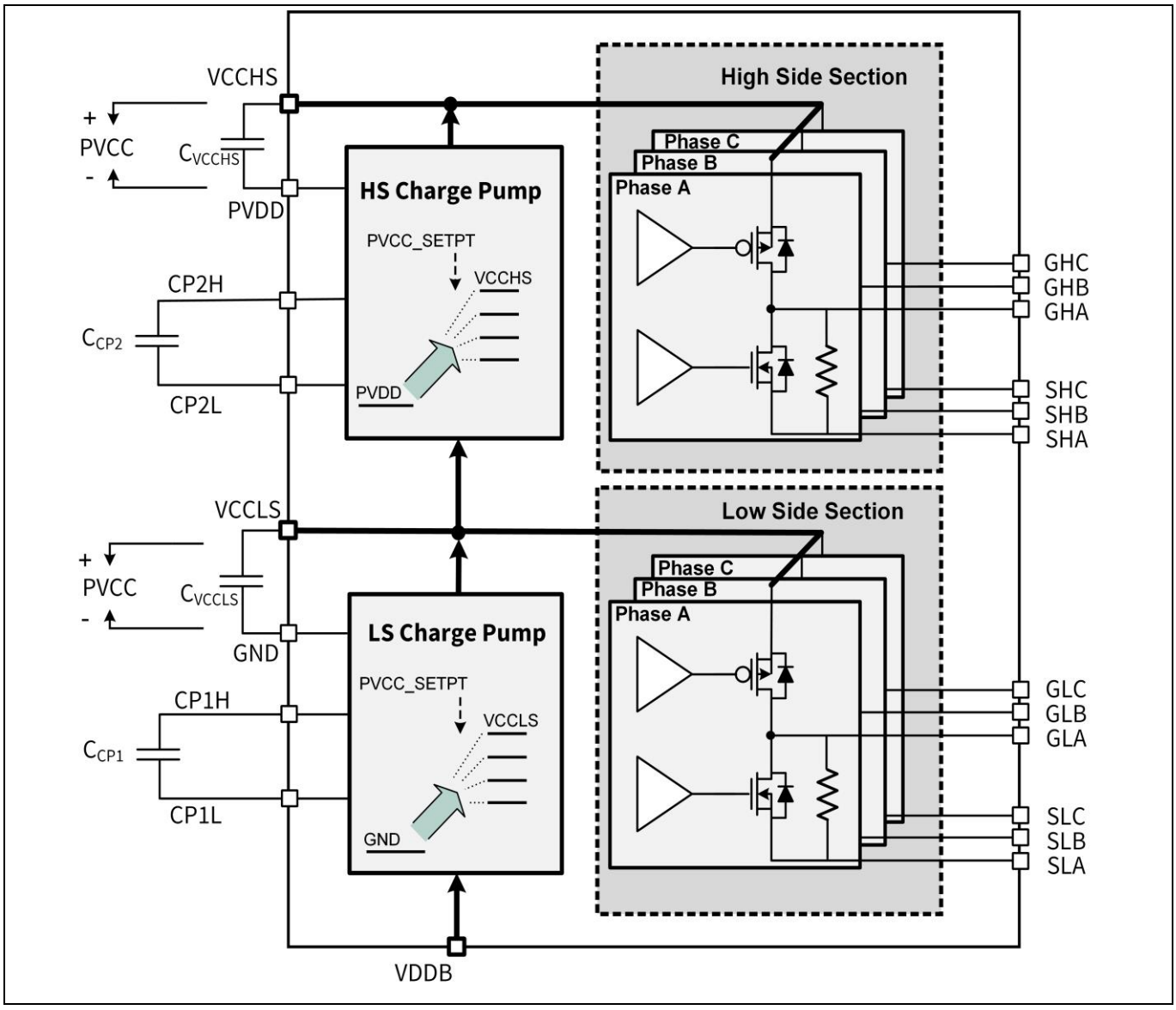

Figure 28 Gate driver architecture overview

The low side section of the gate driver is supplied by VCCLS. When the device is under normal operation, VCCLS is “PVCC” volts above ground. VCCLS voltage is generated by “LS Charge Pump” from VDDB voltage –integrated buck converter output voltage. An external “flying” capacitor C_{CP1} is required for the charge pump to work properly.

The high side section of the gate driver is supplied by VCCHS. A separated charge pump generates “PVCC” volts above PVDD for properly bias of the high side MOSFET drivers. Similarly to low side section, a “flying” capacitor C_{CP2} is necessary for proper operation of the charge pump. PVCC voltage is programmable via SPI registers and defines the gate driving voltage of the inverter power MOSFETs.

Additional decoupling capacitors C_{VCCLS} and C_{VCCHS} are required for VCCLS and VCCHS pins respectively. These and other required components recommended values are shown in Table 30.

The selection of those capacitors will have an impact i different parameters in the charge pump including the voltage ripple in VCCLS/HS, as well as the start-up time or the maximum load that the gate driver can sustain.

4.3 Slew Rate Control

Control of MOSFET V_{DS} rise and fall times is one of the most important parameters for optimizing drive systems, affecting critical factors like:

- Switching losses,
- Dead time optimization,
- V_{DS} ringing with possible avalanche event in MOSFETs. Avalanche is a critical factor in MOSFETs that can lead to device destruction or reliability issues,
- EMI design and optimizations,
- Control of negative spike in SHx pins,
- Possible snubber design (MOSFET snubber or bridge bypass capacitors)

MOTIX™ 6EDL7141 is capable of adjusting the slew rate of the MOSFET switching (V_{DS}). Slew rate control functionality controls independently the rise (low to high) and fall (high to low) slew rates of the drain-to-source voltage by adjusting the gate current applied to MOSFET gate.

Note: *R_g resistors might be used, however, user must consider the voltage drop on the resistor when driving the MOSFET with the constant current provided by 6ELD7141*

4.3.1 Slew Rate Control Parameters and Usage

User can configure the gate driver current and timings with following parameters via SPI accessible registers:

- I_{HS_SRC} – bitfield IHS_SRC: gate driver current value for switching **ON high side** MOSFETs
- I_{HS_SINK} – bitfield IHS_SINK: gate driver current value for switching **OFF high side** MOSFETs
- I_{LS_SRC} – bitfield ILS_SRC: gate driver current value for switching **ON low side** MOSFETs
- I_{LS_SINK} – bitfield ILS_SINK: gate driver current value for switching **OFF low side** MOSFETs
- I_{PRE_SRC} – bitfield IPRE_SRC: **pre-charge** gate driver current value for switching **ON both high and low side** MOSFETs. Needs to be enabled via bitfield IPRE_EN, otherwise pre-charge will be set to max current.
- I_{PRE_SNK} – bitfield IPRE_SNK: **pre-discharge** gate driver current value for switching **OFF both high and low side** MOSFETs. Needs to be enabled via bitfield IPRE_EN, otherwise pre-discharge will be set to max current.
- T_{DRIVE1} – bitfield TDRIVE1: amount of time that I_{PRE_SRC} is applied. Shared configuration between high and low side drivers
- T_{DRIVE2} – bitfield TDRIVE2: amount of time that I_{HS_SRC} and I_{LS_SRC} are applied. Shared configuration between high and low side drivers
- T_{DRIVE3} – bitfield TDRIVE3: amount of time that I_{PRE_SNK} is applied. Shared configuration between high and low side drivers
- T_{DRIVE4} – bitfield TDRIVE4: amount of time that I_{HS_SINK} and I_{LS_SINK} are applied. Shared configuration between high side and low side drivers

The driving implementation is presented in Figure 29. This represents a 6PWM mode in which the XMC1404 inserts a specific dead time between INHx and INLx signals. The driving scheme is applicable to other PWM modes. Propagation delays are not depicted for simplification of the diagram (see Figure 27 for details on propagation delay).

Once the gate is commanded to apply a change to the output, the gate driver will apply a constant current defined by the user programmable value I_{PRE_SRC} for a time defined by T_{DRIVE1}. After T_{DRIVE1} period, the MOSFET gate voltage should ideally have reached the threshold voltage ($V_{GS(th)}$). After T_{DRIVE1}, the gate driver applies next gate current configuration for a period defined by T_{DRIVE2}. The current applied in this period is decisive to determine both dI/dt and dV/dt of the MOSFETs as it will charge the Q_{sw} of the MOSFETs. User can alternatively decide to

reduce this period to cover only Q_{gd} portion, therefore controlling dI/dt region with the T_{DRIVE1} period for independent control. To ensure proper fine tuning, 6EDL7141 offers separate configuration registers for the high side and low side (I_{HS_SRC} and I_{LS_SRC} respectively).

Once T_{DRIVE2} period is elapsed, the gate driver applies full current (1.5A) to ensure fastest turn on of the MOSFET. This will fully charge the MOSFET gate ($Q_{od} = Q_g - Q_{sw} - Q_{g(th)}$) till the programmed PVCC value.

A similar process takes place in the discharge of the MOSFET

Attention: ***Consider that slew rate variation affects the actual dead time value. User must select dead time accordingly***

VGS Comparators

MOTIX™ 6EDL7141 integrates gate to source comparators. These are used to detect when the Vgs signal is almost at the target value PVCC, i.e. $V_{GSX} \geq$ PVCC - $V_{GS\_CPM\_TH}$ during charging phase and $V_{GSX} \leq V_{GS\_CPM\_TH}$ during the discharge phase. When any of these happen, the comparator trips and sets the gate current to I_{HOLD} value. This is to reduce power consumption and help reducing the possible impact of the self-turn-on effect, for example when the high side MOSFET is turning on while the low side MOSFET is off. In this case, the hold current in the low side MOSFET will help tightening down the gate of that MOSFET to the source with I_{HOLD} strength. In Figure 29 I_{HOLD} is shown as dashed and depending on VGS value will be applied sooner or later. In Figure 30 the thresholds for activating I_{HOLD} current are shown.

The comparator integrates a deglitching stage that avoids noise to activate the comparator erroneously during noisy events. The deglitching time is defined by $t_{VGS\_CMP\_DEGLITCH}$.

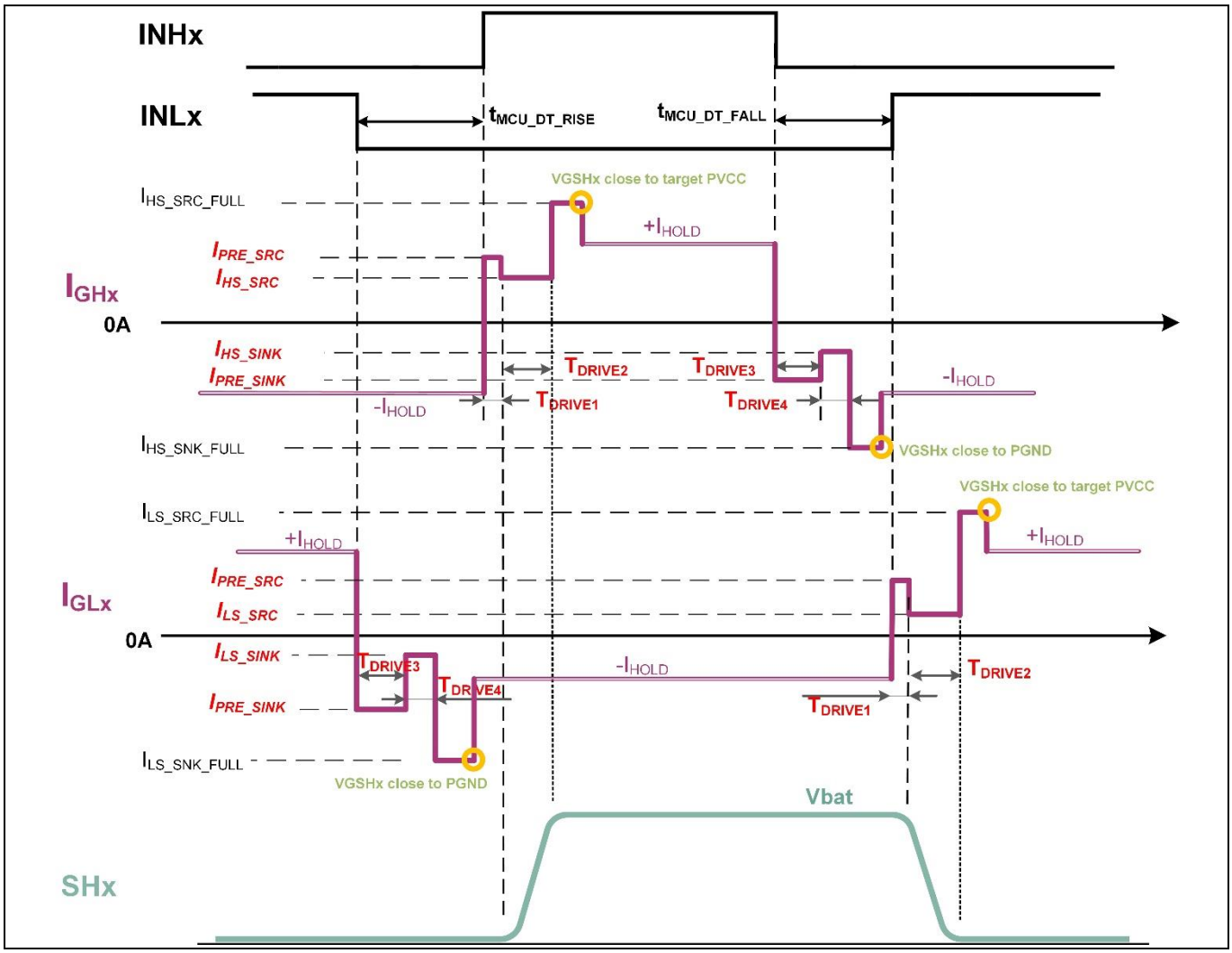

Figure 29 Slew rate control timing for a complete switching cycle on a 6PWM mode-dead time assumed to be inserted by XMC1404. Propagation delays (INxy→Gxy) not considered for simplification. Parameters on red refer to programmable values

Figure 30 shows a detail of the charging and discharging transitions for a high side MOSFET. Similar applies to a low side MOSFET. The different gate charge areas of the MOSFET are shown. Thanks to the flexible timing structure and the high T_{DRIVEX} resolution, user has full control of the gate current applied during critical charge areas like Q_{sw} which is the key parameter controlling the MOSFET Vds slew rate. This at the same time can be done while maintaining fast charging of other areas like Q_{od} which typically is relatively large compared to Q_{sw} and therefore, as it does not affect neither dV/dt nor dI/dt, can be accelerated by increasing gate current.

Additionally, the pre-charge area ($Q_{gs(th)}$), depending on the particular MOSFET, can benefit from a larger gate current than the one applied to the Q_{sw} region where maximum control is required. Thanks to the pre-charge current configuration, higher gate currents can be selected for $Q_{gs(th)}$ reducing importantly the pre-charge timing, which otherwise could have needed several hundreds of ns to reach to $V_{gs(th)}$.

The pre-charge current can be selected from 17 different values. 16 defined by $I_{PRE\_SRC/SNK}$ and additionally 1.5A, which is the maximum peak current capability of the gate driver. In case of large MOSFETs, $Q_{gs(th)}$ during turn on or Q_{od} ($Q_{od} = Q_g - Q_{sw}$-$Q_{gs(th)}$) during turn off, might benefit from using the whole gate driver capability. In order to enable the full strength during the pre-charge area, register I_PRE _EN has to be set in register IDRIVE_PRE_CFG.

Note: When transitioning from one current setting to another, user can experience some transition period until new current value is up and stable. During this period, the current might become lower than programmed for a brief period before reaching the target value.

Note: When the gate to source voltage is getting close to the target voltage, either PVCC when charging or PGND when discharging, the gate driver will not be able to fully maintain the target I_G current. This effect deviates from the ideal behavior shown before and can follow similar behavior to the dashed lines in Figure 30. This is independent from the I_{HOLD} values described before.

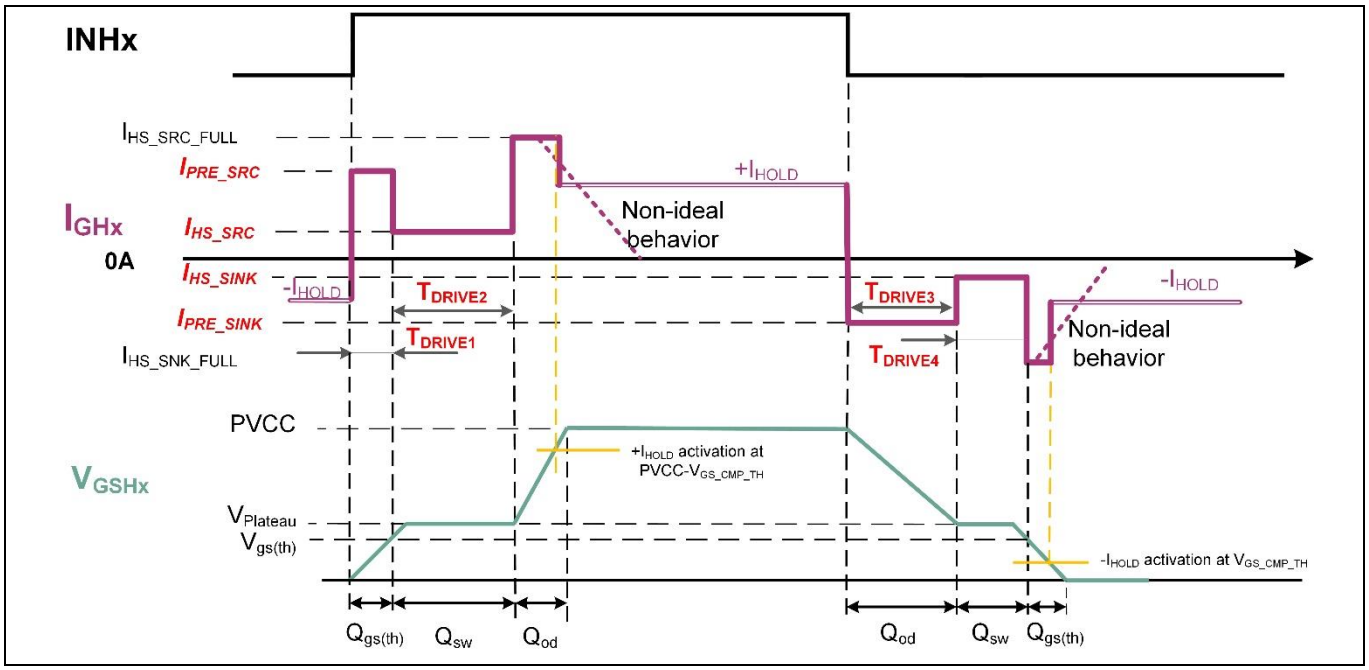

Figure 30 Detail of MOSFET gate charge during the charging and discharging transitions

In cases where $Q_{g(th)}$ is too small to apply a larger current than the one used for slew rate control, user can set T_{DRIVE2} to value 0. This will results in the gate driver start driving the MOSFETs with T_{DRIVE1} and once the period is elapsed it will apply 1.5A ignoring T_{DRIVE2} configuration. This ensures optimal settings for both large and small MOSFETs and right fit for different technologies like OptiMOS™ or StrongIRFET™. Similarly, T_{DRIVE2}, T_{DRIVE3} and/or T_{DRIVE4} can be set to 0 resulting in those configurations being skipped. Figure 31 shows an example of this behavior where T_{DRIVE2} = 0 while other T_{DRIVEX} settings are different than zero.

Note: When driving with a single timing setting the charge or the discharge phases, it is recommended to use either T_{DRIVE1} or T_{DRIVE3} as driving periods and make T_{DRIVE2} or T_{DRIVE4} equal to 0. The opposite is possible, however might result in selected timing (T_{DRIVE2} or T_{DRIVE4}) becoming slightly shorter than the programmed value due to internal propagation delays. User must decide which solution fits better to the application

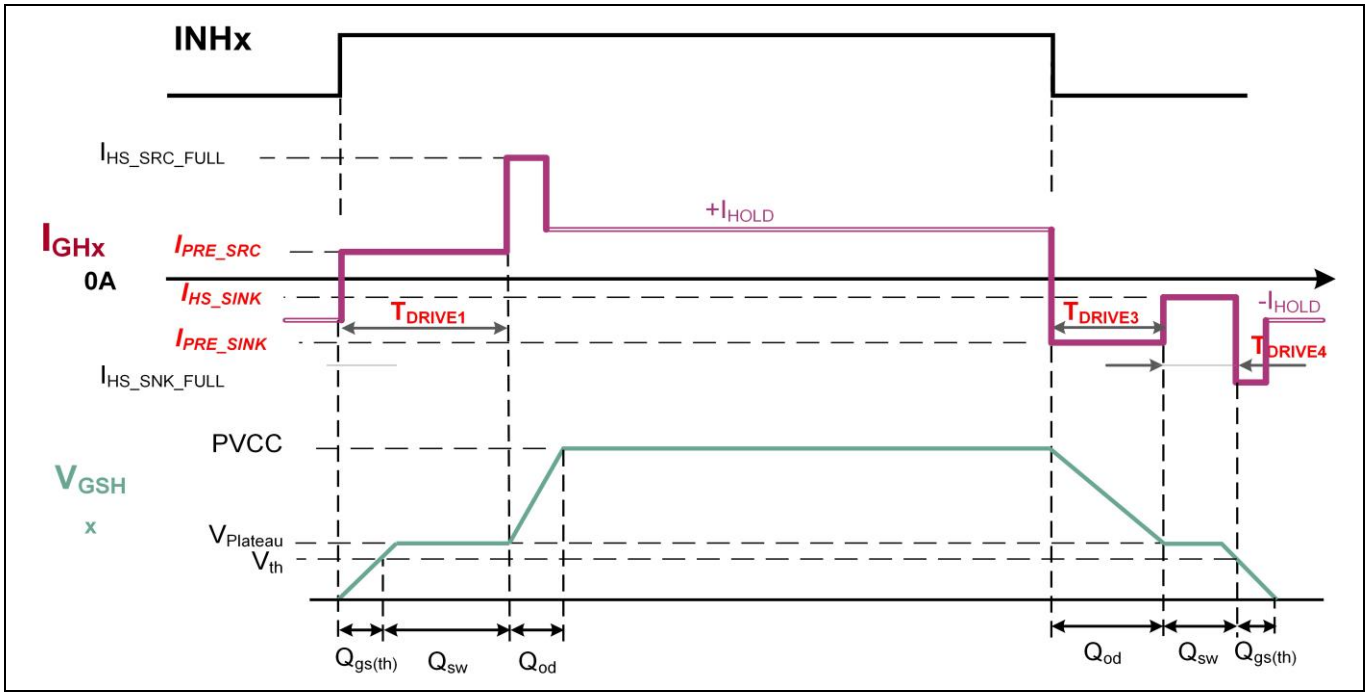

Figure 31 Detail of MOSFET gate charge during the charging and discharging transitions. T_{DRIVE2}=0 example

4.4 Gate Driver Voltage Programmability

Different drives systems might benefit from different MOSFET technologies. An example is the common usage of logic level MOSFET vs standard or normal level MOSFETs, which show a higher threshold voltage ($V_{gs(th)}$). For the same gate to source voltage, a logic level MOSFET presents lower R_{DSON} value than a normal level MOSFET.

Increasing the driving voltage helps reducing the R_{DSON} of the MOSFET channel during conduction and as a result the conduction losses of the system. This is shown in Figure 32. However, increasing the driving voltage increases the rise switching times (rise and fall) leading eventually to higher switching losses. User must choose the right driving voltage depending on the system conditions.

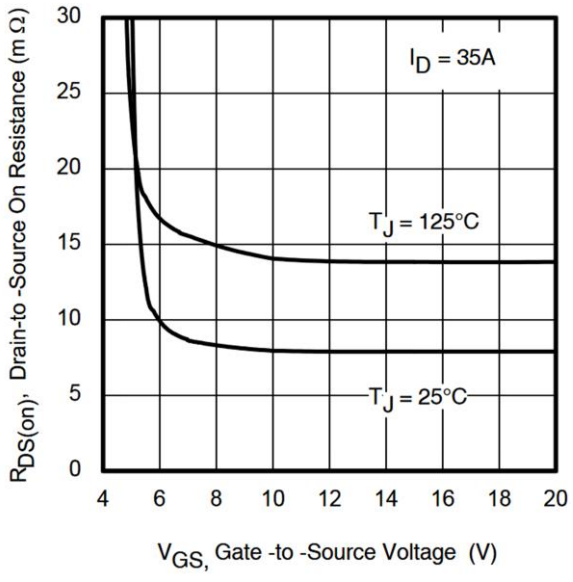

Figure 32 Typical R_{DSON} vs V_{GS} characteristic in MOSFETs. Higher V_{GS} voltage reduces the R_{DSON} of the MOSFET

6EDL7141 allows designers to adjust the MOSFET driving voltage (PVCC voltage) via SPI registers. The same value PVCC applies to both high and low side charge pumps with four possible values: 7V, 10V, 12V, 15V. This is done via bitfield PVCC_SETPT.

Note: It is expected that the high side charge pump produces a lower voltage due to internal circuitry (diode).

Figure 33 shows an ideal example of how supply voltage of the driver and slew rate control can play a role together in an ideal turn on of a low side MOSFET. Section A of the figure shows how to set the slew rate of V_{GS} external MOSFET, by programming different current values (in this case I_{LS_RISE}). Section B shows the case in which, provided a fixed gate driver current I_{LS_SRC}, PVCC is varied.

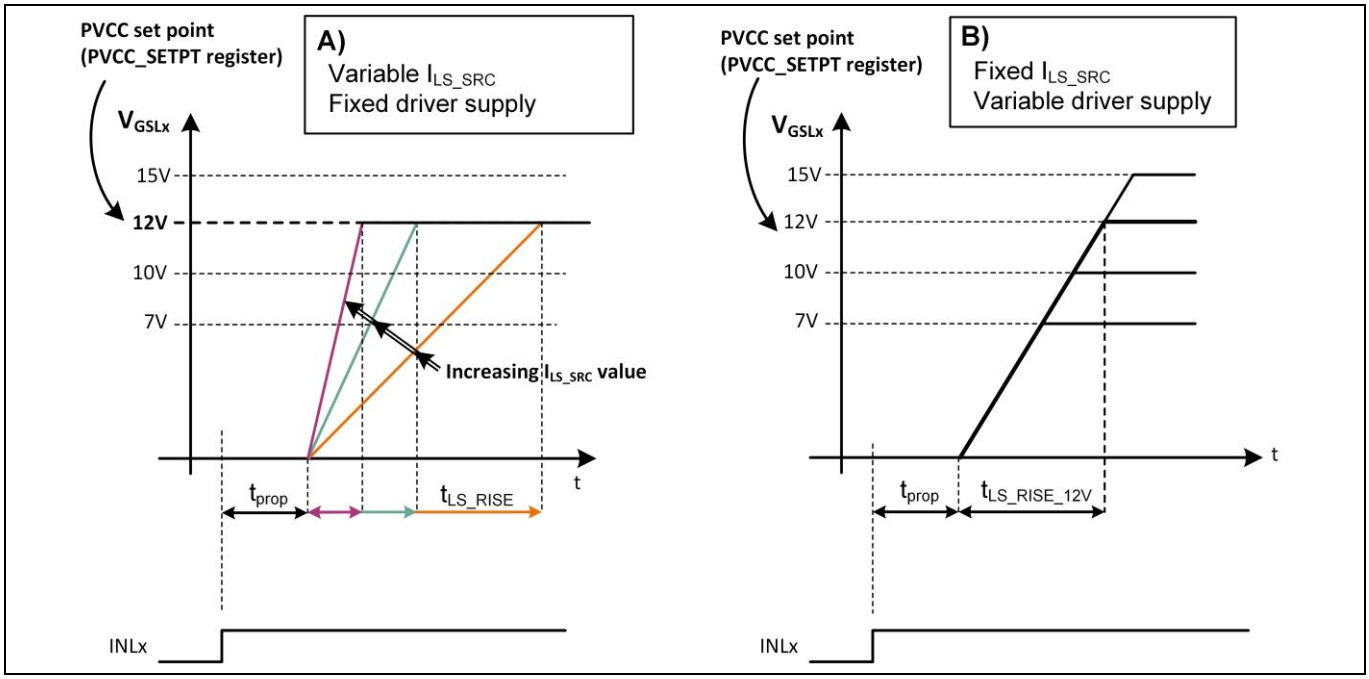

Figure 33 Gate driver slew rate configurability in an ideal low side MOSFET switching: A) given a fixed supply voltage (PVCC=12V), variable I_{LS_RISE} B) Fixing the charging current, changes in PVCC produce different rise times

4.5 Charge Pump Configuration

User can adjust charge pumps operation in MOTIX™ 6EDL7141 depending on the specific needs. Following sections describe this configurations.

4.5.1 Charge Pump Clock Frequency Selection

Charge pumps are based on switched capacitor circuits that work at a given switching frequency. 6EDL714 offers the possibility to choose four different clock frequencies via SPI programming of bitfield CP_CLK_CFG in register CP_CFG. The selection of charge pump capacitors both flying and tank capacitors must be chosen according to this configuration and both affect start-up time of VCCLS and VCCHS rails as well as possible voltage ripple in those pins.

4.5.2 Charge Pump Clock Spread Spectrum Feature

When activated, this feature introduces artificially a frequency variation (see Electrical Characteristics table for values) into the charge pump clock signal. The frequency at which the charge pump operates will vary between those limits reducing the emission intensity on the target frequency value by distributing that energy over a wider range of frequencies.

4.5.3 Charge Pump Pre-Charge for VCCLS

Pre-charge of the charge pumps is a feature that, if enabled via SPI register, pre-charges the VCCLS rail right below the buck converter output voltage (VDDB) before the EN_DRV pin is activated. This pre-charge takes place only the first time after a power up (CE cycle) sequence.

In this case, when EN_DRV is activated to enable the driver stage, the charge pumps need to ramp up the voltage in C_{VCCLS} from the existing pre-charge voltage until the PVCC selected value, therefore reducing considerably the start-up time for the charge pump when compared to the default situation in which C_{VCCLS} needs to charge the whole PVCC voltage.

To enable the pre charge of VCCLS, bitfield CP_PRECHARGE_EN in register SUPPLY_CFG must be set.

4.5.4 Charge Pump Tuning

The start-up time for the charge pumps, defined as the time that the VCCLS voltage requires to get to the target programmed voltage (PVCC Set point), depends on several factors:

- Target voltage programmed via PVCC_SETPT register: the higher the longer the start-up time
- Charge pump clock frequency: higher clock frequency results in faster start-up time
- Charge pump tank capacitors (C_{VCCLS}, C_{VCCHS}): using VCCLS as example, a smaller value of C_{VCCLS} will result in:
    - Higher VCCLS ripple
    - Faster start-up time
- Charge pump flying capacitors (C_{CP1}, C_{CP2}): smaller capacitors lead to slower start-up time

The selection of those parameters have an impact as well in the VCCLS and VCCHS voltage ripple. If fast start-up time is not a design target, it is recommended to increase the C_{VCCLS} value to reduce ripple and to improve load transients. For a given C_{VCCLS} value, the selection of C_{CP1} will impact also the ripple in VCCLS and start-up time.

If start-up time needs to be optimized, charge pump pre-charge feature is recommended. This is explained in section 4.5.

The start-up behavior of the charge pumps and rest of power supply is shown in detail in section 10.1

4.6 Gate Driver and Charge Pumps Protections

The gate driver includes following protections:

- VCCLS UVLO
- VCCHS UVLO
- Floating Gate Driver Pull Down
- Dead Time insertion - This is explained in section 4.1.7

4.6.1 VCCLS Under-Voltage Lock-Out (VCCLS UVLO)

The UVLO prevents the gate driver from propagating PWM signals if the drive voltage is not above the UVLO threshold as specified in the Electrical characteristics table.

During start-up, the charge pump voltage VCCLS will ramp up until the UVLO rising threshold is crossed releasing the UVLO status, allowing then the PWM to propagate.

In case of overload of VCCLS rail beyond the specified maximum load of the charge pump, the VCCLS will drop. Eventually, the VCCLS voltage can cross the VCCLS UVLO falling threshold leading to both the immediate stop of the PWM signal being transmitted to the MOSFETs by setting the gate driver in Hi-Z (high impedance) mode and also reporting a fault to the Fault handler. Consequently, the nFAULT pin will be pulled down so the XMC1404 can decide how to proceed.

4.6.2 VCCHS Under-Voltage Lock-Out (VCCHS UVLO)

Similarly to VCCLS, a UVLO mechanism is integrated for VCCHS voltage rail. The UVLO rising and falling thresholds can be found in the Electrical Characteristics table.

During start-up, the charge pump voltage VCCHS will ramp up until the UVLO rising threshold is crossed releasing the UVLO status, allowing then the PWM to propagate.

In case of overload of VCCHS rail beyond the specified maximum load of the charge pump, the VCCHS voltage will start dropping. VCCHS voltage can then cross the VCCHS UVLO falling threshold leading to both the immediate configuration of the gate driver to Hi-Z (high impedance mode) and also to the reporting to the Fault handler. As a result of the VCCHS UVLO, the nFAULT pin will be pulled down so XMC1404 can decide how to proceed.

4.6.3 Floating Gate Strong Pull Down

MOSFETs in an inverter can be exposed to non-zero gate voltage levels when the controllers or gate drivers are off. Sometimes those voltages are enough to activate or partially activate the MOSFETs leading to system failure or destruction if for example, a high side MOSFET and a low side MOSFET in an inverter leg activate at the same time. In order to prevent this behavior is common to assemble weak pull downs (in the order of 100kΩ resistors) between gate and source of the MOSFET to ensure that when the gate driver is off, the gate is pulled down to the source avoiding any turn on or partial turn on. As it is weak pull down, this does not have noticeable impact when the gate driver is active and driving MOSFETs normally.

These six $R_{G\text{-}S}$ resistors however require a good amount of PCB area and need to be placed in a location where the power layout needs to be optimized with no compromises.

In order to address this, 6EDL7141 gate driver integrates a floating gate strong pull down mechanism that includes both a passive and an active pull down:

- Weak Pull Down: a weak pull down ($R_{GS\_PD\_WEAK}$) is always connected between gate and source of each gate driver output. This ensures a weak pull downs during states where the gate driver is off, either because EN_RV is turned off or because the device is fully off (CE off). This mechanism is similar to the ones described above ($R_{G\text{-}S}$).
- Strong Pull Down: additionally, during those gate driver off periods, if the external gate to source voltage increase for any reason as mentioned, an extra pull down, much stronger ($R_{GD\_PD\_STRONG}$) is activated ensuring a tight pull down and hindering any possible partial turn on.

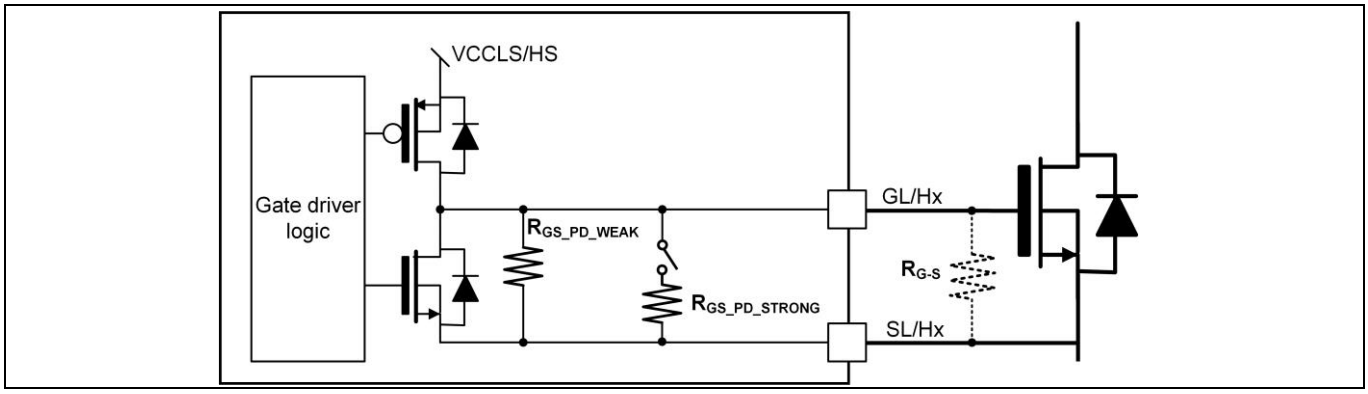

Figure 34 Floating gate driver pull down resistors. Strong pull down activates when gate driver is off and gate to source voltage increases

5 MOTIX™ 6EDL7141 Power Supply Subsystem

The device embeds an advanced power supply system comprised of:

- Synchronous buck converter including both power switches
- DVDD linear voltage regulator pre-programmed to 3.3V (IMD700A) or 5V (IMD701A)
- Charge pump for low side gate driver (described in 4)
- Charge pump for high side gate driver (described in 4)

MOTIX™ IMD70xA has been designed for lowest Bill of Material (BOM). The synchronous buck converter does not require external components like diodes, voltage dividers or bootstrap capacitors yet at the same time reduces the low side conduction losses as it utilizes a NMOS instead of a diode.

The overall goal of the buck converter is to support the rest of the power supply system. With the help of an external filter (LC), it supplies both (high side and low side) charge pumps and the integrated DVDD voltage regulator. This architecture increases the efficiency of the device greatly compared to an only linear regulator system, yet maintains a very compact system solution. Furthermore, allows working at high supply voltage rating (PVDD).

DVDD linear voltage regulator is integrated to provide accurate and stable voltage to XMC1404 and other external components. In Figure 35, a schematic diagram of the complete power converter architecture and interconnections is showed.

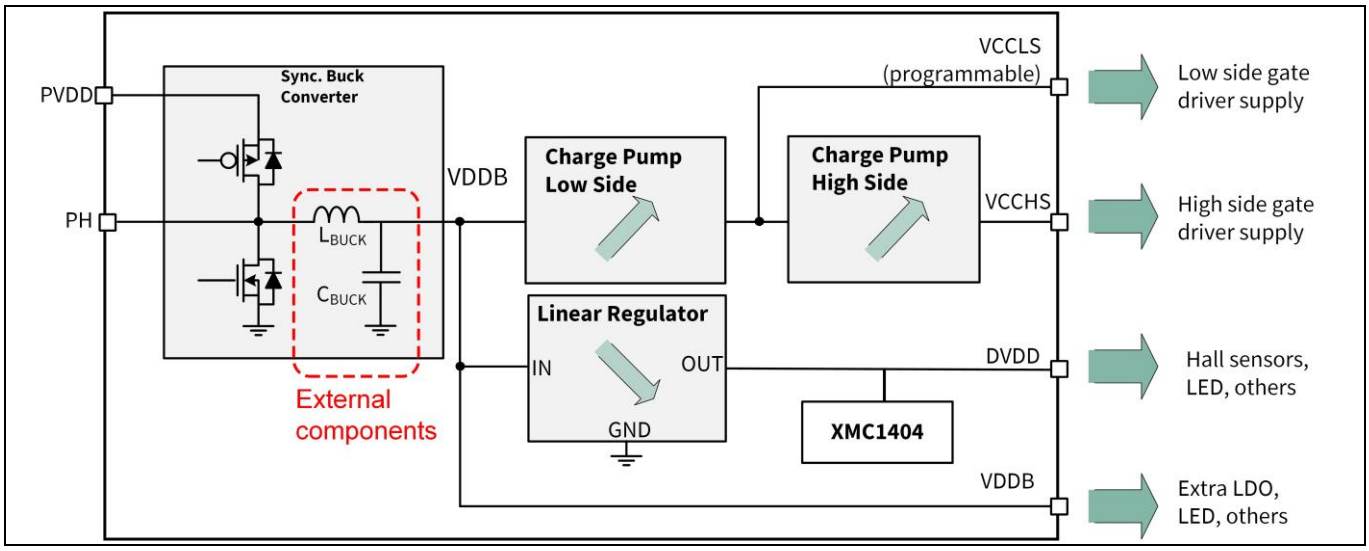

Figure 35 Block diagram of power converter architecture

Designers can use VDDB pin to supply external components as long as the current limits of the buck converter-including charge pumps and linear regulator- are not exceeded. Nevertheless, over-current protections (OCP) are implemented for both buck converter and the linear regulator, preventing any damage to the device when overloading VDDB pin. Additional over-temperature protections (OTS, OTW) are integrated to ensure the device is under correct thermal conditions at any time.

5.1.1 Synchronous Buck Converter Description

Although integrated in the same package, the synchronous buck converter is designed completely independent of the rest of the gate driver circuitry. This makes the supply system robust against gate driver failures. As an example, the buck converter and linear regulator will still operate even if a failure occurs in the gate driver

section (e.g. VCCLS UVLO), ensuring right operation of circuits in the system supplied by the buck converter or LDO integrated.

The control method utilized is Adaptive Constant 'ON' Time (ACOT). In contrast to a pure constant ON time control method, ACOT allows for ON time variations during transitions to avoid large frequency jumps. Together with feedforward techniques, this buck converter can operate almost at fixed switching frequency.

Two different switching frequencies (500 kHz and 1 MHz) can be selected via SPI –BK_FREQ bitfield-for the buck converter. The recommended inductor and capacitor for each configuration is provided in section 12.1. Recommended values for the inductor and capacitor are shown in Table 30.

Note: It is recommended to only modify the buck converter frequency via OTP

A detailed figure of both synchronous buck converter and linear voltage regulator circuits is depicted in Figure 36.

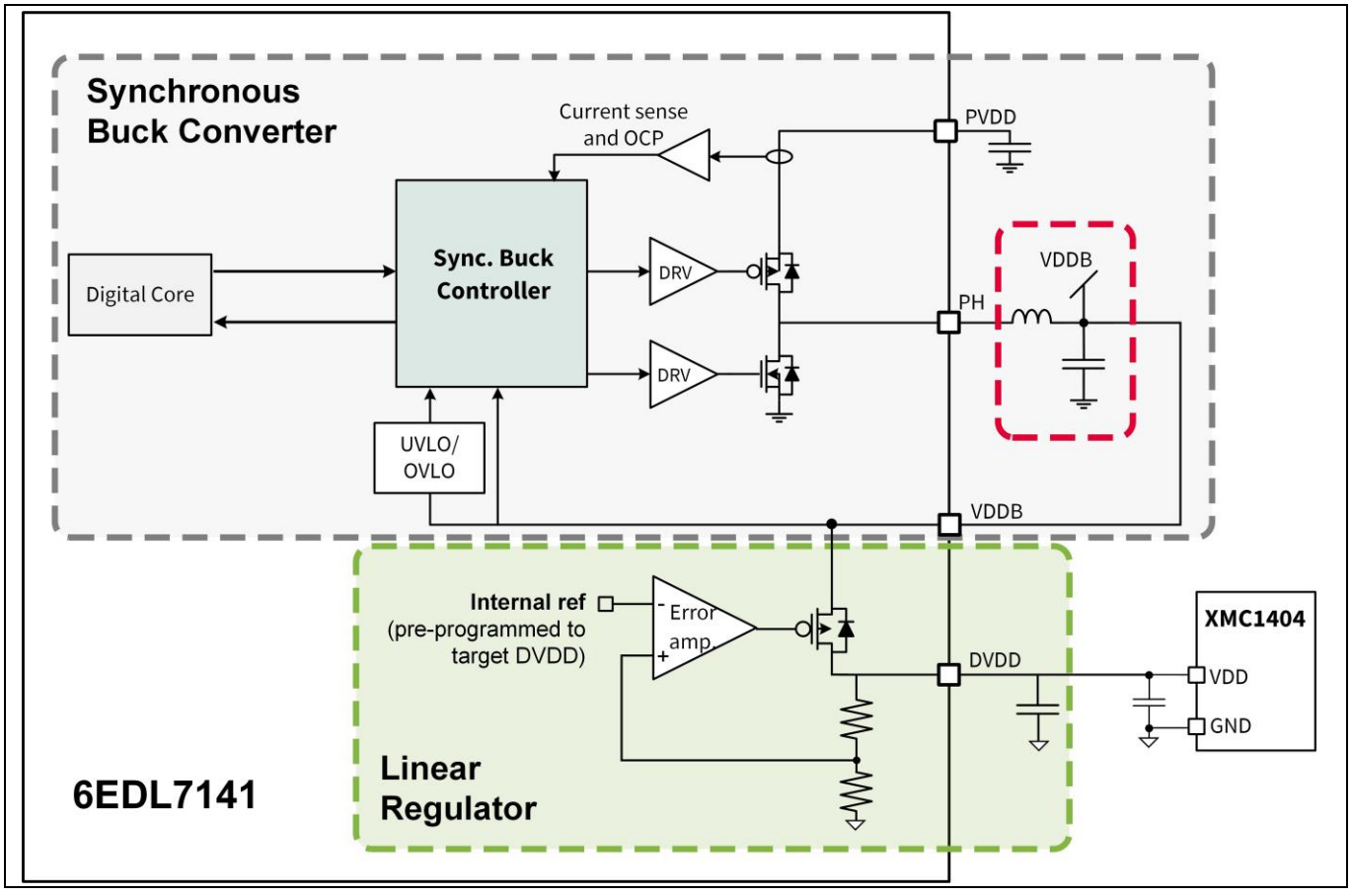

Figure 36 Detail of integrated synchronous buck converter controller and linear regulator

5.1.1.1 Buck Converter Output Voltage Dependency on PVCC_SETPT

An important feature of the buck converter is the ability to automatically adjust VDDB target value depending on PVCC (target gate driver voltage) configured by user via SPI commands. This is done to optimize power losses in the device. For example, if the driving voltage PVCC is 7V, the target voltage of the buck converter is automatically set to 6.5V given and still the charge pumps will have enough room to reach PVCC = 7V on a 'doubler' configuration. The relationship between VDDB and PVCC is shown in Table 23.

Table 23 Buck converter output target voltage vs PVCC_SETPT setting

PVCC_SETPT bitfield	PVCC target voltage (V)	VDDB (V)
b'11	7	6.5
b'10	10	7
b'00	12	8
b'01	15	8

Another important factor to consider in the synchronous buck converter output target voltage is PVDD or supply voltage. If PVDD is low enough so $VDDB_{NOM\_LV}$ rating applies (see Electrical Characteristics table), then the buck converter cannot ensure the target output voltage as provide in Table 23. In this situation, the buck converter enters a 'limiter' mode in which the duty cycle saturates to DC_{BUCK_MAX} (see Electrical characteristics table). If buck converter loading increases or PVDD voltage reduces further, VDDB voltage will drop. On the lower end, VDDB UVLO falling threshold protects from lower limits.

Therefore, depending on PVDD voltage, it is possible that VDDB cannot reach the target voltage, limiting as a consequence the actual PVCC voltage, which even in a doubler configuration might not be sufficient. The approximate possible PVCC voltage (= VCCLS) in the doubler configuration is given by the minimum between the target PVCC voltage or twice VDDB minus 1 V as shown in following equation:

$$PVCC_{max} \approx \min(PVCC\ Target\ Voltage, 2 * VDDB - 1V) \quad (1)$$

As an example, if PVDD = 7.5V, VDDB ≈ 6.5V (limited by low PVDD), if PVCC_SETPT targets 15V, the doubler on the charge pump will be able to reach maximum of approximately 2* VDDB-1V ≈ 12V. If then PVDD rises to 12V, the VCCLS will be able to regulate to 15V as this value is below/equal to the value = 2* VDDB (8V) -1V = 15V.

See 2.7 for more details on relationship between VCCLS, VCCHS and PVDD.

5.1.1.2 Synchronous Buck Converter Protections

Following protections are implemented to ensure correct operation of the buck converter:

- **Output Under-Voltage Lock-Out (UVLO).** See Electrical Characteristics table for specific values
- **Output Over-Voltage Lock-Out (OVLO)**. See Electrical Characteristics table for specific values. If the value is reached the buck converter will switch off both high side and low side MOSFETs interrupting any further energy transfer to the output.
- **Over-Current Protection (OCP)** cycle by cycle. Given a situation in which the current increases till the OCP level (see Electrical Characteristics table for details), the buck converter controller will truncate the high side FET PWM signal until next PWM period start. The low side FET will be driven accordingly after insertion of dead time. The OCP level reduces as well if PVDD is below 7.465V to ensure proper device operation.

  Once the OCP event takes place, a counter will start counting for each consecutive period that the peak current is reached. After 16 periods, the Buck OCP fault is triggered and nFAULT pin (see Table 25) will be set low to inform the XMC1404 that can proceed with correcting actions. The Buck converter will continue operation in current limitation to ensure XMC controller is supplied. If the OCP does not trigger for 3 consecutive PWM periods, the counter will reset and will not trigger the Buck OCP fault. If the Buck OCP fault is activated, the bitfield BK_OCP_FLT in register FAULT_ST will be set.

5.1.2 DVDD Linear Regulator

The integrated linear regulator generates the voltage rail DVDD that can supply XMC1404.

Attention: User must connect externally all DVDD pins as there is no internal connection for DVDD inside.

DVDD linear regulator can be used as well to provide an offset to the current sense amplifiers integrated, allowing negative current measurements. See 6.1.4 for more details.

The linear regulator is soft started during ramp up of the device as depicted in Figure 56 after a delay time $t_{DVDD\_TON\_DLY}$ once the buck converter has reached its UVLO level ($V_{VDDB\_THH\_UV}$) and analog programming of CS_GAIN is finished. The DVDD ramp up timing can be configured via SPI via bitfield DVDD_SFTSTRT.

A schematic view of DVDD linear regulator and the interaction with the buck converter is presented in in Figure 36.

DVDD voltage is be used to supply the integrated XMC1404 controller and can be used to supply additional elements in the circuit like Hall sensors, LEDs, etc. A programmable OCP mechanism is provided to avoid damage to the LDO due to excessive current demand.

5.1.2.1 DVDD Linear Regulator OCP

DVDD OCP can be configured between 4 different levels by writing register DVDD_OCP_CFG. If the OCP for DVDD is reached, a fault will be reported on pin nFAULT. The DVDD OCP works in two different stages:

1. **Pre-warning mode at 66% of selected OCP level**: nFAULT pin will be pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching 100% level, the operation will continue normally releasing the nFAULT pin. The pre-warning allows some extra time for XMC1404 to make a decision on how to react to the possible OCP event.
2. **Current limiting mode at 100% of selected OCP level**: if current increases beyond the configured OCP level, the DVDD regulator will start limiting the current provided. This will cause a DVDD voltage drop, eventually resulting in a DVDD UVLO fault if DVDD UVLO threshold is crossed (see the Electrical Characteristics table for more details). Thanks to this limitation, possible shorts on DVDD rail will not affect rest of the system keeping these other components safe.

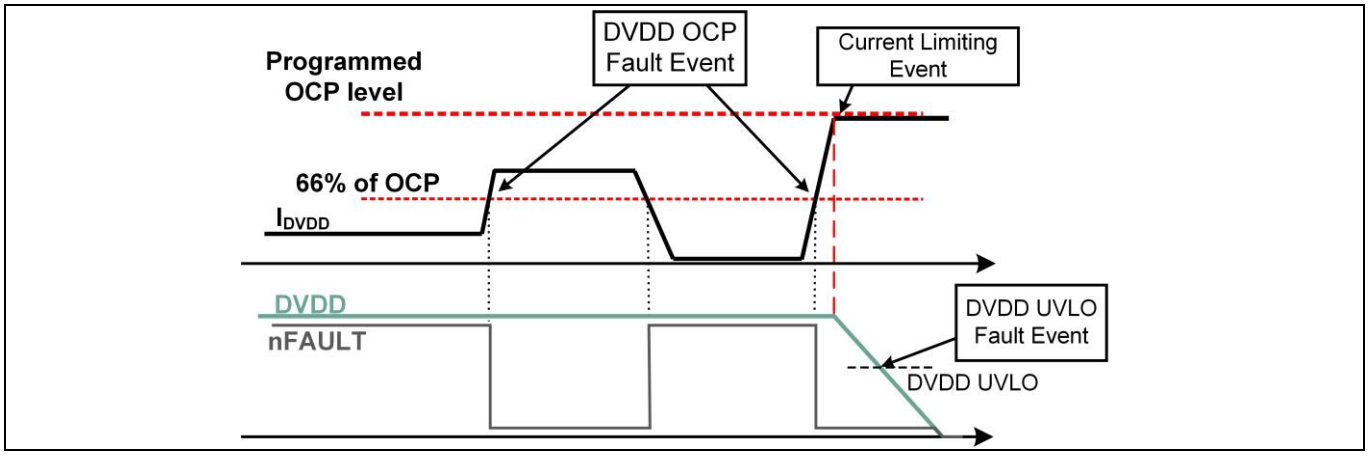

Figure 37 DVDD OCP behavior including pre-warning and current limiting modes

Note: The OCP in DVDD is suppressed during ramp up of the device to avoid that initial charge of DVDD decoupling capacitors (eventually large capacitors) triggers the OCP fault

Over-temperature faults (OTS, OTW) provide an additional level of protection. These will trip if too high temperature is developed in the device, for example when the DVDD linear regulator or the buck converter demand excessive load current.

6 MOTIX™ 6EDL7141 Current Sense Amplifiers

The device integrates three current sense amplifiers that can be used to measure the current in the power inverter via shunt resistors. Single, double or triple shunt measurement are supported as shown in Figure 38.

CS_EN bitfield enables each current sense amplifier individually. The output of the current sense amplifiers can be connected to the ADC inputs (AINx pin) of IMD70xA via optional RC filters to remove high frequency components. Gain and offset are generated internally and must be programmed via SPI commands.

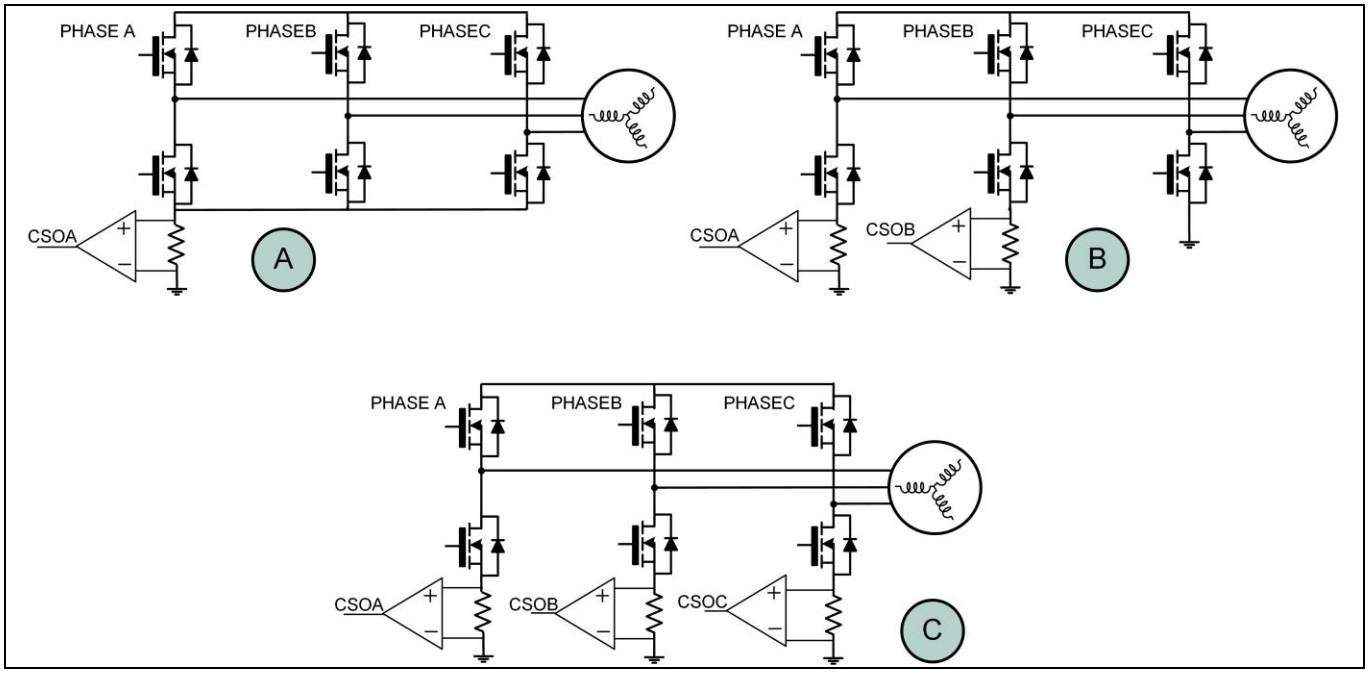

Figure 38 Single (A), dual (B)and triple (C) shunt current sensing configurations are supported

The current sense amplifier block contains the following sub-blocks explained in detail this section:

- **Current sense amplifier**: connected to external shunt resistor or internally to SHx and SLx pins for R_{DSON} sensing configuration. This module amplifies the shunt voltage or V_{DS} voltage to a more appropriate voltage level for a microcontroller ADC. It allows as well blanking the signal synchronized to PWM transitions, during periods where noise is disturbing the measurement. Gain must be set via SPI programming in IMD70xA, no resistor configuration is possible.
- **Output buffer**: allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to 4 different values by programming the internally generated level. With this implementation, negative current in current shunts can be measured. Additionally permits to optimize the controller ADC dynamic range according to system conditions.
- **Positive Over-Current comparator**: used for detecting the over-current condition on motor winding for positive shunt voltage This comparator can be used to apply PWM truncation in trapezoidal commutation schemes, limiting the motor current to the configured OCP threshold.
- **Negative Over-Current comparator**: used for detecting the over-current condition on motor winding for negative shunt currents
- **OCP Digital-to-Analog Converter (DAC)**: used for programming the threshold of the over-current comparators. One for positive level and a second one for negative level. Programming of DAC levels is shared among different OCP comparators.

Current sense amplifiers are able to “Auto-Zero” during operation and ensures best accuracy of measurements during lifetime of the device. Additionally, the device includes a current sense amplifier user calibration mode that can be used to calculate residual offset before the driver is enabled (EN_DRV low), therefore ensuring current in the inverter and in the shunts are zero. XMC1404 can remove this initial residual value from future measurements to improve accuracy.

Figure 39 shows these blocks and their interconnections.

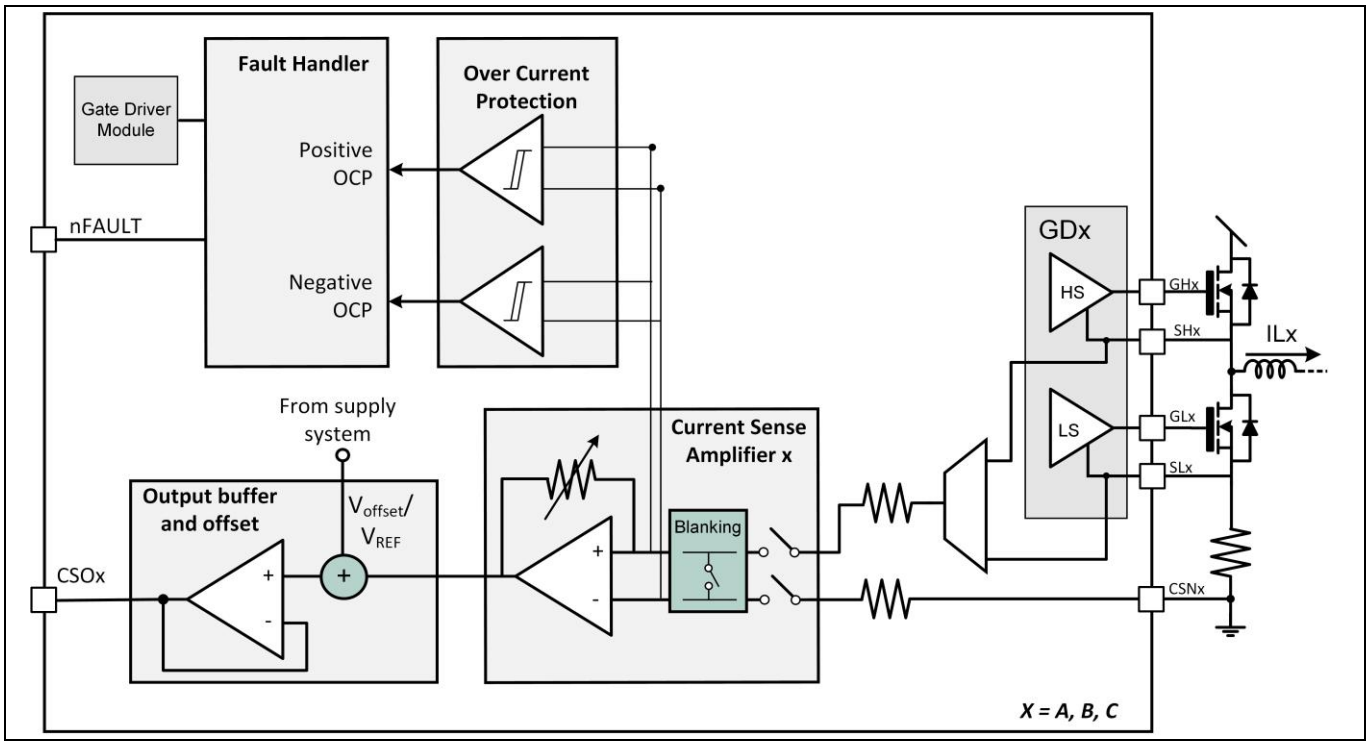

Figure 39 Current sense amplifier simplified block diagram

6.1.1 R_{DSON} Sensing Mode vs Leg Shunt Mode

Current sense amplifiers in MOTIX™ 6EDL7141 can be configured as leg shunt or R_{DSON} sensing, where the ‘ON’ resistance of the MOSFETs is used as shunt in a ‘lossless’ measurement approach.

In R_{DSON} mode, 6EDL7141 connects the drain of the low side MOSFET to the positive input of the current sense amplifier. The negative input is connected to the source as shown in Figure 40. This is in contrast to the external shunt configuration shown in Figure 41, where the positive input of the current sense amplifier is connected to the source of the low side MOSFET. Internal series resistors help filtering possible noise before the amplification takes place. Depending on the circuits and board design, a small filtering capacitor between SLx and CSNx pins can help cleaning up the current signal.

Note: R_{DSON} mode is only possible in 3 shunt mode (mode C in Figure 38)

Note: In R_{DSON} mode, the CSAMP is forced to be CS_TMODE = 0, meaning the current sense amplifiers are only active when low side is ON (GL ON mode). Writes different than b’0, will be ignored by the internal logic.

Note: Temperature compensation for the R_{DSON} measurement, if required, must happen via XMC1404 algorithms not provided here.

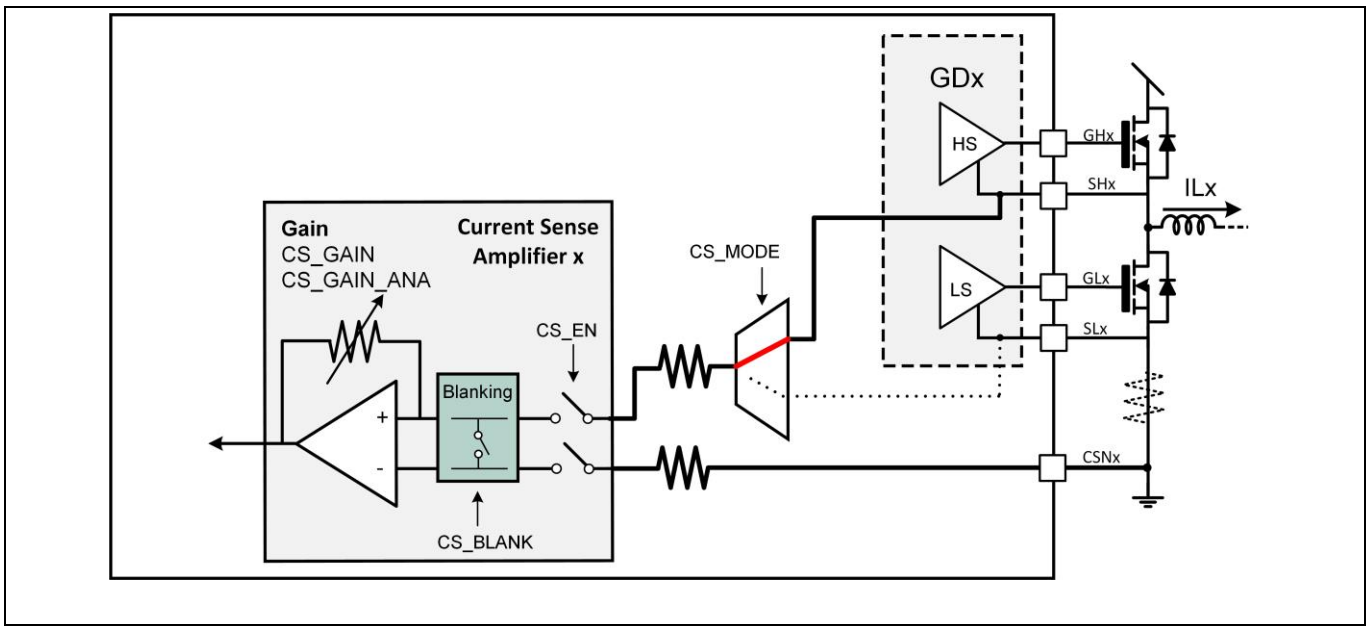

Figure 40 System diagram of a low side R_{DSON} current sensing configuration utilizing integrated current sense amplifiers

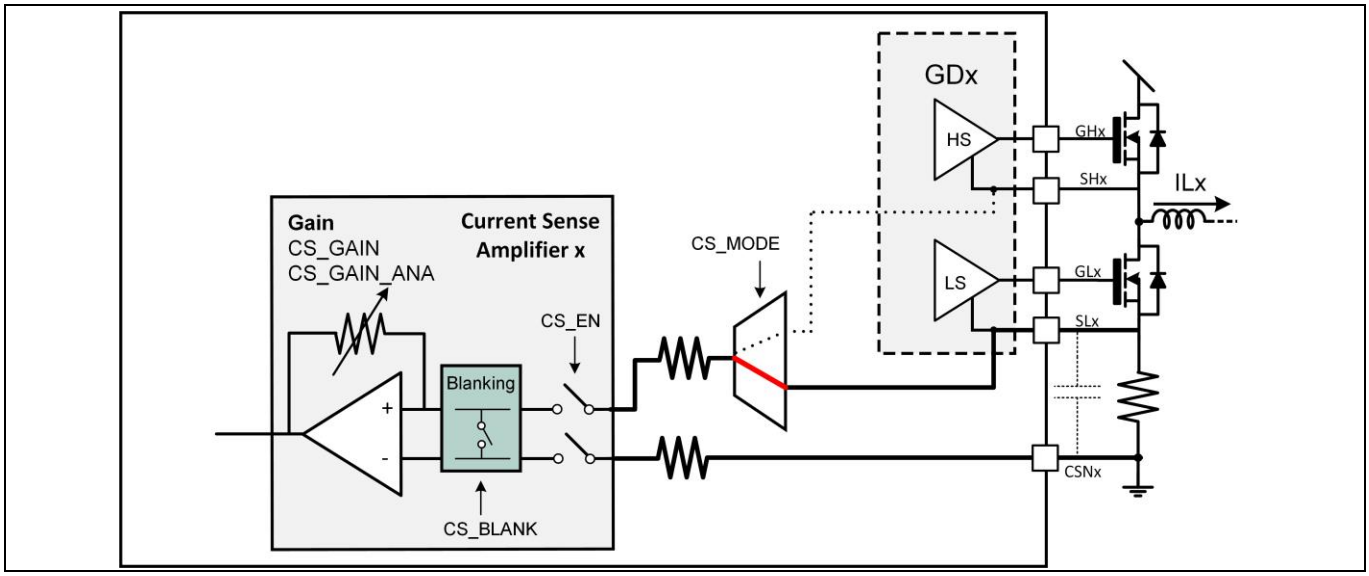

Figure 41 System diagram of an external shunt current sensing configuration utilizing integrated current sense amplifiers

6.1.2 Current Shunt Amplifier Timing Mode

Often in drives applications, the current is sampled via leg shunts. IN this case, the voltage in the shunt that needs to be amplified appears only when the low side MOSFET is turned on. In other cases, it might be useful to propagate the signal continuously. IMD70xA supports four different modes of operation of the current sense amplifiers regarding when the output pin CSOx is connected to the amplifier stage. These four modes are:

- **Always OFF**: current sense amplifier output disabled. This is achieved by disabling the amplifier in register CSAMP_CFG via bitfield CS_EN.

- **GL ON**: in this mode, CSOx pin is connected to the amplifier only when the same leg or phase GLx signal is active. In single shunt mode, CSOx will be connected according to the OR'ing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSox will be dedicated to that GLx signal. This mode is forced if R_{DSON} sensing is selected to avoid possible overvoltage damage in the internal circuitry. In order to enable this mode, the amplifier must be enabled via CS_EN bitfield in CSAMP_CFG register and the timing mode selected via write to CS_TMODE bitfield in SENSOR_CFG.
- **GH OFF**: similarly to GL ON, this modes connects the CSOx outputs during GL ON period but extends that connection to the dead times both rising and falling. This is same than GH OFF. In some cases like during diode recirculation current, the diode might carry current that can be useful especially in cases where the PWM pulses are very narrow. Same as GL ON, single shunt will logic OR the GLx activations and three shunt modes will activate according to each GLx signal only. In order to enable this mode, the amplifier must be enabled via CS_EN bitfield in CSAMP_CFG register and the timing mode selected via write to CS_TMODE bitfield in SENSOR_CFG.
- **Always ON**: this mode connects continuously the activated amplifier CSOx signals to the amplifier independently of PWM signals. In order to enable this mode, the amplifier must be enabled via CS_EN bitfield in CSAMP_CFG register and the mode selected via write to CS_TMODE bitfield in SENSOR_CFG.

Figure 42 (cases 1 and 2) shows a comparison of the current sense amplifier working in both modes GL ON and GH OFF.

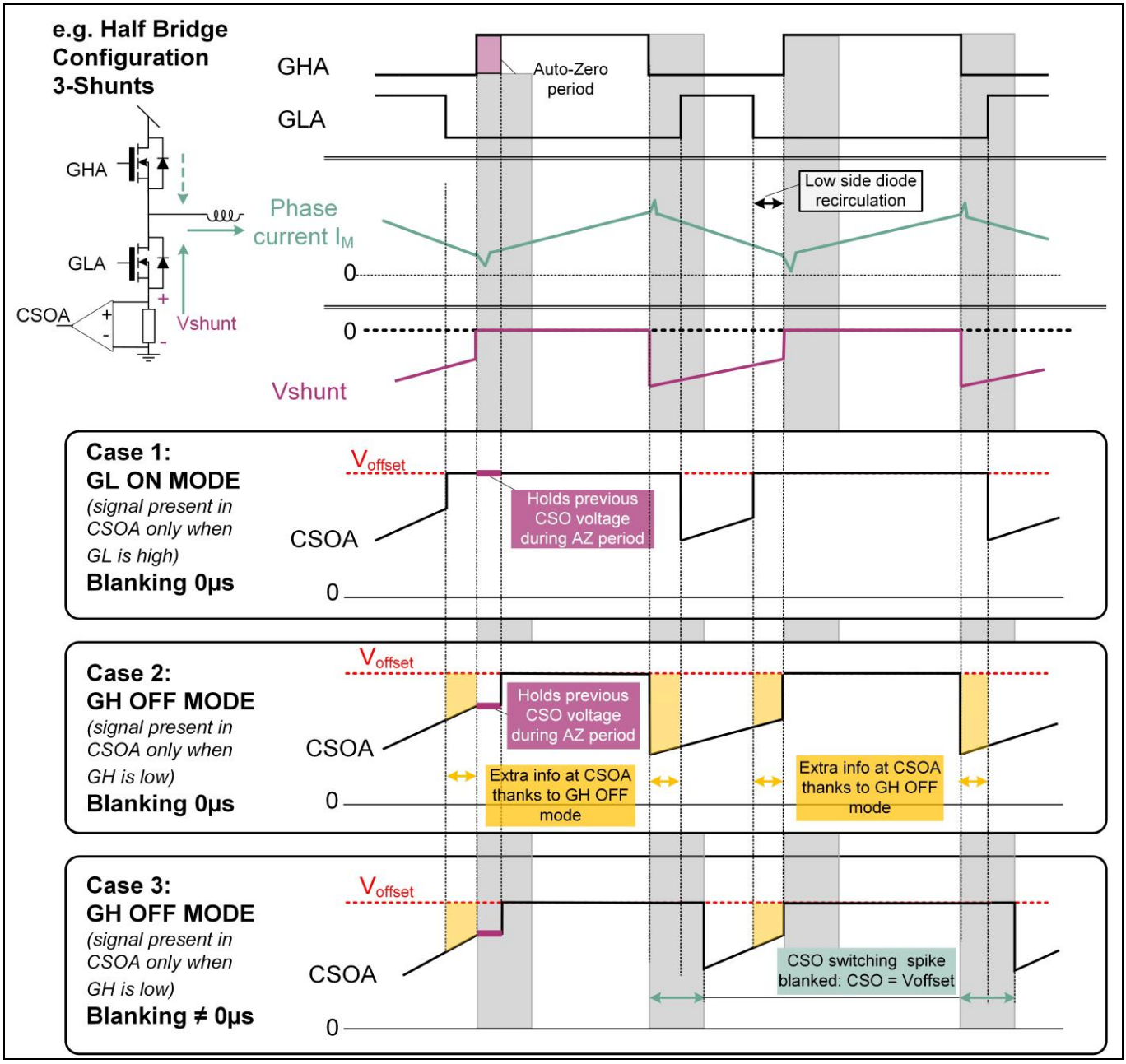

Figure 42 Current sense amplifier ideal timing mode examples. Mode GL ON and GH OFF operation in a half bridge example with leg shunt current sense configuration-3 active amplifiers. GH OFF can potentially propagate current information when the diode recirculates current. Auto Zero injected on GHx rising (internal sync.)

6.1.3 Current Shunt Amplifier Blanking Time

A programmable blanking period can be configured in the current sense amplifiers. The goal of adding some blanking time is to avoid propagating a distorted signal to the microcontroller ADCs during MOSFET switching transitions. Since both, phase node voltage SHx and SLx pins (CSNy) are subject to ringing due to the switching activity, the blanking module disconnects the inputs for a configurable time (CS_BLANK). This action occurs in synchronicity with GHx signals (rising and falling edges) driving the external MOSFETs.

During the blanking time, pin CSO will show V_{offset} voltage until the programmed blanking time period expires and inputs are connected again to the current sense amplifier. Two examples are shown in Figure 43. Example

A) represents a trapezoidal commutation scheme with 1 shunt similar to the one in Figure 62. In such case the high side of one phase (phase B) is switching, while the low side of another phase (phase A) is always ON, allowing the current to flow through the motor windings. As the low side MOSFET of phase A is ON for 120 degree of rotation, the current sense amplifier is amplifying the shunt voltage continuously except blanking and recirculation periods. These blanking periods corresponds to both high side and low side rising edges (ORing of all phases). In this case the voltage across the shunt is positive.

The example in B) corresponds to a generic half bridge configuration (e.g. synchronous buck converter). In this case, when high side is turned on, the current in the inductor increase, while in the complementary cycle when the high side switches off and the low side turns on after dead time, the current flows through the low side and starts decreasing. During the low side conduction, the current sense amplifier generates the shown output proportional to the voltage across the shunt, in this case negative.

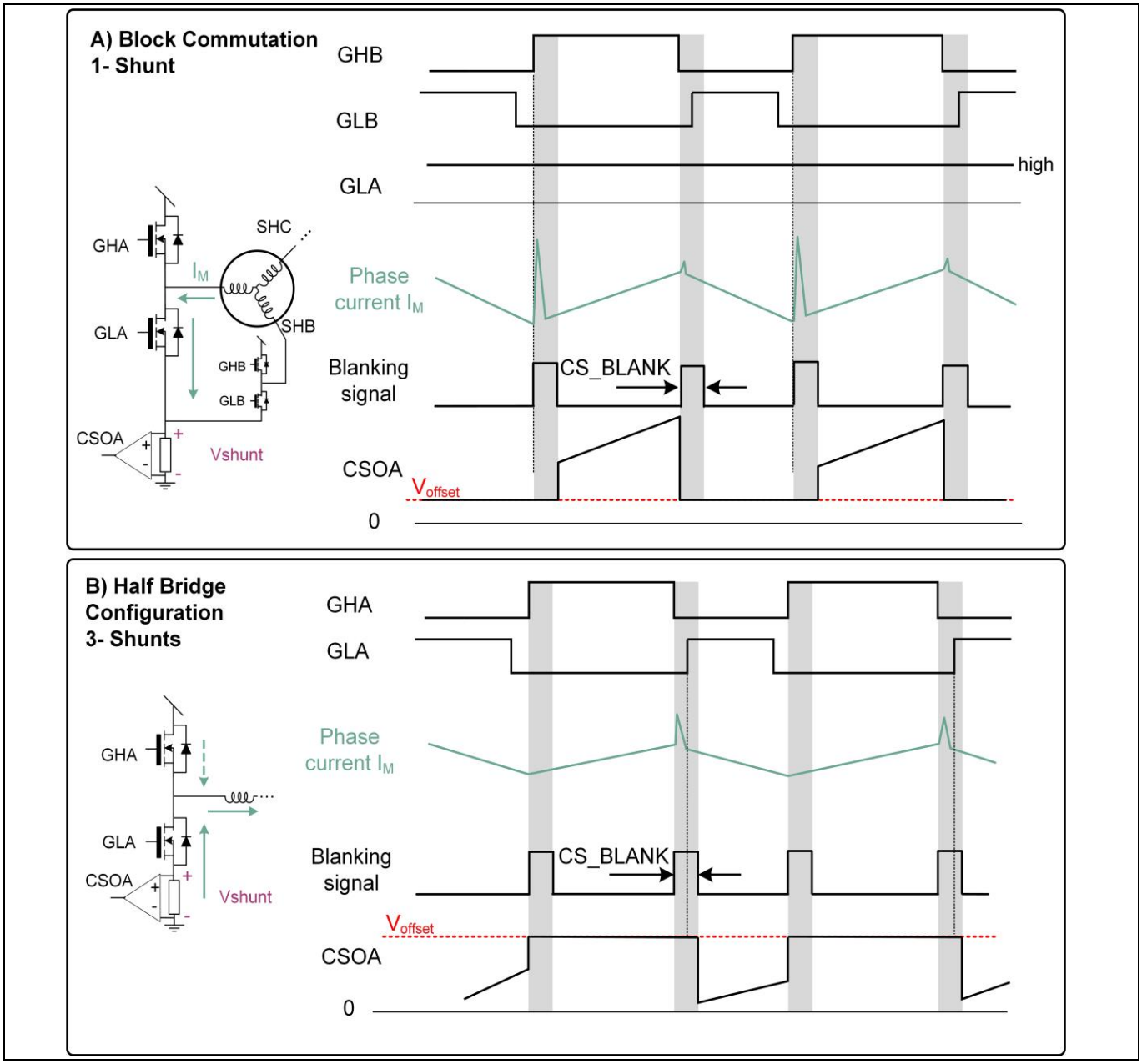

Figure 43 Timing diagram of a current measurement utilizing blanking time feature for suppressing current spikes during MOSFET switching. A) Trapezoidal commutation with 1 shunt configuration. B) Generic half bridge configuration.

6.1.4 Current Sense Amplifier Internal Offset Generation

6EDL7141 integrates an internal linear voltage regulator (DVDD) that can be used for offset generation in all integrated current sense amplifiers. The generated DVDD voltage can be scaled down to different programmable values to adjust the desired offset voltage level. Bitfield CS_REF_CFG controls this scaling factor.

XMC1404 generates internally the reference for the integrated ADC out of the supply voltage. In this way the microcontroller can accurately measure in a ratio-metric way the output of the current sense amplifiers increasing noise immunity. Figure 44 shows a block diagram representing this implementation. Only internal offset generation is possible in IMD70xA.

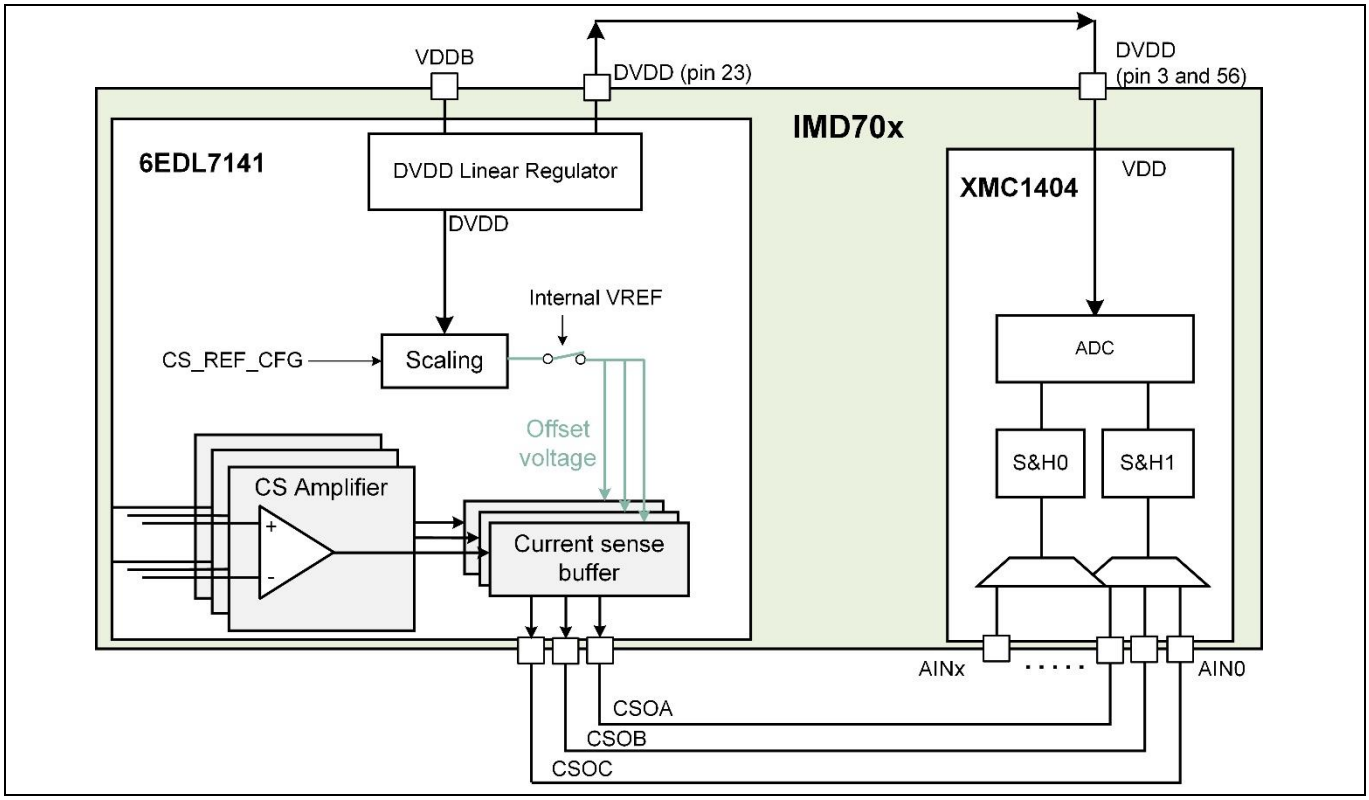

Figure 44 Current sense amplifier offset generation block diagram

6.1.5 Overcurrent Comparators and DAC for Current Sense Amplifiers

Two overcurrent comparators are implemented for monitoring the current in both positive and negative direction with an extensive level of programmability. Figure 45 shows a schematic diagram of this implementation. Both comparators monitor the current flowing through the shunts. The triggering level is independent from the gain setting of the shunt amplifiers and is defined as the voltage across the shunt. The comparator features a hysteresis (specified as V_{OC_HYST}) for consistent operation.

Positive and negative triggering levels for the comparator are set with two independent Digital to Analog Converters (DAC). These DACs are programmed via bitfields CS_OCP_PTHR for positive overcurrent protection and CS_OCP_NTHR for negative overcurrent protection. For possible threshold levels see the registers description in section 11.

The output of the comparators can be deglitched by programming register CS_OCP_DEGLTICH before reaching the Fault handler, where the fault will be processed (See section 6.1.8) and eventually will pull down nFAULT pin reporting a fault to XMC1404.

Alternatively, the comparator output propagates to the PWM modules. PWM truncation can be enabled via bitfield CS_TRUNK_DIS. If PWM truncation is activated, the PWM module immediately interrupts the PWM signal without having to wait for the XMC1404 to make such decision if the OCP level is reached. This ensures fastest possible reaction time to the OCP event. Truncation is detailed in section 0.

CS_OCPFLT_CFG in register CSAMP_CFG allows the user to set a target number of consecutive events (PWM cycles with current above OCP threshold) that will activate OCP fault. This means the user can configure the device to wait for several PWM periods before declaring a fault.

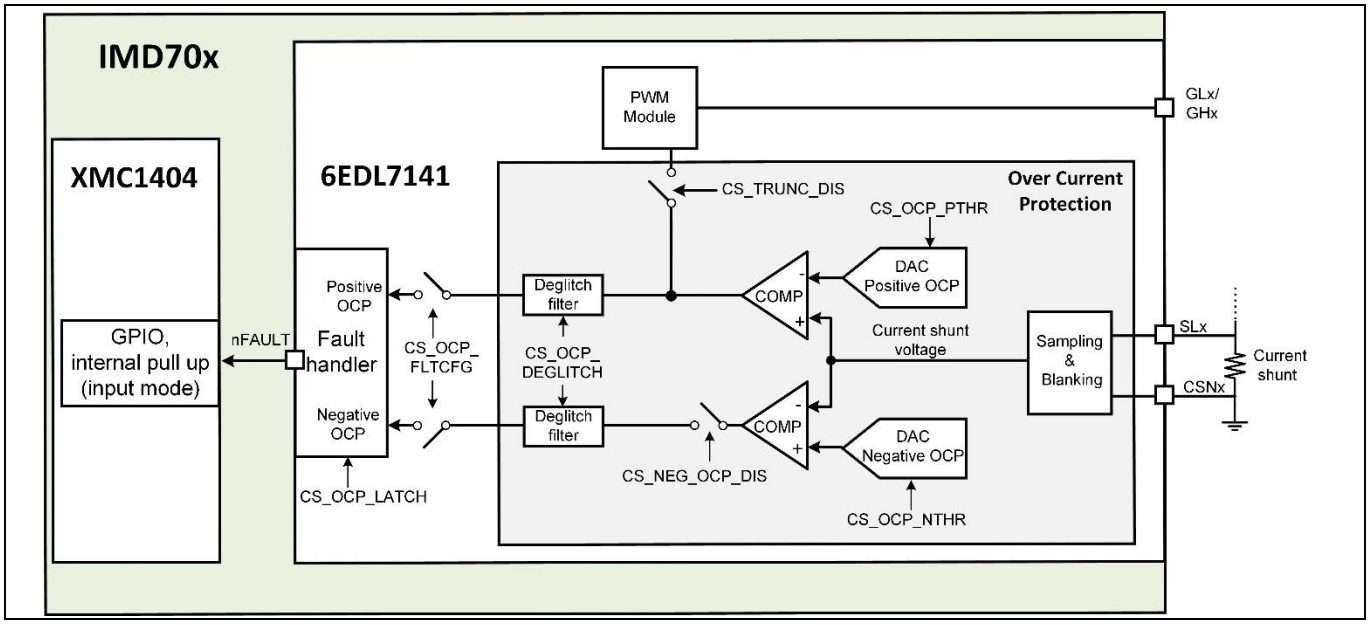

Figure 45 Current sense amplifier protections schematic block diagram

6.1.5.1 OCP Use Cases

The reaction to an OCP event is programmable via SPI. Following scenarios might be useful for different applications:

- **Apply PWM truncation** immediately after OCP event **and report on nFAULT** pin after OCP event- deglitching is disabled if truncation is enabled.
- **Disable reporting and keep truncation of PWM**. This can be useful during events where the reporting function to the microcontroller might not be necessary.
- **Trigger a configurable brake action** upon OCP event. If truncation is not desired, the brake event can be configured to e.g. brake the motor by shorting all low side MOSFETs. By using the deglitch function, the possible noise in the analog signal can be filter out to avoid false trip of the OCP. This configuration can be useful for FOC (Field Oriented Control) schemes given the flexibility. Braking is explained in more detail in sections 4.1.6 and 6.1.8.
- **Disable OCP protection,** both nFAULT reporting and truncation of PWM. In such case, OCP is ignored. This might be useful for transition states or stop procedures as well.

These configurations can be adjusted also during ACTIVE state of the device. It is also possible to select whether the OCP fault trips on a single event or more and whether is latched or not via bitfield CS_OCP_LATCH.

6.1.5.2 OCP Fault Reporting

In case of OCP fault, 6EDL7141 can report the fault by pulling down pin nFAULT. Internally, IMD70xA connects this pin to P3.4 pin in XMC1404. XMC code can poll this GPIO pin to be informed of the fault and make a decision.

CS_OCPFLT_CFG in register CSAMP_CFG allows the user to set a target number of consecutive events (PWM cycles with current above OCP threshold) that will activate OCP fault. This means the user can configure the device to wait for several PWM periods before declaring a fault and therefore be more conservative. Three options are possible: no fault, trigger immediately (i.e. trigger on all events) or trigger on a number of counts (8 or 16). The logic for the counting mode works as follows:

1. Every time that an OCP event occurs, a counter increments. All three phases have dedicated counters.
2. If any counter (ORing) reaches the target value configured in CS_OCPFLT_CFG, then the fault is asserted and nFAULT pin is pulled low.
3. If before reaching the target value, the OCP event does not occur for 3 consecutive PWM cycles, the counter is reset to value 0, starting over next time an OCP event takes place.

6.1.5.3 OCP Fault Latching

The OCP fault can be configured as latched or non-latched. This defines how the fault is cleared via register write. If configured as latched:

- and in counting mode (8 or 16): fault cannot be cleared until there is one whole PWM period without fault
- and in immediate or on all events mode: fault can be cleared only after the fault condition is released.

If not latched, the fault can be cleared any time. If conditions is still present after clear, the fault will be set again after the clear event.

Independently of the latch configuration, the status register will show that the fault happened.

6.1.5.4 PWM Truncation

PWM truncation is a method to intrinsically limit the current flowing into the motor by switching off the PWM signal immediately after OCP detection. In this way, the GHx signals (all three) are pulled down automatically when the configured peak current level is reached. Low side remains unaffected until the PWM resets, increasing current in the motor again. This happens in a PWM cycle by cycle base. An example of how PWM truncation works, is depicted in detail in Figure 46.

Note: Truncation occurs always on high side except for 1PWM mode with alternate recirculation, where the truncation occurs in low side during high side recirculation periods.

If PWM truncation is active, PWM truncation takes place upon OCP event in all phases. For example, if the protection is triggered in current sense amplifier A, then PWM signals in phases A, B and C will be truncated. This will enable single shunt systems to utilize any of the current sense amplifiers.

Blanking is applied to truncation logic on both rising and falling edge of high side as described in Figure 43, see register CS_BLANK for blanking times. Blanking from all phases are OR'ed and prevent any miss-triggering of the PWM truncation during the blanking time selected by the user.

If truncation is enabled, the deglitching filter is automatically disabled. This means, if truncation is enabled, the nFAULT pin signalizes simply that a PWM truncation has occurred.

Attention: ***Depending on the PWM modulation utilized, PWM truncation might not provide the desired results. In modulation schemes where it is possible more than one phase are energizing the motor at a given time like SVM FOC (Space Vector Modulated Field Oriented Control), it is recommended to disable truncation and use OCP fault instead.***

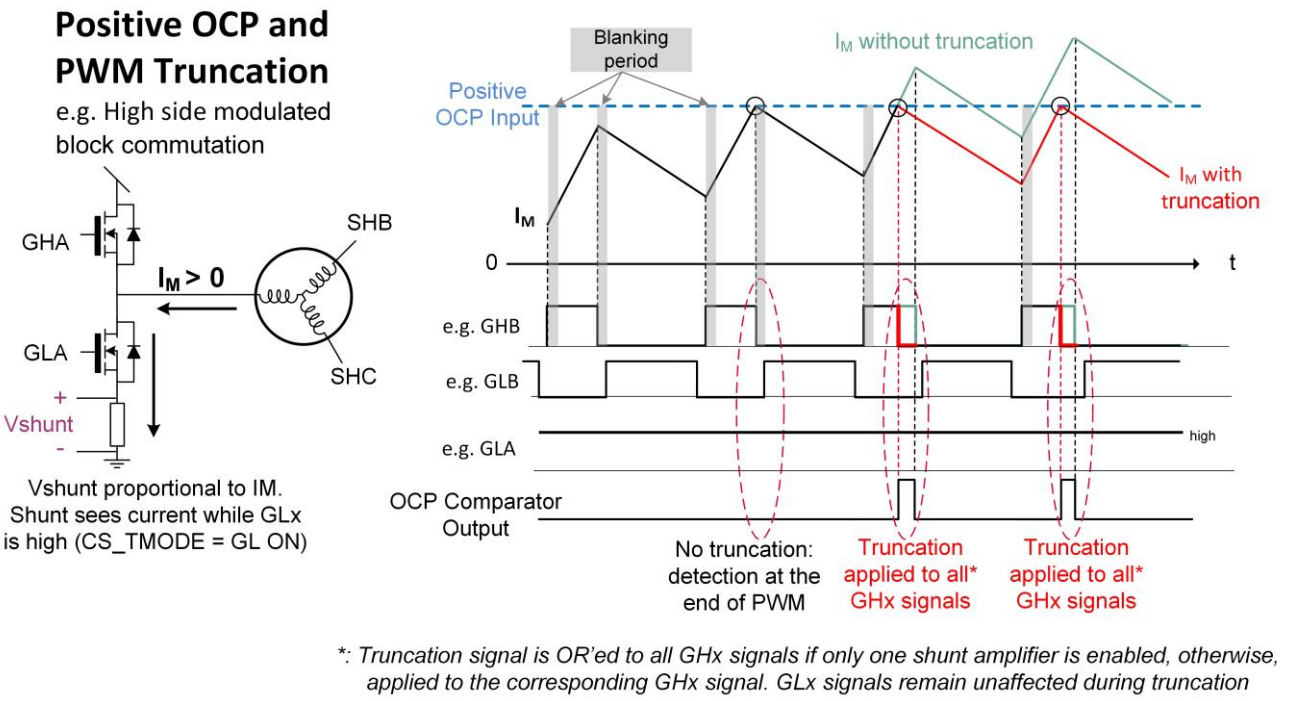

Figure 46 Positive OCP PWM truncation detail. I_M refers to motor current.

6.1.6 Current Sense Amplifier Gain Selection

During start-up of the system, user must program the desired gain of the current sense amplifier. To do this, user must write bitfield CS_GAIN_ANA to ensure digital programming of the gain and write as well CS_GAIN bitfield to set the actual gain. The actual value can be read in CS_GAIN_ST which reports the current gain value programmed. Gain of the shunt amplifiers can be programmed to one of the following values: 4, 8, 12, 16, 20, 24, 32 and 64.

Attention: ***Analog gain programming is not supported in IMD70xA devices. Default configuration is set to analog programming in 6EDL7141 and user must ensure to first change to digital programming and second to program desired gain before starting operation***

6.1.7 Current Sense Amplifier DC Calibration

MOTIX™ 6EDL7141 features a calibration method for the current sense amplifiers. This helps eliminate any unwanted offset in the output of the operational amplifiers before starting motor operation for example.

The activation of the DC calibration mode (only during ACTIVE state-EN_DRV high) via register CS_EN_DCCAL programming, will short the inputs of the amplifiers. Once the DC calibration is enabled, the output on CSOx pins can then be measured by precise ADC channels in XMC1404 AINx pins to record any possible offset in the system. Any excess voltage in CSOx pin from internal VREF voltage can be subtracted by XMC1404 embedded code from any future measurements. It is recommended to perform DC calibration before the PWM is started, when the current in the shunts, is known to be zero. This algorithm must be implemented by user.

Once the offset value is captured, XMC1404 must set CS_EN_DCCAL bitfield again to '0' to finalize the calibration process and reconnect the operation amplifier to the input pins. Then the PWM signals can start-up.

Note: During calibration mode, if Auto-Zero is enable it will be executed every 100µs instead of 200µs.

6.1.8 Auto-Zero Compensation of Current Sense Amplifier

Current sense amplifiers tend to accumulate offset during operation if they are not corrected. This can be due to temperature or the aging effects. The Auto-Zero feature of the current sense amplifiers provides an automatic way of compensating any possible drifts in the amplifiers. Internally the amplifier shorts the inputs to correct any possible offset excess for a t_{AUTO_ZERO} period of time. CSOx pin will hold the voltage before the Auto-Zero start during Auto-Zero period.

The Auto-Zero feature can be as well disabled via register bitfield AZ_DIS in register CSAMP_CFG.

6.1.8.1 Internal Auto-Zero

If configured as internally triggered or synchronized (by writing register bitfield CS_AZ_CFG), the Auto-Zero period starts with GHx signal rising edge after at least 100µsec from last Auto-Zero period (x depends on the activated current sense amplifier, A, B or C). The synchronized start of Auto-Zero period is chosen to interfere minimum possible with the shunt current sensing. When the high side MOSFET turns on, the low side MOSFET is off and therefore no signal should be present in the shunt in normal conditions, therefore not affecting the sampling of relevant information in the signal. Details of signals behavior example can be seen in Figure 42 or in Figure 47.

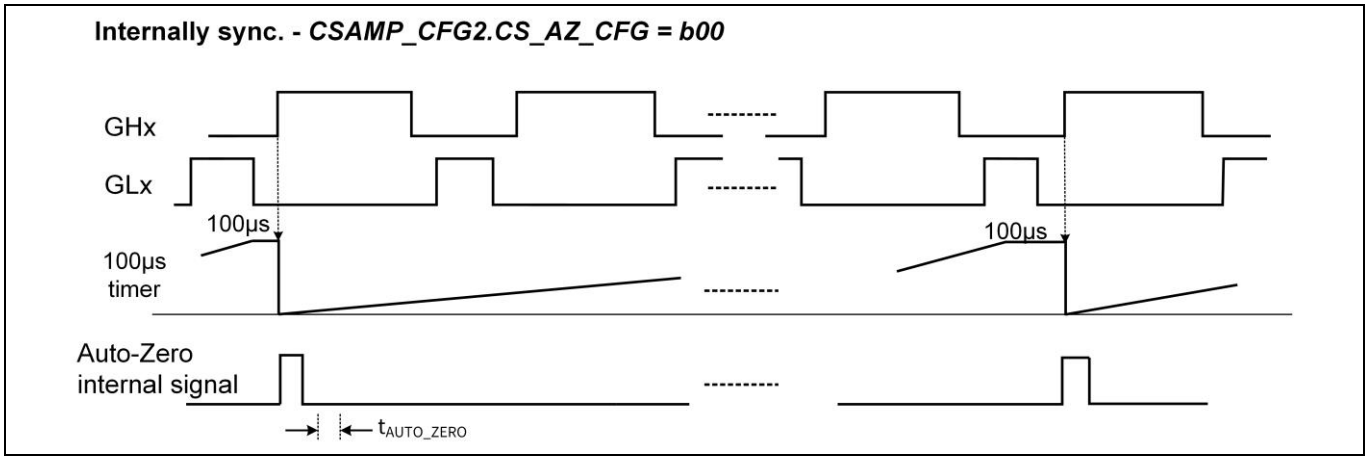

Figure 47 Auto-Zero operating modes. Auto-Zero occurs upon next GHx rising edge after timer has reached 100µs. Auto-Zero period will then rest the timer again

During start-up, the Auto-Zero function automatically activates to ensure that the amplifiers are optimized before the ACTIVE state is entered. This happens during charge pump start-up, this is from EN_DRV turn on until charge pump UVLO is reached.

If no GHx rising edge happens for a given time ($t_{AUTO\_ZERO\_CYCLE}$), for example if the low side is fully turned on for a long period in a 6-step commutation, then an internal watchdog will force an Auto-Zero compensation. Auto-Zero continuous during STANDBY state.

Note: When the Auto-Zero period finishes and the CSOx reconnects to the amplifier, it is expected to see a minor voltage glitch. This can be blanked or filtered out for example before the signal is provided to an ADC.

6.1.8.2 External Auto-Zero Synchronization via AZ Pin

User can enable external synchronization of the Auto-Zero function by writing register bitfield CS_AZ_CFG. In such case, the internal synchronization with GHx signals is disabled and the falling edge of pin AZ becomes the trigger for Auto-Zero correction period. This is depicted in Figure 48.

In IMD70xA, pin AZ is internally connected to pin P1.2. If externally triggered, XMC1404 can decide according to the particular current sense method when to execute the Auto-Zero correction by activating P1.2. Thanks to this feature the Auto-Zero effect can be moved, for example, far from the ADC sampling in XMC benefitting from the corrections but still being able to sample without the interference of the Auto-Zero process.

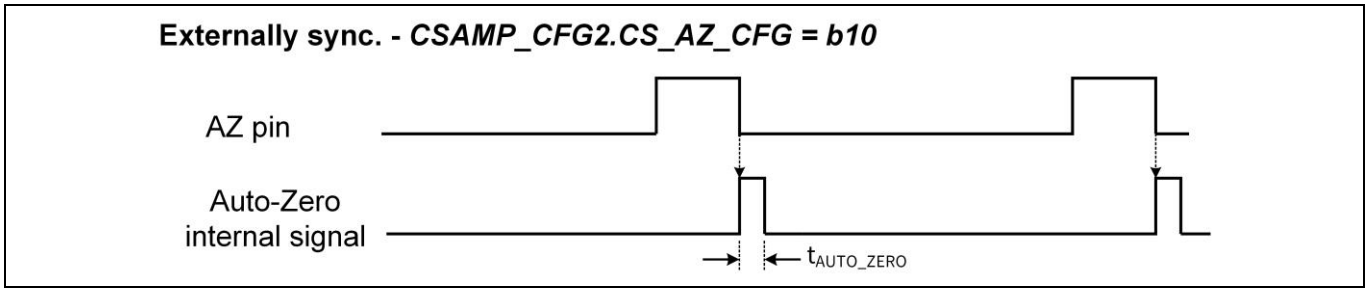

Figure 48 Auto-Zero functionality with external synchronization. AZ pin falling edge will trigger the Auto-Zero correction period

6.1.8.3 External Auto-Zero Synchronization via AZ Pin with Enhanced Sensing

MOTIX™ 6EDL7141 to stop the clock (clock gating) of the charge pump modules according to AZ pin state. If this feature is activated, the charge pumps clock will be gated from the rising edge of AZ pin until end of Auto-Zero period that starts after falling edge of same pin. The effect of the clock gating is the reduction of possible switching noise that can couple into PCB sensitive signals like CSOx or other ADC measured voltages by XMC1404.

Attention: During clock gating period, the charge pump stops operation. As a result, VCCLS and VCCHS rails stops regulation and can drop their regulated voltages. In most cases, VCCLS and VCCHS capacitors will maintain enough voltage to keep driving efficiently the MOSFETs. User must check that Recommended Operating Conditions and MOTIX™ 6EDL7141 Electrical Characteristics are respected. UVLO protections on both VCCLS and VCCHS are present in case a malfunction takes place, protecting the inverter

The operation of charge pump clock gating mode is shown in Figure 49.

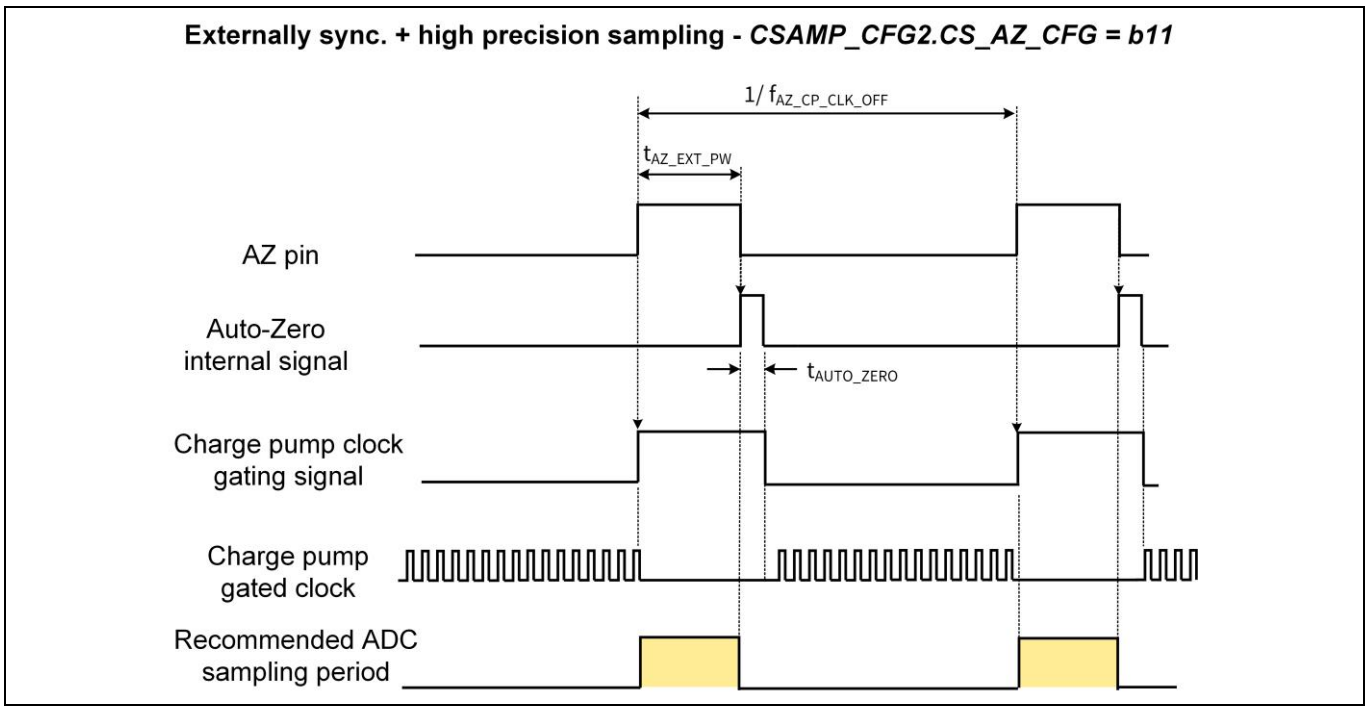

Figure 49 Signal diagram for the enhanced sensing mode using external synchronization of Auto-Zero function. The charge pump clock is gated to reduce switching noise coupling during periods where sensitive measurements are performed in the system like the ADC in XMC1404 or other external sampling circuits

7 MOTIX™ 6EDL7141 House-Keeping Functions

7.1 Hall Comparators

Hall comparators are designed to be used in 1PWM mode with Hall sensors or emulated signals from XMC1404, described in section 4.1.4 as well as for ‘locked rotor’ detection functionality described in 7.2.3.

The Hall inputs are digitally deglitched. That means those inputs ignore any extra Hall transitions for a configurable period of time. This is selected in bitfield HALL_DEGLITCH that can be accessed via SPI commands. This prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

The polarity of the Hall sensor inputs can be read at any time in register FUNCT_ST, bitfield HALLIN_ST.

7.2 Watchdog Timer

MOTIX™ 6EDL7141 integrates three independent watchdog timers that are SPI configurable. These are protection features used to ensure the correct functionality of different modules inside and outside the device, e.g. to ensure that XMC1404 is having correct behaviour by serving or ‘kicking’ the watchdog. To configure watchdog timers two registers are available: WD_CFG and WD_CFG2. The three independent watchdog timers are:

- Buck converter watchdog:
- General purpose watchdog
- Rotor locked watchdog

Each watchdog timer core unit includes a digital timer (watchdog timer). A source signal is connected to that timer which resets whenever a toggle occurs on the signal. Otherwise the timer keeps counting up. If the watchdog timer limit is reached without a reset input, then a fault takes place and action will be performed according to Table 25.

The reaction to a watchdog fault is programmable to following actions:

- Reporting to status register only.
- Reporting to status register and nFAULT pin connected internally to XMC1404 (pin P3.4).
- Trigger a configurable braking event.
- Select whether watchdog fault is latched or not.

An example of watchdog operation is presented in Figure 50. In this example, a generic signal ‘WD_Input’ is resetting the counter periodically (for example when reading the status register). If the input signal stops toggling, the watchdog timer expires after the watchdog period resulting in a watchdog fault.

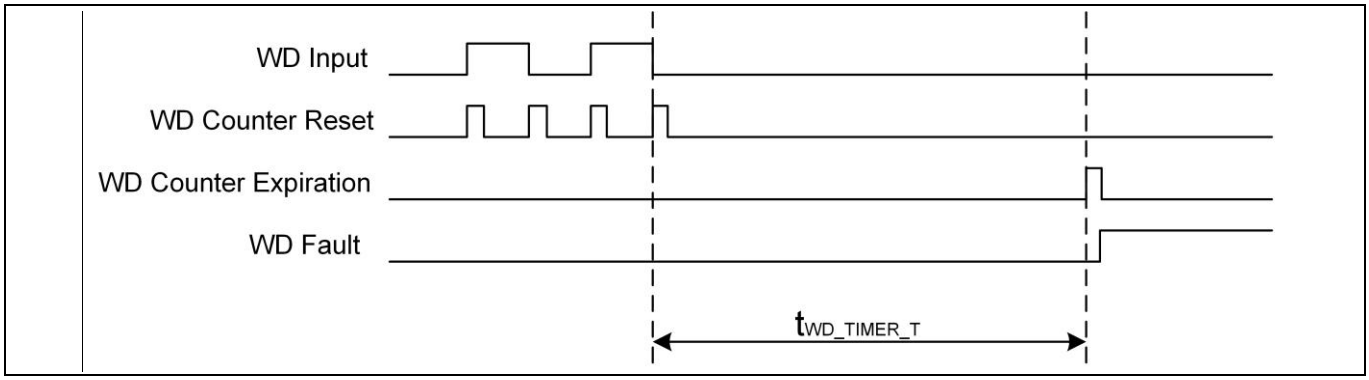

Figure 50 Watchdog operation diagram

7.2.1 Buck converter watchdog

During start-up of the device, this watchdog monitors VDDB UVLO signal. When UVLO of VDDB is asserted, the watchdog is cleared. If UVLO of VDDB is not asserted within the watchdog period ($t_{WD\_BUCK\_T}$), the system will stop (STOP state in the state machine is described in section Device Start-up and Functional States) and stay disabled until a power cycle takes place. This watchdog can be used for safe start-up debugging. To enable this feature WD_CFG2, bitfield WD_BK_DIS needs to be accessed.

7.2.2 General Purpose Watchdog

This watchdog timer can be configured to use different general purpose inputs (timer reset signal) via register WD_INSEL. Possible inputs are:

- ***EN_DRV: this is the default input. Due to connectivity between XMC1404 and 6EDL7141, it is not possible to generate a clock in EN_DRV pin. Therefore, this input must not be used.***
- **DVDD start-up**: during start-up, if this input is selected, the watchdog will be cleared upon DVDD UVLO signal assertion. If DVDD has not reached the correct value before the watchdog period, the DVDD regulator will retry to start. The number of attempts to restart DVDD regulator when start-up fails, can be configured in WD_DVDD _RSTRT_ATT. Additionally, the time between restarts attempts is set in bitfield WD_DVDD_RSTRT_DLY
- **Charge pumps start-up**: similarly, the start-up time of the charge pumps (both) can be monitored. The UVLO signal of both VCCHS and VCCLS will clear the watchdog, otherwise, a fault will be reported. To select this input, bitfield in WD_INSEL has to be set accordingly.
- **Status register SPI read action**: in this configuration, the watchdog resets every time the FAULT_ST status register is read via a SPI command. In this way, it checks that XMC1404 is active and that the SPI communication is working adequately.

The general purpose watchdog timer needs to be enabled via WD_EN bitfield. Watchdog period programmed din WD_TIMER_T.

Brake on General Purpose Watchdog Fault

The general purpose watchdog timer can be configured to trigger a brake event when the comparator trips. This is activated in bitfield WD_BRAKE and is only possible when ‘Status register read’ is chosen as input. The brake event can be configured to either brake the motor by shorting all high side MOSFETs, all low side MOSFETs, alternate between those options or set all MOSFETs to high Z. This is explained in more detail in sections 4.1.6. This is configured in bitfields BRAKE_CFG in PWM_CFG register.

7.2.3 Locked-Rotor Protection Watchdog Timer

MOTIX™ 6EDL7141 provides a locked or stalled rotor protection function by integrating a dedicated watchdog timer. The rotor locked watchdog timer inputs are signals INLA, INLB and INLC. XMC1404 firmware needs to provide the Hall sensor signal copy into those pins. This protection is only possible when using Hall sensor based control schemes or 1PWM modes.

Locked or stalled rotor can occur in the event of a mechanical malfunction or excessive load torque that causes the motor to stop rotating while enabled. The locked rotor function can be enabled by setting the bitfield WD_RLOCK_EN to b’01.

A locked rotor condition is detected if the Hall pattern is maintained for t_{LOCKED} period. The t_{LOCKED} time is configured via SPI (bitfield WD_RLOCK_T).

In order to increase robustness, an especial case of rotor locked detection is implemented. In some cases, the motor stalls in a position in which the Hall sensors can still provide a cyclic or repeated toggling. In some cases

vibration or bending of the motor can cause this effect, in other cases, the Hall sensors get stalled close to the magnets. The internal logic detects this condition as rotor locked. An example is of such Hall sensor inputs sequence that would report a fault is the following:

100, 101, 100, 101, 100, 101, …..

As soon as the locked rotor condition is detected, the device sets bitfields WD_FLT and RLOCK_FLT of the FAULT_ST register to b'01. Upon detection of locked rotor condition the device enters high impedance state (high Z). Additionally, nFAULT pin will be pulled down. XMC1404 can read this signal (internally connected) and request a status update to the device or execute other corrective actions.

Hall Sensor Malfunction

In case of Hall sensor failure, the rotor locked protection can help to bring the motor to a safe state. The malfunction of 2 or 3 Hall sensors (erroneous operation of the GPIOs emulating the Hall sensors) will cause a rotor lock fault in 6EDL7141, however, a single Hall sensor failure cannot be detected as malfunction and does not trigger a fault.

The rotor locked condition can be reset by toggling EN_DRV (switch off and on again).

Hall Comparators when PWM Signals are on Hold

If the PWM input signals generated by the controller stop switching while the rotor locked protection is enabled, 6EDL7141 will recognize this as a failure and it will trigger the rotor locked protection after t_{LOCKED} period. In case this behavior is not desired, the user code in the controller that stopped the PWM switching must be preceded by a command (SPI) to disable the rotor locked protection.

7.3 Gate Driver ADC Module-Analog to Digital Converter

MOTIX™ 6EDL7141 integrates an ADC based on SAR architecture with 7 bits resolution. This ADC can be used to do redundant measurements to those executed in the XMC1404 controller or to measure gate driver related voltages. XMC1404 can request the results of these internal measurements via SPI reads of ADC_ST register. The ADC can measure following inputs during ACTIVE mode:

- Automatically in ADC conversion sequence:
  - On die **temperature** sensor (see 7.3.2)
  - **PVDD:** supply voltage
  - **VCCLS:** low side gate driver supply
  - **VCCHS:** high side gate driver supply
- Other (on demand) conversion inputs selected via bitfield ADC_OD_INSEL :
  - **$I_{DIGITAL}$:** device digital section current consumption
  - **DVDD:** linear regulator output voltage
  - **VDDB:** buck converter output voltage

Those ADC inputs are continuously converted in sequence. After each conversion is finished, the result of the conversion can be processed through integrated digital filters. These are moving average filters with configurable number of samples. PVDD uses a dedicated filter (ADC_FILT_CFG_PVDD) while the rest share a second filter (ADC_FILT_CFG). The complete architecture of the ADC module is depicted in Figure 51.

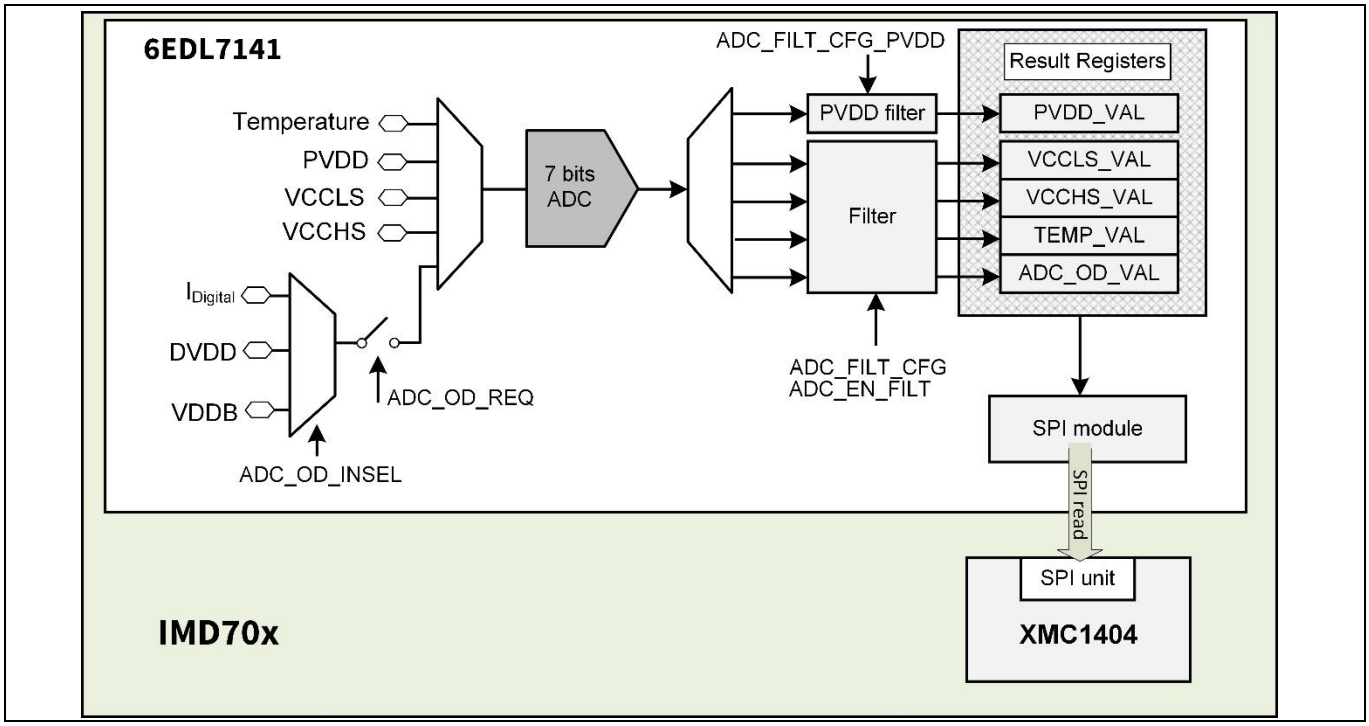

Figure 51 ADC module block diagram

Table 24 summarizes the ADC inputs characteristic including the scaling factors. These scaling factors can be used by XMC1404 firmware to calculate back the real analog values in volts, amperes or degree Celsius.

Table 24 ADC measurements overview

Measurement	On demand conversion	Bitfield	Filter - register	Scaling factor
PVDD	N	PVDD_VAL	ADC_FILT_CFG_PVDD	$= (0.581 * PVDD_{VAL} + 5.52)\ V$
Temperature	N	TEMP_VAL	ADC_FILT_CFG	$= (2 * TEMP\_VAL - 94)$℃
VCCLS	N	VCCLS_VAL	ADC_FILT_CFG	$= VCCLS\_VAL * \frac{16}{127} V$
VCCHS	N	VCCHS_VAL	ADC_FILT_CFG	$= VCCHS\_VAL * \frac{16}{127} V$
Device current (I_{PVDD})	Y	ADC_OD_VAL	ADC_FILT_CFG	$= (0.24 * ADC\_OD\_VAL) mA$
DVDD	Y	ADC_OD_VAL	ADC_FILT_CFG	$= ADC\_OD\_VAL * \frac{DVDD_{TARGET}}{127}\ V$
VDDB	Y	ADC_OD_VAL	ADC_FILT_CFG	$= ADC\_OD\_VAL * \frac{VDDB_{TARGET}}{127}\ V$

For example, if DVDD voltage is the desired parameter, XMC1404 will read via SPI register ADC_OD_VAL. With DVDD equal to 5V (IMD701A example) if the reading was 0x78=120 decimal value. XMC1404 controller can easily calculate the following:

$$DVDD = ADC\_OD\_VAL * \frac{5.0V}{2^7} = 120 * \frac{5.0V}{127} = 4.72V \quad (7)$$

7.3.1 6EDL7141 ADC Measurement Sequencing and On Demand Conversion

In ACTIVE state, the ADC converts repeatedly in loop the following sequence of 6 measurements:

1. PVDD
2. Temperature sensor
3. PVDD
4. VCCLS
5. PVDD
6. VCCHS

This is shown in Figure 52. Results of those conversions will be placed in the dedicated result registers that can be read via SPI by the XMC1404. PVDD result is reported in SUPPLY_ST register, VCCLS and VCCHS are reported in register CP_ST and the temperature measurement is reported in register TEMP_ST.

Additional to the standard sequence, the user can select to have other signals converted on demand. Any of this “on demand” conversion inputs, can be injected once in the standard sequence. This is done by selecting the signal to be converted in bitfield ADC_OD_INSEL, and setting to ‘1’ the request bitfield ADC_OD_REQ.

Note: The write of ADC_CFG bitfields must happen in a single SPI write. A write to a single bitfield will overwrite the rest to the default value, so the full desired register value must be given in a single write or via read-modify-write sequence.

If an on demand conversion is requested, the ADC waits to finish (End Of Conversion) any running conversion. Then the requested on demand conversion is started. When the on demand conversion is finished, bitfield ADC_OD_RDY is set. XMC1404 code can poll this bitfield to make sure the result register contains newest value of the requested conversion. The result of the on demand conversion is located in bitfield ADC_OD_VAL and the sequence continuous right where it was interrupted after the EOC of the on demand conversion. This is illustrated in Figure 52.

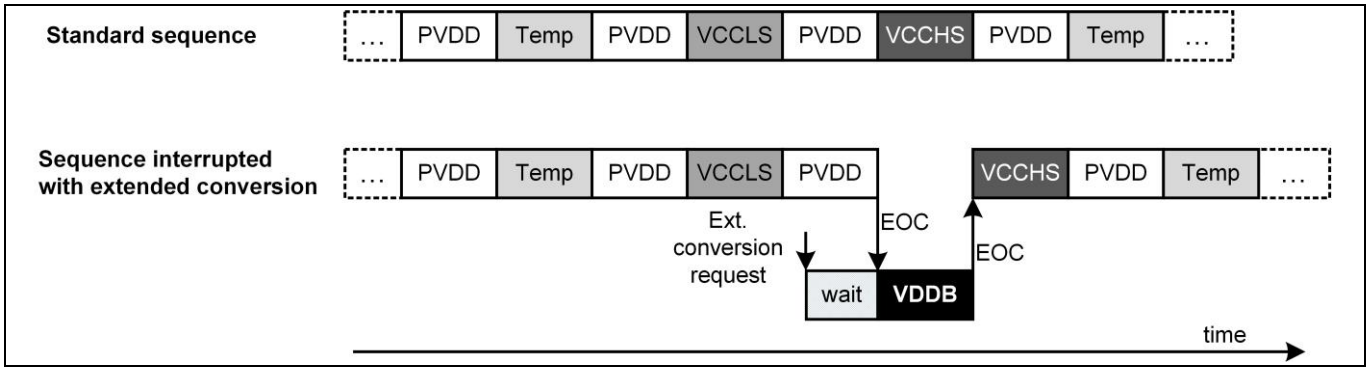

Figure 52 ADC sequencing and interruption by extended conversion request of VDDB signal

7.3.2 Die Temperature Sensor

An especially useful ADC measurement is the temperature of the die. The temperature of the device can be read via SPI by accessing bitfield TEMP_VAL in TEMP_ST register. The value is measured with a resolution of 2 degrees Celsius. Additionally, over-temperature warning and faults are implemented. In register SENSOR_CFG (OTS_DIS), the over-temperature shut down protection can be disabled. The threshold values are provided in Table 11. The occurrence of these faults can be detected by reading bitfields OTW_FLT and OTS_FLT.

According to Table 24, an example reading of 0x4A = 74 would convert into:

$$Temperature = TEMP\_VAL * 2°C - 94°C = 74 * 2°C - 94°C = 54°C \quad (8)$$

8 MOTIX™ 6EDL7141 Protections and Faults Handling

MOTIX™ 6EDL7141 contains an extensive number of protections. These are:

- Over-Current Protections (OCP) for:
  - DVDD linear regulator
  - Buck converter
  - Motor leg shunt OCP
- Under-Voltage Lock Out (UVLO) protection for:
  - Gate driver supply voltage both high side and low side drivers
  - Supply voltage PVDD
  - DVDD linear regulator output voltage
  - Buck converter output voltage
- DVDD linear regulator Over Voltage Lock Out (OVLO) protections
- Rotor locked detection based on Hall sensor inputs
- Configurable watchdog
- Over-Temperature Shutdown (OTS) and Warning (OTW)
- OTP memory fault.

An arbitration state machine, takes all the fault inputs from the specific fault blocks and decides which fault needs to be serviced first in case several faults occur at same time (same clock cycle). Once a fault is acknowledged, the system takes the specific action as shown in Table 25 and the arbitration round stops until the fault is cleared.

The state machine is split in two main independent arbitration sections:

- **Supply faults** (B0 to B4). B0 is highest priority.
- **Other faults** (F0 to F7). The fault that happens first will be dealt first and others will be ignored until this fault is removed. If more than one fault happens at the same time, then the one with the highest priority will be processed. (F0 is highest priority).

The resultant actions from both sections are OR'ed on nFAULT.

Additionally to any possible actions like switching off PWM signal, status bits will be updated to inform XMC1404 of any warning or/and fault occurrence. This is done regardless of priority and those status bits can be read via SPI commands by the microcontroller in the system.

Note: It is highly recommended to understand faults reason by reading the status registers and clear faults as soon as they occur so new events can be captured. This is done by writing register FAULTS_CLR via SPI interface

Following registers provide information on the status of the device faults:

- FAULT_ST: holds most of functional related faults. A fault might be triggered only after a number of events of a malfunction. Status will immediately record the event information.
- TEMP_ST: provides status on temperature warning and the temperature reading itself
- SUPPLY_ST: reports on status of all supplies UVLO/OVLO and OCPs
- FUNC_ST: status of OCP faults for each of current sense amplifiers, Hall sensors, wrong hall pattern.
- OTP_ST: programming and reading of OTP related faults

In order to clear faults the user has to write via SPI the bitfield CLR_FAULTS in FAULTS_CLR register. However, to clear a latched fault, a write to CLR_LATCH register is required.

If ‘Motor leg shunt OCP’ fault is programmed to be latched the fault cannot be cleared until:

- If in OCP counting mode (8, 16 periods) there is one whole PWM period without an OCP event or STANDBY state is entered.
- If in immediate trigger mode then it can be cleared after the fault is gone.

Table 25 6EDL7141 faults and protections table

Name	Description	Programmability	Latched	nFAULT report	Active State	Prio	Action(s)
VCCLS UVLO	Charge pump low side UVLO fault	-	N	Y	DEV_ ACTIVE	F1 & F2 (shared)	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65
VCCHS UVLO	Charge pump high side UVLO fault	-	N	Y	DEV_ ACTIVE	F1 & F2 (shared)	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65
DVDD OVLO	DVDD OVLO fault	-	N	Y	All states after DVDD ok (after STANDBY)	B1	No action. XMC1404 to perform user action
DVDD OCP	DVDD OCP fault	Threshold level	N	Y	All states after DVDD ok (after STANDBY)	B3	No action. XMC1404 to perform user action
DVDD UVLO	DVDD UVLO fault	-	N(requires power cycle-CE toggle)	Y (however is nFAULT supplied by DVDD)	All states after BUCK_ START	B0 and F0	• Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. *Note: the behavior can be interrupted depending on DVDD as logic is supplied by it*. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65. These are always active. • Waits for power cycle (CE pin low and high) • Buck converter continues operation • When DVDD UVLO happens the functional state machine changes from DEV_ACTIVE to DVDD_STOP. Please refer to section Device Start-up and Functional Statesfor details. From the application perspective, this fault is highest priority. Requires a power cycle (CE toggle)

Name	Description	Programmability	Latched	nFAULT report	Active State	Prio	Action(s)
BUCK OCP	Buck Converter Over Current Protection	-	N	Y	All states after DVDD ok (after STANDBY)- Fault blanked during charge pump start	B2	• No action. XMC1404 to perform user action. Protection is blanked during start-up of charge pumps
Motor leg shunt OCP [2:0]	Current sense amplifier Over Current Protection for each phase	Threshold level, count on number of trips, reaction, PWM truncation	Programmable- Latched if brake on OCP is active	Y	DEV_ ACTIVE	F4	• PWM truncation if configured. • If fault is configured as “Latched” then: gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65 • Brake as defined in PWM_CFG register when CS_OCP_BRAKE register enabled. Fault latched if braking active
Locked rotor	Locked rotor watchdog overflow	Timing	Y	Y	DEV_ ACTIVE	F5	• Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65 • Requires toggle of EN_DRV to re-start normal operation again
Watch dog timers	Watchdog timer overflow. Several inputs programmable	Timing, reaction. Depending on input	Programmable-Latched if brake on watchdog fault is enabled	Y (with input EN_DRV only, otherwise not)	Depending on input, either START-UP or DEV_ACTIVE	F6	If input: • EN_DRV - gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown inFigure 65. • Buck input- No action required from user or device.

Name	Description	Programmability	Latched	nFAULT report	Active State	Prio	Action(s)
							• If charge pump input – nFAULT reported. Driver won't start-up. • Others: brake as defined in PWM_CFG register when WD_BRAKE register enabled. Always latched if braked enabled
OTS	Over Temperature Shutdown	-	Y	Y	DEV_ ACTIVE	F3	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65
OTW	Over Temperature Warning	-	N	N (only status register report)	DEV_ ACTIVE	F8	No action. XMC1404 to perform user action
OTP Fault	OTP read fault or OTP user programming error	-	Y	Y	All states	F7	Gate signals (GHx, GLx) pulled down according to configured gate driver slew rate. After that, gate signals are pulling down according to $R_{GS\_PD\_WEAK}$ and $R_{GS\_PD\_STRONG}$ as shown in Figure 65

9 MOTIX™ 6EDL7141 Programming-OTP and SPI interface

Programming of 6EDL7141 features in MOTIX™ IMD70xA requires accessing internal registers via SPI interface shown in Figure 53.

The configuration of 6EDL7141 features, including gain of amplifiers, driving voltage for gate drivers or fault reactions, is stored in registers while the device is active. The configuration of those functions can be changed during run time operation via SPI commands. These registers are volatile memory cells and therefore, its information will be lost every time the power supply is removed from the device.

For this reason, 6EDL7141 integrates an OTP NVM (One Time Programmable Non-Volatile Memory) that stores a given default configuration even when power supply is not available. Initially the device is programmed with the default register settings provided in section 11. During startup phase of the device (see state machine flowchart in Figure 58), the configuration in the OTP will be copied or mirrored into registers. These registers are the ones that govern the actual behavior of the device. This is shown in Figure 53.

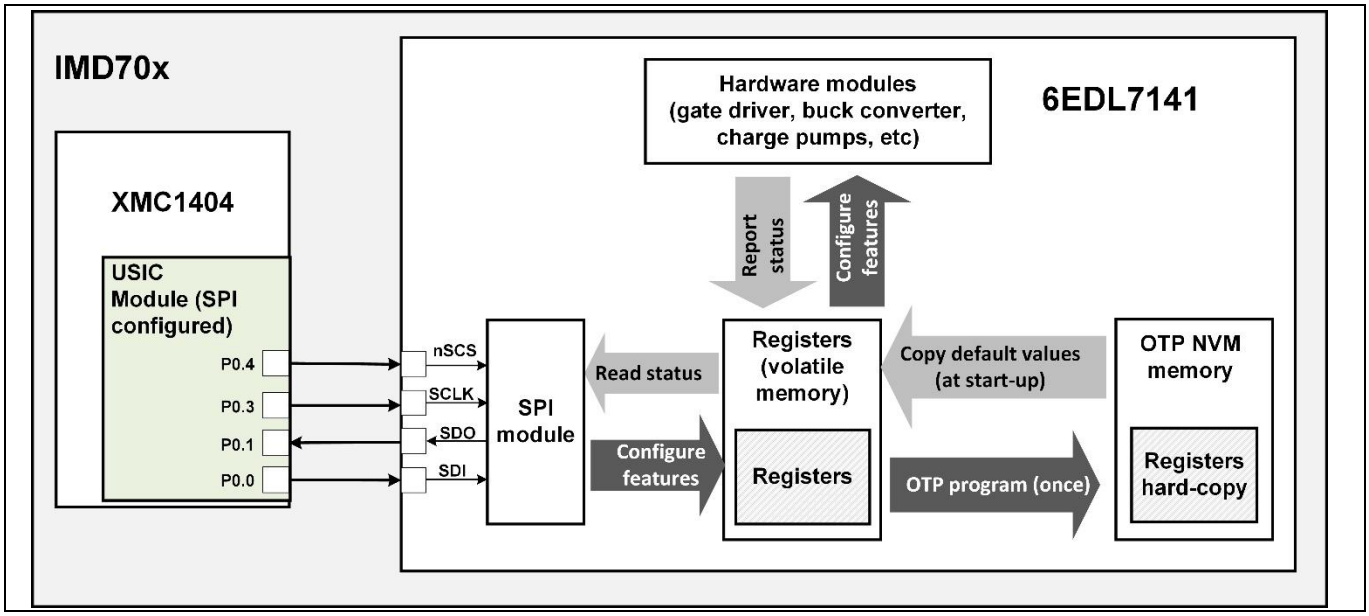

Figure 53 6EDL7141 programming overview

In case the default (“out of the fab”) configuration of the device stored in OTP is not the desired one, the designer can select a different configuration for its application and store it indefinitely in the OTP memory (hard-copy). See section 9.1.1 for detailed procedure. This action can be done only once. A second write to the OTP is not possible. However, configurations can be overwritten on volatile registers after start-up via SPI commands as mentioned above.

The user configuration can be tracked thanks to a software ID bitfield -USER_ID- located in OTP_PROG register.

Note: It is therefore recommended that every writing action to the registers is followed by a confirmation read to ensure that written and read data in registers match and thus confirming correct programming.

9.1.1 MOTIX™ 6EDL7141 OTP User Programming Procedure: Loading Custom Default Values

The OTP is used for user configuration storage. The OTP module implements a double error correction, plus one additional error detection when programming it.

OTP programming must only occur in a controlled environment. This requires the user to ensure that programming happens at the correct supply voltage, this is PVDD> $PVDD_{OTP\_PROG}$. Also the temperature must be below T_{OTP_PROG}. Internally both parameters are monitored. This means that if programming is attempted outside of these parameters it will not be started. If this blocking occurs, then bitfield OTP_PROG_BLOCK will be set to '1' to indicate that one of the parameter is outside of the required range. Default values (as given in bold in section 11.4) will be used after start-up in such situation. Further programming attempts are possible. OTP_PROG_BLOCK will be reset either when the programming finishes successfully or after a power down.

Following programming steps should be performed to write OTP with a specific configuration:

1. Start device into STANDBY mode (EN_DRV< $V_{EN\_DRV\_TH}$)
2. Write registers to the desired default values via SPI write commands
3. Program these values into OTP using OTP_PROG bitfield
    a. If the temperature is higher than T_{OTP_PROG} or PVDD < $PVDD_{OTP\_PROG}$, then programming does not start and OTP_PROG_BLOCK is set to '1'. Conditions might be modified and the programming can be attempted again. If the programming fails twice, the device will be blocked signaled by OTP_USED=b'1, OTP_PASS = b'0
    b. If temperature and PVDD values are in range, programming starts, copying register parameters into the OTP memory. This can only be done once.
4. (Recommended) Check if OTP programming succeeded via bitfields OTP_USED and OTP_PASS or OTP_PROG_FAIL:
    a. If the programming of the OTP failed, then the device will be locked until a power cycle (CE pin pulled down and up) takes place. Signaled by OTP_USED=b'1 and OTP_PASS = b'0 or simply OTP_PROG_FAIL =b'1. Further programming of OTP is not possible. Memory content is considered corrupted and therefore the part should be discarded.
    b. If programming succeeded, then normal function will continue. This is signaled by OTP_USED = b'01 and OTP_PASS = b'01 or simply OTP_PROG_FAIL = b'0. It is recommended to perform a power cycle (CE pin pulled down and up) for new values to take effect after a successful programming

Trying to write an already programmed OTP will be ignored.

An OTP programming failure (wrong copy of registers into OTP memory) will force the device to enter STOP state during read out (see Figure 58). In such case, the fault is reported on nFAULT pin and XC1404 can perform a status read of 6EDL7141 to provide status of memory by reading bitfields OTP_USED, OTP_PASS, or OTP_PROG_FAIL, and OTP_PROG_BLOCK. The OTP possible statuses are described in Table 26.

If the user chooses to program OTP during start-up of the XMC1404 software, this should check each time that OTP_USED = b'01 before programming again. Otherwise incorrect programming could occur.

Table 26 OTP programming status

Device status	OTP_USED	OTP_PASS	OTP_PROG_BLOCK	OTP_PROG_FAIL	Status Description
Non-programmed device	0	0	0	0	Default values used
Successful programming of OTP	1	1	X	X	User programming was successful. Upon start-up, the newly programmed default values will be loaded into registers for custom configuration
Programming blocked due to PVDD or temperature conditions	0	0	1	0	Part can be reprogrammed once condition are within limits
Programming started but failed due to PVDD or temperature conditions	1	0	1	1	Part must be discarded
Programming started but failed due to OTP issue	1	0	0	1	Part must be discarded

9.1.2 MOTIX™ 6EDL7141 SPI Communication

All communication between XMC1404 and 6EDL7141 happens through the internal connection between both devices as shown in Interconnects Pin Description table. The SPI module in 6ELD7141is used to program the configuration registers and therefore to command the device for example to change settings or program OTP memory.

6EDL7141 SPI module is based on a 4-pin configuration. Data sampling happens during the falling edge of the SPI clock signal. This protocol can easily be implemented in XMC1404 USIC peripheral when configuring it as SSC channel. User must ensure that XMC1404 is properly configured according following write and read protocols.

All communication happens in a 24 bit length shift register.

- 7 bit address
- 16 bit data byte
- 1 bit command

Data is shifted in with MSB first.
Two commands are defined:

- 1 – Register write
- 0 – Register read

Figure 54 and Figure 55 show respectively write and read operations with SPI interface.

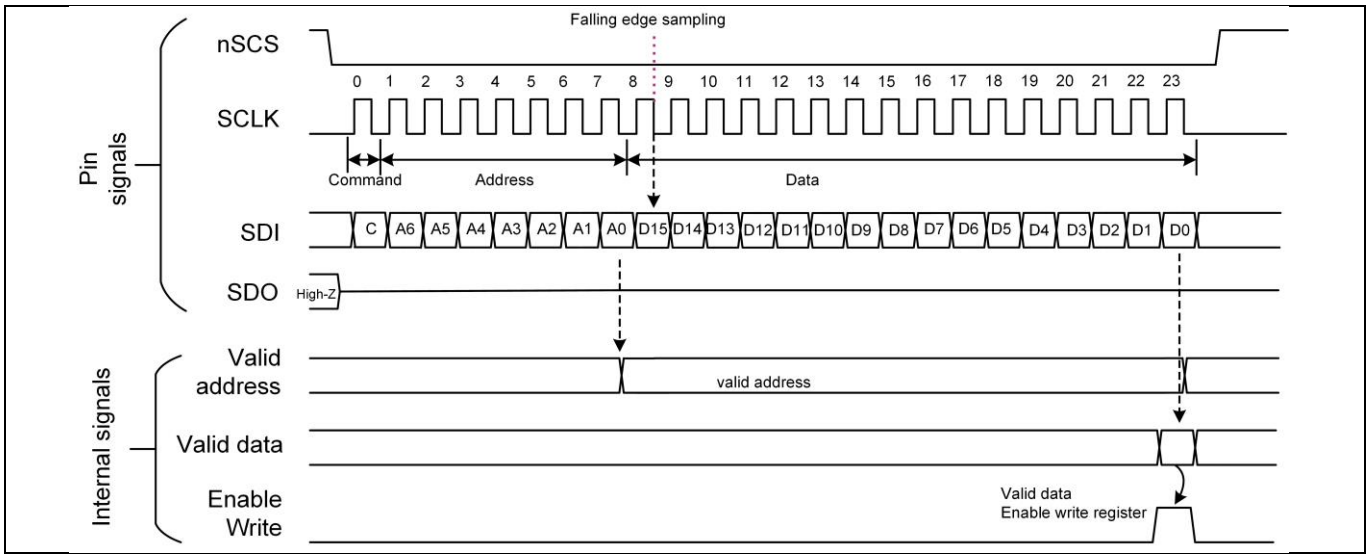

Figure 54 SPI write operation

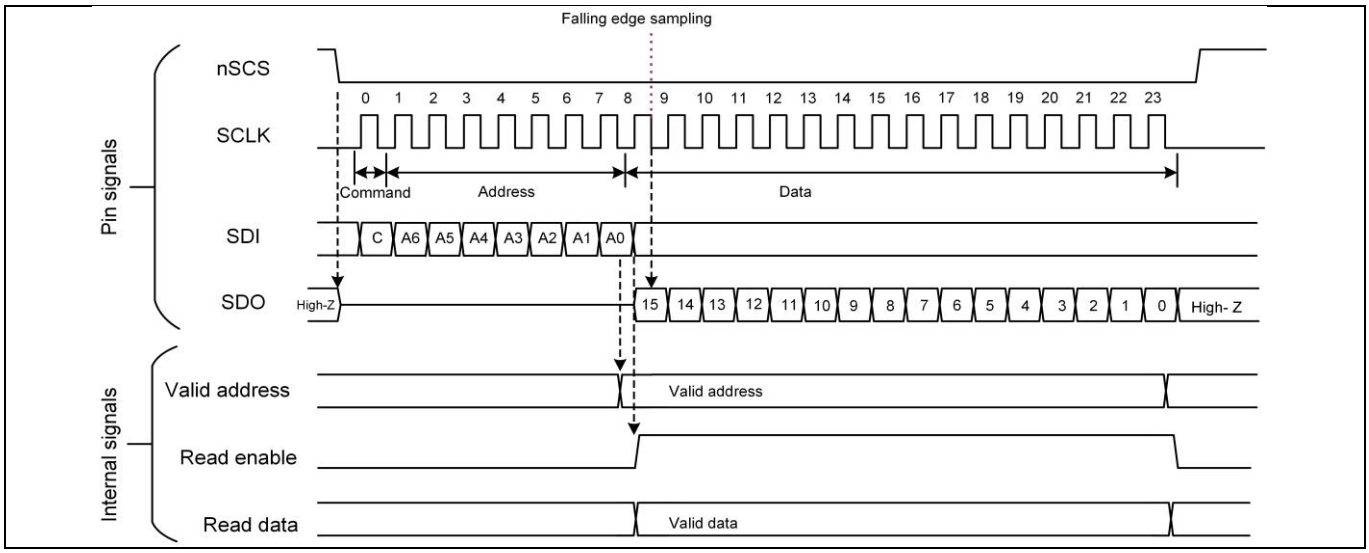

Figure 55 SPI read operation

9.1.2.1 SPI Communication Example

If for example, user wants to write new values TDRIVE1 = 50ns (0x01) and TDRIVE2 = 2540ns (0xFE), to register TDRIVE_SRC_CFG (address 0x19), then the content of the register needs to be 0xFE01 by collating TDRIVE2 and TDRIVE1 values. The microcontroller then needs to write following command in the SPI bus (SDI signal) once nSCS signal is pulled down:

Binary: b 1001 1001 1111 1110 0000 0001

Hexadecimal: 0x99 FE 01

If after write, a read is necessary, the following sequence must be applied by the microcontroller. This will read TDRIVE_SRC_CFG register by writing SDI signal:

Binary: b 0001 1001 ---- ---- ---- ----

Hexadecimal: 0x19 -- --

9.1.2.2 XMC1404 SPI Configuration Recommendation

In this section it is described the recommended configuration of XMC1404 USIC channel to communicate with 6EDL7141 interface. For this purpose, XMC Low Level Drivers have been used. APIs supported in by that library can be identified by the prefix “XMC_”, like XMC_GPIO_Init(). Three APIs are shown here:

- USIC SPI channel Initialization
- Read command
- Write command

USIC SPI channel Initialization

```
/*******************************************************************************
 * DATA STRUCTURES
*******************************************************************************/
uint8_t error_SPI;

/* SPI configuration structure */
XMC_SPI_CH_CONFIG_t spi_config =
{
  .baudrate = SPI_BAUD_RATE,
  .bus_mode = XMC_SPI_CH_BUS_MODE_MASTER,
  .selo_inversion = XMC_SPI_CH_SLAVE_SEL_INV_TO_MSLS,//Slave select active
low
  .parity_mode = XMC_USIC_CH_PARITY_MODE_NONE
};

/* GPIO SPI TX pin configuration */
XMC_GPIO_CONFIG_t tx_pin_config =
{
  .mode = XMC_GPIO_MODE_OUTPUT_PUSH_PULL_ALT9 //Pin selection ALT9
};

/* GPIO SPI DX pin configuration */
XMC_GPIO_CONFIG_t dx_pin_config =
{
  .mode = XMC_GPIO_MODE_INPUT_TRISTATE
};

/* GPIO SPI SELO pin configuration */
XMC_GPIO_CONFIG_t selo_pin_config =
{
  .mode = XMC_GPIO_MODE_OUTPUT_PUSH_PULL_ALT8, //Pin selection ALT8
};
```

```
/* GPIO SPI SCLKOUT pin configuration */
XMC_GPIO_CONFIG_t clk_pin_config =
{
  .mode = XMC_GPIO_MODE_OUTPUT_PUSH_PULL_ALT8, //Pin selection ALT8
};

/* API to initialize USIC SPI peripherals */
void spi_master_init(XMC_USIC_CH_t * const channel)
{
/* Initialize GPIO */
  XMC_GPIO_Init(MOSI_PIN, &tx_pin_config);
  XMC_GPIO_Init(MISO_PIN, &dx_pin_config);
  XMC_GPIO_Init(SELO_PIN, &selo_pin_config);
  XMC_GPIO_Init(SCLK_PIN, &clk_pin_config);

 /* Initialize SPI master*/
  XMC_SPI_CH_Init(channel, &spi_config);
  XMC_SPI_CH_SetWordLength(channel, SPI_WORD_LENGTH);
  XMC_SPI_CH_SetFrameLength(channel, SPI_FRAME_LENGTH);
  XMC_SPI_CH_SetBitOrderMsbFirst(channel);
  XMC_SPI_CH_EnableSlaveSelect(channel, XMC_SPI_CH_SLAVE_SELECT_0); //Falling
sclk sampling and no polarity inversion

  XMC_SPI_CH_ConfigureShiftClockOutput(channel,
XMC_SPI_CH_BRG_SHIFT_CLOCK_PASSIVE_LEVEL_0_DELAY_DISABLED,
XMC_SPI_CH_BRG_SHIFT_CLOCK_OUTPUT_SCLK); //Slave select is active low to
communicate with 6EDL7141
  XMC_SPI_CH_SetSlaveSelectPolarity(channel,
XMC_SPI_CH_SLAVE_SEL_INV_TO_MSLS);

/* Initialize FIFO */
  XMC_USIC_CH_RXFIFO_Configure(channel, 40, XMC_USIC_CH_FIFO_SIZE_8WORDS, 2);
//receive from SPI slave: limit is 1, when FIFO is full with 2 word and a 3nd
is received, the event happens.
  //this is used in main to while until 3 words are received
  XMC_USIC_CH_TXFIFO_Configure(channel, 32, XMC_USIC_CH_FIFO_SIZE_8WORDS, 0);

/* Configure input multiplexer */
  XMC_SPI_CH_SetInputSource(channel, XMC_SPI_CH_INPUT_DIN0,
USIC1_C1_DX0_P0_0); //P0.0 DX0A, 6EDL_SPI_LINK SPI pin assignment

/* Start operation. */
```

```
  XMC_SPI_CH_Start(channel);
  error_SPI = 0;
}
```

Read Command

```
/*The RegAddr is the address of register to read. Data parameter is a pointer
to store the two bytes of data read from the register */
uint16_t Read_Word_16b(uint8_t RegAddr)
{
  XMC_USIC_CH_RXFIFO_Flush(SPI_MAS_CH);
  SPI_MAS_CH->IN[0] = RegAddr & REG_READ;
  SPI_MAS_CH->IN[0] = 0x00;
  SPI_MAS_CH->IN[0] = 0x00;
  uint32_t timeout_counter = 0;
  while ((XMC_USIC_CH_RXFIFO_GetEvent(SPI_MAS_CH) &
XMC_USIC_CH_RXFIFO_EVENT_STANDARD) == 0) /*wait for received data /2 words*/
  {
         if (++timeout_counter > SPI_TIMEOUT)
         {
           error_SPI = 1;
           break;
         }
  };
 XMC_USIC_CH_RXFIFO_ClearEvent(SPI_MAS_CH,XMC_USIC_CH_RXFIFO_EVENT_STANDARD);
  SPI_MAS_CH->OUTR; //data read of invalid data
  uint8_t data_high = SPI_MAS_CH->OUTR; //data read of MSB
  uint8_t data_low = SPI_MAS_CH->OUTR;  //data read of LSB
  return ((data_high << 8) + data_low);
}
```

Write Command

```
/* To write data to register via SPI channel.
   The RegAddr is the address of register to write to.
   Data parameter is a pointer which stored the two bytes of data written to
the register */
void Write_Word_16b(uint8_t RegAddr, uint16_t data)
{
  XMC_USIC_CH_RXFIFO_Flush(SPI_MAS_CH);
  SPI_MAS_CH->IN[0] = RegAddr | REG_WRITE;
  SPI_MAS_CH->IN[0] = (uint8_t)(data >> 8);
  SPI_MAS_CH->IN[0] = (uint8_t)data;
  uint32_t timeout_counter = 0;
```

```
  while ((XMC_USIC_CH_RXFIFO_GetEvent(SPI_MAS_CH) &
XMC_USIC_CH_RXFIFO_EVENT_STANDARD) == 0)  //wait for received data /2 words
  {
        if (++timeout_counter > SPI_TIMEOUT)
        {
          error_SPI = 1;
          break;
        }
  };
 XMC_USIC_CH_RXFIFO_ClearEvent(SPI_MAS_CH,XMC_USIC_CH_RXFIFO_EVENT_STANDARD);
  SPI_MAS_CH->OUTR; //data read to clear buffer
  SPI_MAS_CH->OUTR; //data read to clear buffer
  SPI_MAS_CH->OUTR; //data read to clear buffer
}
```

10 Device Start-up and Functional States

10.1 MOTIX™ 6EDL7141 Power Supply Start-up

6EDL7141power supply section start-up can be divided in two main periods:

- **Power supply start-up**: initiated by CE rise, leads to ramp up of VDDB and DVDD rails.
- **Gate Driver and CSAMP start-up**: begins with EN_DRV rise and results in charge pumps ramp up and current sense amplifiers activation

10.1.1 Power Supply System Start-up

Given a steady battery supply voltage (PVDD), the input pin CE will control the startup of the power supply system. Figure 56 shows graphically the ramp up of buck converter voltage once CE voltage goes above $V_{CE\_TH\_R}$ value. If external filter capacitor is too large, the ramp up time might be exceeding the values provided in Table 11 ($t_{VDDB\_SFT\_START}$). The integrated watchdog can be enabled to monitor and debug the start-up of VDDB, DVDD or charge pumps.

Soft-start for the buck converter is automatically implemented using an integrated DAC for generating the target reference. Once VDDB has reached its UVLO voltage, analog programming starts. This initiates a period of t_{AN_T} duration in which CS_GAIN pin is read internally. The analog programming can be disabled via OTP programming, therefore reducing the start-up time.

After these analog programming period(s) have elapsed, another OTP programmable delay (DVDD_TON_DELAY) is inserted ($t_{DVDD\_TON\_DLY}$) before the DVDD voltage starts ramping up. Longer delays allow the buck converter voltage to stabilize before the DVDD starts charging. If faster start-up time is required, the delay can be shortened taking into consideration the buck output voltage and the external components used (L_{BUCK}, C_{BUCK}). DVDD will ramp up in a configurable time (DVDD_SFTSTART). Tuning of this value can help ensuring proper start-up.

10.1.2 Gate Driver and CSAMP Start-up

Once DVDD is up and stable, XMC1404 firmware starts execution until it decides to enable the gate driver. EN_DRV pin needs to be set above $V_{EN\_DRV\_TH}$ value to enable the driver section. Before this, no PWM signal will transfer to the gate of the MOSFETs. Once EN_DRV is set above $V_{EN\_DRV\_TH}$, both low side and high side charge pumps ramp up to the target value PVCC. This time will depend on the different configurations (capacitors, charge pump frequency, PVCC voltage) as explained in 4.5.

The high side charge pump will start after enough voltage is built in the low side charge pump. After both high side and low side charge pumps UVLOs are reached, the PWM path is activated and the gate driver can output signals to the power MOSFET.

Note: Depending on timing of PWM send to inputs and charge pump capacitor values, the gate driver could start driving the MOSFETs while the charge pumps are not fully at target voltage if the PWM signal is activated early. User can delay the start of PWM signals until charge pumps are fully charged if this is required

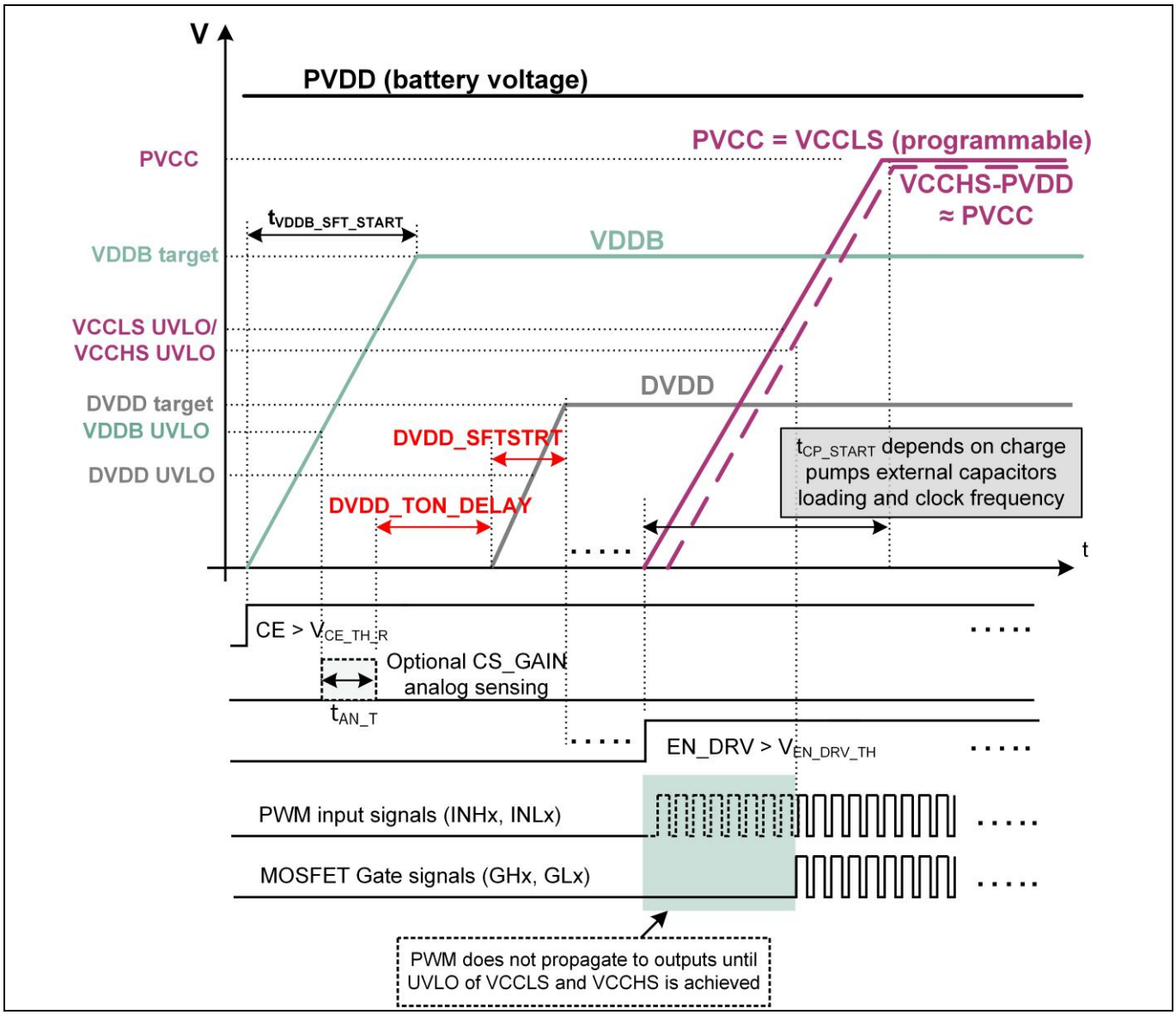

Figure 56 Start-up behavior of supply voltages at steady PVDD supply. EN_DRV and CE_EN functionality. DVDD_SFTSTRT is an SPI programmable parameter

If CE is generated from PVDD, for example via a voltage divider as shown in Figure 62, the start-up behavior will follow the one in Figure 57 or similar. In such case, it is important to notice that the device will not start –i.e. the buck converter will not start switching - until both PVDD UVLO is released and the CE rising voltage thresholds ($V_{CE\_TH\_R}$) are crossed, as can be seen in flowchart in Figure 58. The order of CE and PVDD can swap with similar results.

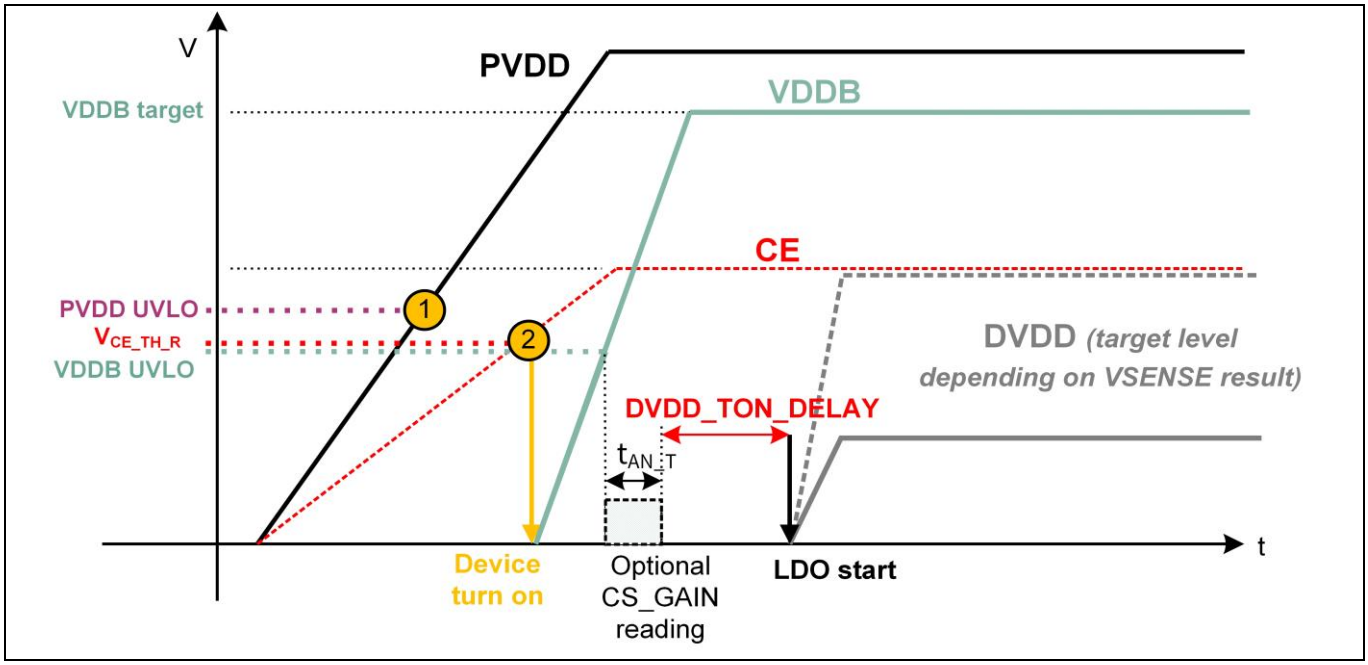

Figure 57 **Start-up behavior detail when PVDD is ramping up and CE is created with a voltage divider from PVDD. Device will only turn on after events 1 and 2 occur, starting up the buck converter controller**

10.2 Device Functional States

The functionality of the device is governed by a state machine. A flowchart of this state machine is shown in Figure 58.

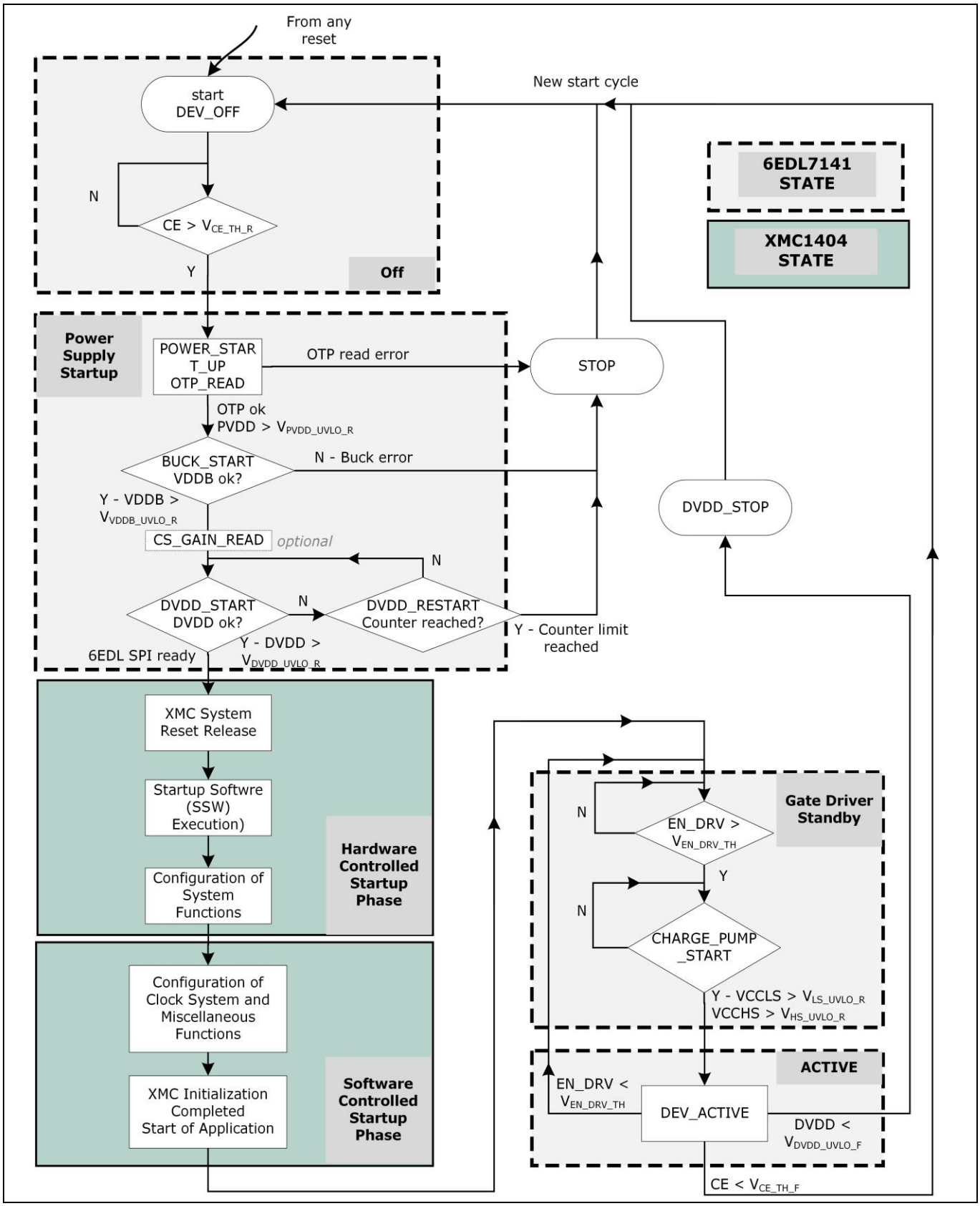

Figure 58 Flowchart diagram for power states of device

Device Start-up and Functional States

Following main states and substates can be considered for IMD70xA:

Off State

- **DEV_OFF** - This state is the default state when in reset.

Power Supply Start-up States

- **POWER_START_UP, OTP_READ** - In this state voltage in PVDD is ramping up and checked by the 6EDL7141. Once ok, the OTP memory in 6EDL7141 is read. This is done before enabling any further blocks to ensure configuration is known. If a fault is signaled by the OTP block then the STOP state will be entered.
- **BUCK_START** - The buck converter is enabled in this state and the VDDB needs to be correct before leaving this state. If the VDDB has not reached the target voltage in a certain time, then the buck will be shut down and the device set in the STOP state.
- **CS_GAIN_READ** - The device will sense pin CS_GAIN (optionally programmable) to program the current sense amplifier gain if analog programming is selected. This is, if CS_GAIN_ANA is set to '0' then the CS gain will be set by the register CS_GAIN. In case of digital programming the state is skipped. In IMD70x gain of current sense amplifiers must be set digitally via SPI commands, which will skip this state in the state machine.
- **DVDD_START** – at this point, once the buck converter output is stable, the linear voltage regulator for DVDD is ramped up according the start-up delay and soft start programming. At the end of this state, DVDD is at target voltage and stable. With this, the start-up procedure of the device finishes and enters a wait state until EN_DRV signal arrives from a XMC1404. This will start the standby section.
- **STOP** - If this state is entered it is because a serious fault with either the buck converter DVDD start-up. The device will not operate until a power cycle or EN_DRV toggle takes place. SPI cannot be used during this state.

XMC1404 Hardware Controlled Start-up:

This state is entered automatically after power up of the microcontroller. This part is generic and it ensures basic configuration of the controller internal circuitry. The hardware setup needs to ensure fulfillment of requirements specified in the Absolute max table in order to enable reliable start-up of the microcontroller before control is handed over to the user software/application. The sequence where boot code gets executed is considered a part of the hardware controlled phase of the startup sequence. For details of the setup requirements, please refer to XMC1400 Reference Manual.

XMC1404 Software Controlled Start-up:

The software controlled startup phase is the part where the application specific configuration gets applied with user software. It involves several steps that are critical for proper operation of the microcontroller in the application context and may also involve some optional configuration actions in order to improve system performance and stability in the application context.

Power-up of the microcontroller gets performed by applying DVDD supply (for details of the supply requirements, please refer to XMC1400 Reference Manual).The connection between pin 3 (DVDD input) and pins 23 and 56 (DVDD output/input) must be done at the PCB level to ensure XMC is properly powered, there is no internal connection internally in IMD70xA.

When XMC supply voltage reaches a stable threshold level, the power-on reset is released.

Next, after the on-chip oscillators in XMC generate a stable clock output, the system reset is released automatically and the Start-up Software (SSW) code starts to run in the controller. The system reset can be triggered from various sources like software controlled CPU reset register or a watchdog time-out-triggered reset.

After reset release, internal XMC clock signals MCLK and PCLK are running at 8MHz and most of the peripherals' clocks are disabled except for CPU, memories and PORT. It is recommended to disable the clock of the unused modules in order to reduce power consumption.

Start-up Software (SSW) execution: after the reset is de-asserted, CPU starts to execute the SSW code from the ROM memory. To indicate the start of the SSW execution, the pull up device in P0.14 is enabled. Pull up device is disabled during reset. SSW reads the Boot Mode Index (BMI) stored in Flash and decide the startup modes elected by the user. The Boot Mode Index is 2 Byte value stored in Flash and holding information about start-up mode and debug configuration of the device. For more details about the various startup modes and handling of BMI, please refer to XMC1400 Reference Manual.

To handle the initial hardfault error during the SSW execution, SSW installs “jump to itself” instruction at SRAM location 2000’000CH as temporary HardFault handler – until the user code installs its own. It is installed upon master reset only. During SSW execution, the SRAM area between 2000’00C0H and 2000’0200H is reserved for usage by XMC1404 SSW, therefore the user software should not store in this area data which must be preserved throughout (non-power) resets.

GATE_DRIVE_STANDBY

- **CHARGE_PUMP_START -** The charge pumps are enabled. If target voltages are reached, the device moves to DEV_ACTIVE.

ACTIVE

- **DEV_ACTIVE (or ACTIVE)**

  In this state the driver is ready to be used. The PWM path is enabled. If EN_DRV signal goes low during active the device turns off both charge pumps and disables the PWM path by going into the STANDBY section.
- **DVDD_STOP** - This state is entered from states after DVDD has been powered and DVDD rail fails. Device stops operation and requires a CE toggle or power cycle to restart. Buck converter and ADC remains active.

11 Register Map

11.1 XMC1404 Registers

For the configuration registers of XMC1404 microcontroller, refer the specific sections fully described in latest XMC1404 reference manual at Infineon website (www.infineon.com). At the time of creation of this document, latest version can be found here: XMC1400 Reference Manual.

11.2 MOTIX™ 6EDL7141 Smart Gate Driver Register Map

Table 27 shows a complete list of 6EDL7141 registers accessible via SPI interface. Registers are explained in detail in this section.

Table 27 Register map overview

Short Name	Long Name	Offset Address	Page Link
FAULT_ST	Fault and warning status	00H	117
TEMP_ST	Temperature status	01H	118
SUPPLY_ST	Power supply status	02H	119
FUNC_ST	Functional status	03H	120
OTP_ST	OTP status	04H	121
ADC_ST	ADC status	05H	122
CP_ST	Charge pumps status	06	122
DEVICE_ID	Device ID	07H	123
FAULTS_CLR	Fault clear	10H	123
SUPPLY_CFG	Power supply configuration	11H	124
ADC_CFG	ADC configuration	12H	126
PWM_CFG	PWM configuration	13H	127
SENSOR_CFG	Sensor configuration	14H	128
WD_CFG	Watchdog configuration	15H	129
WD_CFG2	Watchdog configuration 2	16H	130
IDRIVE_CFG	Gate driver current configuration	17H	131
IDRIVE_PRE_CFG	Pre-charge gate driver current configuration	18H	133
TDRIVE_SRC_CFG	Gate driver sourcing timing configuration	19H	133
TDRIVE_SINK_CFG	Gate driver sinking timing configuration	1AH	134
DT_CFG	Dead time configuration	1BH	136
CP_CFG	Charge pump configuration	1CH	136
CSAMP_CFG	Current sense amplifier configuration	1DH	137
CSAMP_CFG2	Current sense amplifier configuration 2	1EH	139
OTP_PROG	OTP program	1F	141

11.3 MOTIX™ 6EDL7141 Registers Programmability

The programmable registers in 6EDL7141 can be programmed at any time after SPI interface is active, however, some of the bitfield changes will not have an effect until certain conditions occur. This is to protect from wrong behaviors or to avoid glitches in the operation. Three categories are defined:

1. **Always** programmable: programming these bitfields will have an effect immediately after programming in any state of the device. The effect can be synchronized with PWM or braking events for some cases.
2. **Standby** programmable: programming these bitfields will have an effect only when EN_DRV level is low. If programmed when EN_DRV is high, the register will show the new value, but effect will not be applied until EN_DRV is pulled down. This is to avoid system malfunctions. Therefore these registers are recommended to be programmed before EN_DRV is activated.
3. **OTP only**: programming these bitfields will have an effect only if programmed in OTP and after device new power up (PVDD). These are settings affecting the start-up of the device, namely bitfields whose effect takes place even before DVDD ramps up, therefore must be burned into OTP to be effective on next power up.

As an example, if during ACTIVE state a write happens to a ‘Standby’ value, the value will be written and reads to this register will return the written value, however, the value is not (shadow) transferred to actual effective register until the device state machine goes into STANDBY state.

Table 28 provides a categorization for every configuration of the device (‘w’ type bitfield)

Table 28 Register programmability

Register Name	Bitfield Name	Programmability
SUPPLY_CFG	PVCC_SETPT	Standby
	CS_REF_CFG	Standby
	DVDD_OCP_CFG	Always
	DVDD_SFTSTRT	OTP only
	BK_FREQ	Standby
	DVDD_TON_DELAY	OTP only
	CP_PRE_CHARGE_EN	Standby
ADC_CFG	ADC_OD_REQ	Always – no OTP field, just register
	ADC_OD_INSEL	Always – no OTP field, just register
	ADC_EN_FILT	Always – no OTP field, just register
	ADC_FILT_CFG	Always
	ADC_FILT_CFG_PVDD	Always
PWM_CFG	PWM_MODE	Standby
	PWM_FREEW_CFG	Always
	BRAKE_CFG	Always
	PWM_RECIRC	Standby
SENSOR_CFG	HALL_DEGLITCH	Always
	OTS_DIS	Always
	CS_TMODE	Always
WD_CFG	WD_EN	Standby
	WD_INSEL	Standby
	WD_FLTCFG	Standby

Register Map

Register Name	Bitfield Name	Programmability
	WD_TIMER_T	Standby
WD_CFG2	WD_BRAKE	Standby
	WD_EN_LATCH	Standby
	WD_DVDD_RSTRT_ATT	Standby
	WD_DVDD_RSTRT_DLY	Standby
	WD_RLOCK_EN	Always
	WD_RLOCK_T	Always
	WD_BK_DIS	OTP only
IDRIVE_CFG	IHS_SRC	Always
	IHS_SNK	Always
	ILS_SRC	Always
	ILS_SNK	Always
IDRIVE_PRE_CFG	I_PRE_SRC	Always
	I_PRE_SNK	Always
	I_PRE_EN	Always
TDRIVE_SRC_CFG	TDRIVE1	Always
	TDRIVE2	Always
TDRIVE_SINK_CFG	TDRIVE3	Always
	TDRIVE4	Always
DT_CFG	DT_RISE	Always
	DT_FALL	Always
CP_CFG	CP_CLK_ CFG	Always
	CP_CLK_ SS_DIS	Standby
CSAMP_CFG	CS_GAIN	Always – recommended to stop PWM first
	CS_GAIN_ANA	*Standby (change to digital mode)-change to analog mode only possible if written in OTP* – **do not change value, analog programming not possible in IMD70xA**
	CS_EN	Always
	CS_BLANK	Always – recommended to stop PWM first
	CS_EN_DCCAL	Standby
	CS_OCP_DEGLITCH	Standby
	CS_OCPFLT_CFG	Standby
CSAMP_CFG2	CS_OCP_PTHR	Always
	CS_OCP_NTHR	Always
	CS_OCP_LATCH	Standby
	CS_MODE	Standby
	CS_OCP_BRAKE	Standby
	CS_TRUNC_DIS	Always
	VREF_INSEL	Standby

Register Map

Register Name	Bitfield Name	Programmability
	CS_AZ_CFG	Always
	CS_NEG_OCP_DIS	Always
OTP_PROG	OTP_PROG	Standby (programming of OTP only in Standby)
	USER_ID	Always

Table 29 Register read/write coding description

Code	Access type	Description
res	No access	Reserved
r	Read	Read only. A write produces no action
rw	Read/Write	Read or write by user
w	Write	Write only. A read returns 0

11.4 MOTIX™ 6EDL7141 Register Map

Faults Status Register

If the status of one of the bits switches to value b'1, the corresponding fault/warning has occurred. To clear the fault use the clear faults bit in the FAULTS_CLR register

FAULT_ST Address: 00_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			OTP_FLT	WD_FLT	RLOCK_FLT	OTW_FLT	OTS_FLT	BK_OCP_FLT	DVDD_OV_FLT	DVDD_UV_FLT	DVDD_OCP_FLT	CP_FLT	CS_OCP_FLT		
res			r	r	r	r	r	r	r	r	r	r	r		

Field	Bits	Type	Description
CS_OCP_FLT	2:0	r	**Current sense amplifier OCP fault status** OCP (shunt amplifier OCP) fault status bXX0: No fault on phase A bXX1: Fault on phase A bX0X: No Fault on phase B bX1X: Fault on phase B b0XX: No Fault on phase C b1XX: Fault on phase C
CP_ FLT	3	r	**Charge pumps fault status** Charge pump low side and high side combined fault status b0: No fault has occurred b1: A fault has occurred
DVDD_OCP_FLT	4	r	**DVDD OCP (Over-Current Protection) fault status** DVDD linear voltage regulator Over-Current-Protection fault status b0: No fault has occurred b1: A fault has occurred
DVDD_UV_FLT	5	r	**DVDD UVLO (Under-Voltage Lock-Out) fault status** DVDD UVLO fault status b0: No fault has occurred b1: A fault has occurred
DVDD_OV_FLT	6	r	**DVDD OVLO (Over-Voltage Lock-Out)fault status** DVDD OVLO fault status b0: No fault has occurred b1: A fault has occurred
BK_OCP_FLT	7	r	**Buck OCP fault status** Buck Over-Current-Protection fault status b0: No fault has occurred b1: A fault has occurred

OTS_FLT	8	r	**Over-temperature shutdown fault status** Over temperature shutdown event status b0: No fault has occurred b1: A fault has occurred
OTW_FLT	9	r	**Over-temperature warning status** Over temperature warning signal status b0: No warning signal has occurred b1: A warning signal has occurred
RLOCK_FLT	10	r	**Locked rotor fault status** Locked Rotor fault status using hall sensors b0: No fault has occurred b1: A fault has occurred
WD_FLT	11	r	**Watchdog fault status** Watchdog status b0: No fault has occurred b1: A fault has occurred
OTP_FLT	12	r	**OTP status** OTP (One Time Programmable) memory fault status b0: No fault has occurred b1: A fault has occurred
0	15:13	res	**Reserved** A read always returns 0

Temperature Status Register

This register contains the 6EDL7141 die temperature value

TEMP_ST Address: 01_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									**TEMP_VAL**						
res									r						

Field	Bits	Type	Description
TEMP_VAL	6:0	r	**Temperature reading** Temperature value in step of 2 degrees b000000: -94 degrees Celsius ..... every 2 degrees Celsius b1111111: 160 degrees Celsius
0	15:7	res	**Reserved** A read always returns 0

Power Supply Status Register

This registers contains status of power supply related blocks

SUPPLY_ST Address: 02_H

Power Supply Status Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			**PVDD_VAL**							**VDDB_OVST**	**VDDB_UVST**	**DVDD_OVST**	**DVDD_UVST**	**VCCHS_UVST**	**VCCLS_UVST**
res			r							r	r	r	r	r	r

Field	Bits	Type	Description
VCCLS_UVST	0	r	**Charge Pump low side UVLO status** b0: Below threshold b1: Above threshold
VCCHS_UVST	1	r	**Charge Pump high side UVLO status** b0: Below threshold b1: Above threshold
DVDD_UVST	2	r	**DVDD UVLO status** b0: Below threshold b1: Above threshold
DVDD_OVST	3	r	**DVDD OVLO (Over-Voltage Lock-Out) status** b0: Below threshold b1: Above threshold
VDDB_UVST	4	r	**VDDB UVLO status** b0: Below threshold b1: Above threshold
VDDB_OVST	5	r	**VDDB OVLO status** b0: Below threshold b1: Above threshold
PVDD_VAL	12:6	r	**PVDD ADC result reading value** This bitfields holds the analog to digital conversions value for PVDD input voltage
0	15:13	r	**Reserved** A read always returns 0

Functional Status Register

Status of various functional signals.

FUNCT_ST Address: 03_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**CS_GAIN_ST**			**DVDD_ST**	**HALLPOL_ST**	**HALLIN_ST**		
res								r			r	r	r		

Field	Bits	Type	Description
HALLIN_ST	2:0	r	**Hall sensor inputs status -** HALL sensor input pins status for each phase. b0: signal is low b1: signal is high bit 0: Phase A bit 1: Phase B bit 2: Phase C
HALLPOL_ST	3	r	**Hall sensor polarity equal indicator** Status bit that indicate if all phases of the hall sensors have the same polarity at the same time. b0: Hall sensors have different polarity b1: Hall sensors have the same polarity
DVDD_ST	4	r	**DVDD set point status** DVDD set point read value. ***Note: For IMD700A the DVDD rail is forced to be 3.3V and for IMD701A is forced to 5.0V*** b0: 3.3 V – *value for IMD700A* b1: 5.0 V – *value for IMD701A*
CS_GAIN_ST	7:5	r	**Status of the current sense amplifiers gain** Shows the value of the current sense amplifier gain independently of whether programmed digitally or via external resistor b000: 4 V/V b001: 8 V/V b010: 12 V/V b011: 16 V/V b100: 20 V/V b101: 24 V/V b110: 32 V/V b111: 64 V/V
0	15:8	r	**Reserved** A read always returns 0

OTP Status Register

OTP memory status information is found in this register.

OTP_ST Address: 04_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												**OTP_PROG_FAIL**	**OTP_PROG_BLOCK**	**OTP_PASS**	**OTP_USED**
res												r	r	r	r

Field	Bits	Type	Description
OTP_USED	0	r	**OTP used** This bitfield shows if OTP memory has been written by user or still holds factory defaults: b0: OTP memory is not used: factory defaults b1: OTP memory is used: new custom values loaded
OTP_PASS	1	r	**User OTP programming status** Is set if user OTP programming has passed without error. b0: Not programmed or not passed. b1: Programming passed without error.
OTP_PROG_BLOCK	2	r	**User OTP programming blocked** Signals if OTP programming has been attempted when voltage or temperature outside range. b0: Programming was not blocked b1: Programming blocked
OTP_PROG_FAIL	3	r	**OTP Programming fail** If set, indicates that the programming of the OTP has failed. b0: No failure. b1: Programming failed
0	15:4	res	**Reserved** A read always returns 0

ADC Status Register

ADC status registers.

ADC_ST Address: 05_H

Default Name Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**ADC_OD_VAL**							**ADC_OD_RDY**
res								r							r

Field	Bits	Type	Description
ADC_OD_RDY	0	r	**ADC on demand conversion result ready** This bitfields indicates if ADC result for one of the extended conversions is ready to be read b0: Not ready b1: Ready
ADC_OD_VAL	7:1	r	**ADC on demand result value** ADC result value for on demand conversions
0	15:8	res	**Reserved** A read always returns 0

Charge Pumps Status Register

Charge pumps status registers.

CP_ST Address: 06_H

Default Name Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**VCCLS_VAL**							**VCCHS_VAL**						
res		r							r						

Field	Bits	Type	Description
VCCHS_VAL	6:0	r	**VCCHS ADC result reading value** This bitfields holds the analog to digital conversions value for VCCHS voltage
VCCLS_VAL	13:7	r	**VCCLS ADC result reading value** This bitfields holds the analog to digital conversions value for VCCLS voltage
0	15:14	res	**Reserved** A read always returns 0

Device ID Register

Device ID

DEVICE_ID Address: 07_H

Device ID Reset Value 0006_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												**DEV_ID**			
res												r			

Field	Bits	Type	Description
DEV_ID	**3:0**	**r**	**Device ID** Device identifier for user version control
0	15:4	r	**Reserved** A read always returns 0

Faults Clear Register

Clear different faults in the device.

FAULTS_CLR Address: 10_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0														**CLR_ LATCH**	**CLR_ FLTS**
res														w	w

Field	Bits	Type	Description
CLR_FLTS	0	w	**Clear all faults** Setting this bitfield will clear all faults in the device excluding latched faults. A reading always returns 0. b0: No action. b1: Clear all fault status bits except latched ones
CLR_LATCH	1	w	**Clear all latched faults** Setting this bitfield will clear all (and only) latched faults in the device. A reading always returns 0. b0: No action. b1: Clear latched fault status bits
0	15:2	res	**Reserved** A read always returns 0

Power Supply Configuration Register

This register contains bitfields to configure and control power supplies in the device.

SUPPLY_CFG Address: 11_H

Reset Value 6000_H

15	14 13	12	11 10	9 8 7 6	5 4	3 2	1 0
CP_PRECHARGE_EN	**DVDD_TON_DELAY**	**BK_FREQ**	**0**	**DVDD_SFTSTRT**	**DVDD_OCP_CFG**	**CS_REF_CFG**	**PVCC_SETPT**
rw	rw	rw	res	rw	rw	rw	rw

Field	Bits	Type	Description
PVCC_SETPT	1:0	rw	**PVCC set point** Configures the target PVCC (gate driving voltage) voltage level **b00: 12V** b01: 15V b10: 10V b11: 7V
CS_REF_CFG	3:2	rw	**Current sense reference configuration (internal VREF voltage)** Selects the VREF voltage that is applied as offset in all 3 current shunt amplifiers: **b00: ½ DVDD** b01: 5/12 DVDD b10: 1/3 DVDD b11: ¼ DVDD
DVDD_OCP_CFG	5:4	rw	**DVDD OCP threshold configuration** DVDD OCP threshold selection. Pre-waring occurs at 66% of the selected value. **b00: 450mA** b01: 300mA b10: 150mA b11: 50mA
DVDD_SFTSTRT	9:6	rw	**DVDD soft-start configuration** DVDD linear regulator soft start programming 100us stepping 100us up to 1.6ms **b0000: 100 us** b0001: 200 us ..... 100 us steps ..... b1111: 1.6 ms
0	11:10	res	**Reserved** A read always returns 0

BK_FREQ	12	rw	**Buck converter switching frequency selection** This bitfield configures the switching frequency of the buck converter **b0- Low frequency (500kHz)** b1: High frequency (1MHz)
DVDD_TON_DELAY	14:13	rw	**DVDD turn on delay configuration** The device will wait for the configured time before turning on the DVDD starting counting from VDDB UVLO during start-up of the device b00 - 200us b01 - 400us b10 - 600us **b11 - 800us**
CP_PRECHARGE_EN	15	rw	**Charge pump pre-charge configuration** Enables during start-up the pre-charge of the charge pump **1'b0 : pre-charge disabled** 1'b1 : pre-charge enabled

ADC Configuration Register

Note: The complete content of the register must be written at once (read-modify-write). Writing a single bitfield at a time will set to default all other bitfields.

Configuration of ADC related functions.

ADC_CFG Address: 12_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**ADC_FILT_CFG_PVDD**		**ADC_FILT_CFG**		**ADC_EN_FILT**	**ADC_OD_INSEL**		**ADC_OD_REQ**
res								rw		rw		rw	rw		w

Field	Bits	Type	Description
ADC_OD_REQ	0	w	**ADC on demand conversion request** Setting this bitfield will inject an additional measurement in the standard sequence. This additional measurement is selected in ADC_IN_SEL bitfield. A read always return 0. b0: No action. b1: Request the conversion of the signal selected in ADC_IN_SEL
ADC_OD_INSEL	2:1	rw	**ADC input selection for on demand conversions** This bitfield configures the input to the ADC: **b00: $I_{DIGITAL}$: device digital area current consumption** b01: DVDD b10: VDDB b11: Reserved
ADC_EN_FILT	3	w	**Enable filtering for on demand ADC measurement** Enables moving averaging filter for on demand ADC measurements. A read always return 0 b0: No action. b1: Enable filtering
ADC_FILT_CFG	5:4	rw	**ADC generic filtering configuration** Selects the moving averaging filter characteristic for the ADC measurements except PVDD measurements: **b00: 8 samples averaging filter** b01: 16 samples averaging filter b10: 32 samples averaging filter b11: 64 Samples averaging filter

ADC_FILT_CFG_PVDD	7:6	rw	**PVDD ADC measurement result filtering configuration** This bitfield selects the moving averaging filter characteristic for PVDD measurement: **b00: 32 samples** b01: 16 samples b10: 8 samples b11: 1 sample
0	15:8	res	**Reserved** A read always returns 0

PWM Configuration Register

Configuration of PWM related configurations.

PWM_CFG Address: 13_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									**PWM_RECIRC**	**BRAKE_CFG**		**PWM_FREEW_CFG**	**PWM_MODE**		
res									rw	rw		rw	rw		

Field	Bits	Type	Description
PWM_MODE	2:0	rw	**PWM commutation mode selection** PWM Mode selection: **b000: 6PWM mode** b001: 3PWM mode b010: 1PWM mode b011: 1PWM with Hall sensors – **not possible due to interconnects – do not use** b100: b111: Reserved
PWM_FREEW_CFG	3	rw	**PWM freewheeling configuration** This bitfield selects which rectification or freewheeling is desired (only for 1 PWM input modes) **b0: Active freewheeling** b1: Diode freewheeling
BRAKE_CFG	5:4	rw	**Brake configuration** Brake scheme configuration. **b00: Low Side** b01: High Side b10: High Z (no power) b11: Brake toggle-alternates between low and high side braking on every braking event

PWM_RECIRC	6	rw	**PWM recirculation selection (only if PWM_MODE = b011:)** Setting this bitfield will activate the alternating recirculation feature of the 1PWM with Hall Sensors and Alternating Recirculation PWM mode. Only functional if PWM_MODE=b011. **b0: Disable alternating recirculation mode** b1: Enable alternating recirculation mode
0	15:7	res	**Reserved** A read always returns 0

Sensor Configuration Register

Sensors configuration.

SENSOR_CFG Address: 14_H

Reset Value 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									**CS_TMODE**		**OTS_DIS**	**HALL_DEGLITCH**			
res									rw		rw	rw			

Field	Bits	Type	Description
HALL_DEGLITCH	3:0	rw	**Hall Sensor deglitch** Deglitch time configuration for Hall sensor inputs in steps of 640ns b0000: 0ns **b0001: 640 ns** … in steps of 640 ns b1111- 9600 ns
OTS_DIS	4	rw	**Over-temperature shutdown disable** This bitfield allows to disable the shutdown feature due to over temperature in the device: **b0: Enable shutdown protection** b1: Disable shutdown protection
CS_TMODE	6:5	rw	**Current sense amplifier timing mode** This bitfield configures how the current sense amplifier operates regarding the timing related to the PWM signals: **b00: CS amplifier outputs are active when GLx signal is high** b01: CS amplifier outputs are active when GHx signal is low b1x: CS amplifier outputs are always active
0	15:7	res	**Reserved** A read always returns 0

Watchdog Configuration Register

Watchdog controls.

WD_CFG Address: 15_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**WD_TIMER_T**										**WD_FLTCFG**	**WD_INSEL**			**WD_EN**
res	rw										rw	rw			rw

Field	Bits	Type	Description
WD_EN	0	rw	**Watchdog enable** Watchdog timer enable **b0: Watchdog timer is disabled** b1: Watchdog timer is enabled
WD_INSEL	3:1	rw	**Watchdog input selection** This bitfield selects the input to the watchdog timer among following options: ***b000: EN_DRV pin (measure input signal frequency)-Not possible due to interconnects between XMC1404 and 6EDL7141, must be reprogrammed to other value if watchdog is needed.*** b001: Reserved b010: DVDD (linear regulator) b011: VCCLS and VCCHS, (charge pumps) b100: Status register read – candidate for default b101: Reserved b110: Reserved b111: Reserved
WD_FLTCFG	4	rw	**Watchdog fault configuration** This bitfield controls the reaction to a watchdog fault event: **b00: Status register only** b01: Status register and pull down of nFAULT pin
WD_ TIMER_T	14:5	rw	**Watchdog timer period value** This bitfields configures the period of the watchdog timer. After this time is elapsed with no re-start of the timer by the watchdog input, a watchdog fault is triggered. In 100us steps. Not applicable for VDDB (buck) watchdog input. **b0000000000: 100 us** b0000000001: 200 us b1111111111: 102.4ms
0	15	res	**Reserved** A read always returns 0

Watchdog Configuration Register 2

Watchdog configurations register extension.

WD_CFG2 Address: 16_H

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			**WD_BK_DIS**	**WD_RLOCK_T**			**WD_RLOCK_EN**	**WD_DVDD_RSTRT_DLY**				**WD_DVDD_RSTRT_ATT**		**WD_EN_LATCH**	**WD_BRAKE**
res			rw	rw			rw	rw				rw		rw	rw

Field	Bits	Type	Description
WD_BRAKE	0	rw	**Brake on watchdog timer overflow** This bitfields provides the option to configure a braking event when the watchdog overflow occurs **b0: Normal reaction to fault** b1: Brake on watchdog fault (Automatically latched). The braking mode is configured in PWM_CFG register. Status register is updated accordingly
WD_EN_LATCH	1	rw	**Enable latching of watchdog fault** Enable latching of watch dog fault **b0: Fault not latched** b1: Fault latched
WD_DVDD_RSTRT_ATT	3:2	rw	**Restart delay for DVDD** Number of restart attempts for DVDD WD **b00: 0 attempts** b01: 1 attempt b10: 2 attempts b11: 3 attempts
WD_DVDD_RSTRT_DLY	7:4	rw	**DVDD restart delay** Time after WD trigger signal until restart is attempted again for DVDD. In steps of 0.5ms **b0000: 0.5 ms** b0001: 1 ms …… b1110: 7.5 ms b1111: 8 ms
WD_RLOCK_EN	8	rw	**Enable rotor locked detection** Enable rotor lock dedicated watchdog timer input **b0: Disabled** b1: Enabled

WD_RLOCK_T	11:9	rw	**Rotor locked watchdog timeout** Watchdog timer period value (overflow value). In steps of 1s **b000: 1 second** b001: 2 s ……. b111: 8 s
WD_BK_DIS	12	rw	**Buck watchdog disable** Buck watchdog (start-up) disable **b0: Buck watchdog enabled** b1: Buck watchdog disabled
0	15:13	res	**Reserved** A read always returns 0

Gate Driver Current Control Register

Gate driver current settings for slew rate control.

IDRIVE_CFG Address: 17_H

Reset Value BBBBH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ILS_SINK				**ILS_SRC**				**IHS_SINK**				**IHS_SRC**			
res				rw				rw				rw			

Field	Bits	Type	Description

IHS_SRC	3:0	rw	**High-side source current** High side gate driver rise or pull-up gate current applied during period T_{DRIVE2} b0000 - 10mA b0001 - 20mA b0010 - 30mA b0011 - 40mA b0100 - 50mA b0101 - 60mA b0110 - 80mA b0111 – 100mA b1000 - 125mA b1001 - 150mA b1010 - 175mA **b1011 - 200mA** b1100 - 250mA b1101 – 300mA b1110 – 400mA b1111 – 500mA
IHS_SINK	7:4	rw	**High-side sink current** High-side gate driver fall or pull-down gate current applied during period T_{DRIVE4} Same coding as IHS_SRC
ILS_SRC	11:8	**rw**	**Low-side source current** Low side gate driver rise or pull-up gate current applied during period T_{DRIVE2} Same coding as IHS_SRC
ILS_SINK	15:12	**rw**	**Low-side sink current** Low side gate driver fall or pull-down gate current applied during period T_{DRIVE4} Same coding as IHS_SRC

Gate Driver Pre-Charge Current Control Register

Low side gate driver control parameters

IDRIVE_PRE_CFG Address: 18_H

Reset Value $00BB_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**I_PRE_EN**	**I_PRE_SINK**				**I_PRE_SRC**			
res							rw	rw				rw			

Field	Bits	Type	Description
I_PRE_SRC	3:0	rw	**Pre-charge source current setting (T_{DRIVE1})** Rise or pull-up gate current applied during pre-charge phase (T_{DRIVE1}) b0000 - 10mA b0001 - 20mA b0010 - 30mA b0011 - 40mA b0100 - 50mA b0101 - 60mA b0110 - 80mA b0111 - 100mA b1000 - 125mA b1001 - 150mA b1010 - 175mA **b1011 - 200mA** b1100 - 250mA b1101 – 300mA b1110 – 400mA b1111 – 500mA
I_PRE_SINK	7:4	rw	**Pre-charge sink current setting (T_{DRIVE3})** Fall or pull-down current during pre-charge phase (T_{DRIVE3}) Same coding as I_PRE_SRC
I_PRE_EN	8	rw	**Gate driver pre-charge mode enable** Enables extra pre-charge current configurations. In case of disabled, 1.5A are applied during T_{drive1} and T_{drive3} periods **b0: Pre-charge current enabled**. Values I_PRE_SINK and I_PRE_SRC are applied during T_{DRIVE1} and T_{DRIVE3} respectively
0	15:9	res	**Reserved** A read always returns 0

TDRIVE Source Control Register

T_{DRIVE1} and T_{DRIVE2} configuration registers for ate driver sourcing mode.

TDRIVE_SRC_CFG Address: 19_H

Reset Value $FF00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDRIVE2								**TDRIVE1**							
rw								rw							

Field	Bits	Type	Description
TDRIVE1	7:0	rw	**T_{DRIVE1} timing** T_{DRIVE1} value for high and low side. First turn on or pre-charge period **b00000000 - 0ns** b00000001 - 50ns (values between 0ns and 50ns not allowed) 10ns steps b11111111 - 2590ns
TDRIVE2	15:8	rw	**T_{DRIVE2} timing** T_{DRIVE2} value for high and low side. b00000000 - 0ns b00000001 - 10ns 10ns steps **b11111111 - 2550ns**

TDRIVE Sink Control Register

Tdrive3 and Tdrive4 configuration registers for ate driver sourcing mode.

TDRIVE_SINK_CFG Address: $1A_H$

Reset Value $FF00_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDRIVE4								**TDRIVE3**							
rw								rw							

Field	Bits	Type	Description
TDRIVE3	7:0	rw	**T_{DRIVE3} timing** T_{DRIVE3} value for high and low side. First turn off or pre-discharge period **b00000000 - 0ns** b00000001 - 50ns (values between 0ns and 50ns not allowed) 10ns steps b11111111 - 2590ns

TDRIVE4	15:8	rw	**T_{DRIVE4}timing** T_{DRIVE4} value for high and low side. b00000000 - 0ns b00000001 - 10ns 10ns steps **b11111111 - 2550ns**

Dead Time Register

Dead time configurations.

DT_CFG Address: $1B_H$

Reset Value 3131_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DT_FALL								**DT_RISE**							
rw								rw							

Field	Bits	Type	Description
DT_RISE	7:0	rw	**Dead time rise (of phase node voltage)** Dead time rise (low to high) value b00000000: 120 ns b00000001: 200 ns In steps of 80ns … **b00110001: 4040ns** … b10010101: 12040 ns b10010110: b11111111: Unused (defaults to 120ns)
DT_FALL	15:8	rw	**Dead time fall (of phase node voltage)** Dead time fall (high to low) value b00000000: 120 ns b00000001: 200 ns In steps of 80ns … **b00110001: 4040ns** … b10010101: 12040 ns b10010110: b11111111: Unused (defaults to 120ns)

Charge Pump Configuration Register

Charge pump related controls.

CP_CFG Address: $1C_H$

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													**CP_CLK_SS_DIS**	**CP_CLK_CFG**	
res													rw	rw	

Field	Bits	Type	Description
CP_CLK_CFG	1:0	rw	**Charge pump clock frequency configuration** This bitfield configures the charge pump clock switching frequency. **b00: 781.25 kHz** b01: 390.6 kHz b10: 195.3 kHz b11: 1.5625 MHz
CP_CLK_SS_DIS	2	rw	**Charge pump clock spread spectrum disable** **b0: Spread spectrum is enabled** b1: Spread spectrum disabled
0	15:3	res	**Reserved** A read always returns 0

Current Sense Amplifier Configuration Register

Current sense amplifier configurations.

CSAMP_CFG Address: $1D_H$

Reset Value 0028_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS_OCPFLT_CFG		**CS_OCP_DEGLITCH**		**CS_ EN_DCCAL**	**CS_BLANK**				**CS_EN**			**CS_GAIN_ANA**	**CS_GAIN**		
rw		rw		rw	rw				rw			rw	rw		

Field	Bits	Type	Description
CS_GAIN	2:0	rw	**Gain of current sense amplifiers** Selects gain of current sense amplifier when digitally programmed **b000: 4 V/V** b001: 8 V/V b010: 12 V/V b011: 16 V/V b100: 20 V/V b101: 24 V/V b110: 32 V/V b111: 64 V/V
CS_GAIN_ANA	3	rw	**CS Gain analogue programming enable** ***Change to b0 to program GAIN digitally – due to interconnects of XMC1404 and 6EDL7141, analog programming is not possible and CS_GAIN must be programmed digitally*** CS Gain analogue programming enable b0: Gain is selected via register configuration (CS_GAIN bitfield) **b1: Gain is defined by CS_GAIN pin resistor**
CS_EN	6:4	rw	**Enable of each current shunt amplifier** Enable of each current shunt amplifier bit 0: phase A **bit 1: phase B** bit 2: phase C b0: Amplifier disabled **b1: Amplifier enabled**

CS_BLANK	10:7	rw	**Current shunt amplifier blanking time** Current shunt amplifier blanking time **b0000: 0 ns** b0001: 50 ns b0010: 100 ns b0011: 200 ns b0100: 300 ns b0101: 400 ns b0110: 500 ns b0111: 600 ns b1000: 700 ns b1001: 800 ns b1010: 900 ns b1011: 1 us b1100: 2 us b1101: 4 us b1110: 6 us b1111: 8 us
CS_EN_DCCAL	11	rw	**Enable DC Calibration of CS amplifier** DC calibration of CS amplifier **b0: No calibration is executed** b1: DC calibration mode executed: all power stages in high Z: powered but not driving
CS_OCP_DEGLITCH	13:12	rw	**Current sense amplifier OCP deglitch** OCP deglitch timing configuration of the OCP on current sense amplifiers-deglitch disabled (bypassed) if CS_TRUNC_DIS = b0 (register CSAMP_CFG2) **b00: 0 µs** b01: 2 µs b10: 4 µs b11: 8 µs
CS_OCPFLT_CFG	15:14	rw	**Current sense amplifier OCP fault trigger configuration** OCP fault trigger configuration **b00: Count 8 OCP events** b01: Count 16 OCP events b10: Trigger on all OCP events b11: No fault trigger (PWM Truncation continues as defined in bitfield CS_TRUNC_DIS in register CSAMP_CFG2)

Current Sense Amplifier Configuration Register 2

Current sense amplifier configurations extension register.

CSAMP_CFG2 Address: $1E_H$

Reset Value 0833_H

15 14	13	12	11	10	9	8	7 6 5 4	3 2 1 0
CS_AZ_CFG	**CS_NEG_OCP_DIS**	**VREF_INSEL**	**CS_TRUNC_DIS**	**CS_OCP_BRAKE**	**CS_MODE**	**CS_OCP_LATCH**	**CS_OCP_NTHR**	**CS_OCP_PTHR**
rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CS_OCP_PTHR	3:0	rw	**Current sense amplifier OCP positive thresholds** This bitfield configures the threshold level for the positive OCP 4'b0000: 300mV 4'b0001: 250mV 4'b0010: 225mV **4'b0011: 200mV** 4'b0100: 175mV 4'b0101: 150mV 4'b0110: 125mV 4'b0111: 100mV 4'b1000: 90mV 4'b1001: 80mV 4'b1010: 70mV 4'b1011: 60mV 4'b1100: 50mV 4'b1101: 40mV 4'b1110: 30mV 4'b1111: 20mV

CS_OCP_NTHR	7:4	rw	**Current sense amplifier OCP negative thresholds** This bitfield configures the threshold level for the negative OCP **4'b0000: -300mV** 4'b0001: -250mV 4'b0010: -225mV **4'b0011: -200mV** 4'b0100: -175mV 4'b0101: -150mV 4'b0110: -125mV 4'b0111: -100mV 4'b1000: -90mV 4'b1001: -80mV 4'b1010: -70mV 4'b1011: -60mV 4'b1100: -50mV 4'b1101: -40mV 4'b1110: -30mV 4'b1111: -20mV
CS_OCP_LATCH	8	rw	**OCP latch choice** OCP fault can be selected with this bitfield to be a latched: **b0: Unlatched** b1: Latched
CS_MODE	9	rw	**Current sense amplifier sensing mode** Select between shunt resistor and R_{DSON} sensing modes **b0: Shunt resistor** b1: R_{DSON} sensing-CS_TMODE forced to be GL ON only
CS_OCP_BRAKE	10	rw	**Current sense amplifier brake on OCP configuration** Brake on OCP **b0: No braking upon OCP fault.** b1: Brake on OCP fault (fault set to latched). The braking mode is configured in PWM_CFG register
CS_TRUNC_DIS	11	rw	**PWM truncation disable** Disables the truncation of PWM when an OCP occurs. This does not affect fault triggering. b00: PWM truncation enabled **b01: PWM truncation disabled**
VREF_INSEL	12	rw	**VREF source selection – *DO NOT CHANGE – VREF external not possible*** This bitfield controls whether the current sense amplifier buffer offset (reference) is generated internally or is applied externally through the device pin VREF **b0: Use internal – DO NOT CHANGE** b1: Use external – *This configuration is not possible*

CS_NEG_OCP_DIS	13	rw	**Current sense negative OCP disable** This bitfield disables the negative Over Current Protection in the current shunt amplifiers including both the PWM truncation and fault reporting **b0: Negative OCP fault is enabled** b1: Negative OCP fault is disabled
CS_AZ_CFG	15:14	rw	**Current sense Auto-Zero configuration** This bitfield configures the Auto-Zero feature **b00: Auto-Zero enabled with internal synchronization** b01: Auto-Zero disabled b10: Auto-Zero enabled with external synchronization b11: Auto-Zero enabled with external synchronization and charge pump clock gating

OTP Program Register

OTP program command and user ID.

OTP_PROG Address: $1F_H$

Reset Value 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											**USER_ID**				**OTP_PROG**
res											rw				w

Field	Bits	Type	Description
OTP_PROG	0	w	**Program OTP** Setting this bitfield will start programming of OTP
USER_ID	4:1	rw	**User ID** Space for user to enter an ID into OTP for version control
0	15:5	res	**Reserved** A read always returns 0

12 Application Description

12.1 Recommended External Components

MOTIX™ IMD70xA requires some external components for proper operation. Recommended components and values are listed in Table 30.

Table 30 Recommended external components

Element	Pin1	Pin2	Recommended value	Rating	Notes
C_{PVDD}	PVDD	PGND	4.7µF	According to PVDD	
C_{DVDD}	DVDD	DGND	10µF + 0.1µF	16V	
C_{VCCHS}	VCCHS	PVDD or PGND	1µF < C_{VCCHS} < 2.2µF	25V if connected to PVDD or according to (PVDD+PVCC) if connected to PGND	Depending on VCCHS ripple and start-up requirements. Connection possible to PGND and PVDD
C_{VCCLS}	VCCLS	PGND	1µF < C_{VCCLS} < 4.7µF	25V	Depending on VCCLS ripple and start-up requirements
C_{CP1}	CP1H	CP1L	220nF< C_{CP1} <1µF	16V or 25V	0.47µF recommended
C_{CP2}	CP2H	CP2L	220nF< C_{CP2} <1µF	According to PVDD	0.47µF recommended
L_{BUCK}	PH	VDDB	22µH	According to max peak current	500kHz configuration
			10µH		1MHz configuration
C_{BUCK}	VDDB	PGND	47 µF	16V	500kHz configuration
			47 µF		1MHz configuration

12.2 PCB Layout Recommendations

Layout is critical to ensure high quality signal and sensing. Different recommendations are provided in this section for best electrical, thermal and EMI results.

Grounding and Supply

PGND is the ground used for the following sections in 6EDL7141:

- Buck converter
- Charge pumps
- Gate drivers for low and high side

DGND is used for:

- XMC1404,
- Digital logic in 6EDL7141,
- Current sense amplifiers
- DVDD

It is recommended to cover well components that refer to PGND with PGND solid planes and to cover DGND referred components with DGND solid plane. Also ensure that there is no overlap between PGND and DGND planes to avoid cross coupling.

Application Description

However, PGND and DGND have be connected to the same electrical potential and must be connected to each other in one place in the PCB. The location depends on many factors. Sometimes close to the negative (return) of the supply or battery can lead to best results.

Decoupling capacitors for supply pin (PVDD) should be as close as possible to the pin 25 (PVDD) and pin 27 (PGND). It can as well be helpful to use a small 0.1uF capacitor for high frequency glitches suppression.

Generally speaking shielding of signals like gate signals but also sensing signals is important to avoid coupling and noise injection from other noisy areas.

If battery is expected suddenly drop close to the UVLO level of PVDD, it is recommended to have large capacitors that can maintain the supply voltage during those transients. Eventually, a diode (e.g. Schottky) can be used in series with PVDD and before the decoupling capacitor. This can avoid that the PVDD decoupling capacitors discharge to the battery or other circuits when the battery transient crosses below the PVDD UVLO level of 6EDL7141.

Similarly, CE pin if derived from the battery voltage with voltage dividers, might be affected by these transients. It can be a good idea to use a small capacitor in CE pin to ensure noise is not switching off the device. Current consumption of CE pin is extremely low. If the only way to discharge the CE capacitor is through 6EDL7141, the device might stay on for long periods. It could be useful to design a discharge path in case this is a problem.

Thermal design

Depending on the configuration of the device and the usage of the different integrated power converters like synchronous buck, LDO or charge pump, the device will present different power losses that will translate into self-heating. User can choose for example the LDO output voltage: selecting 5V instead of 3.3V will reduce the losses in the LDO module. Another example: the buck converter output voltage (which is the input for the LDO), can be configured according to the gate driving voltage needs. If 12V/15V are not required, user can configure the buck converter to produce 7V output voltage, reducing the losses as well in the LDO when compared with the standard case 8V.

In order to dissipate the generated heat to the PCB is critical to have a solid connection of the device to the thermal pad (DGND pad). It is as well highly recommended to have a good amount of thermal vias that can transfer efficiently the heat from the pad to the PCB. An example is presented in Figure 59.

As a general rule, thicker PCB layers (2 oz/ft^2-70µm- or above) can help dissipate faster any heat generated inside the device.

Buck Converter and DVDD

The relatively high switching frequency and high voltage switching (PVDD to PGND) of the buck converter makes it a sensitive block in the device to pay extra attention during design phase.

Main goal is to reduce buck switching loop as much as possible (V_{PH}-Inductor-Capacitor-VDDB). In 6EDL7141, most elements in the synchronous buck are integrated mitigating the EMI emissions, like external diode or low side MOSFET as well as the feedback or reference resistors.

Apart from the loop itself, it is very important to reduce in particular the V_{PH} traces to the shortest possible and avoid any large copper amount in the inductor connection. This node is switching PVDD voltage at high frequency and therefore can be a source of noise in other elements especially this trace must be as far as possible from sensitive analog sensing like current sensing.

Figure 59 shows a possible buck converter layout with minimized V_{PH} trace and buck loop area.

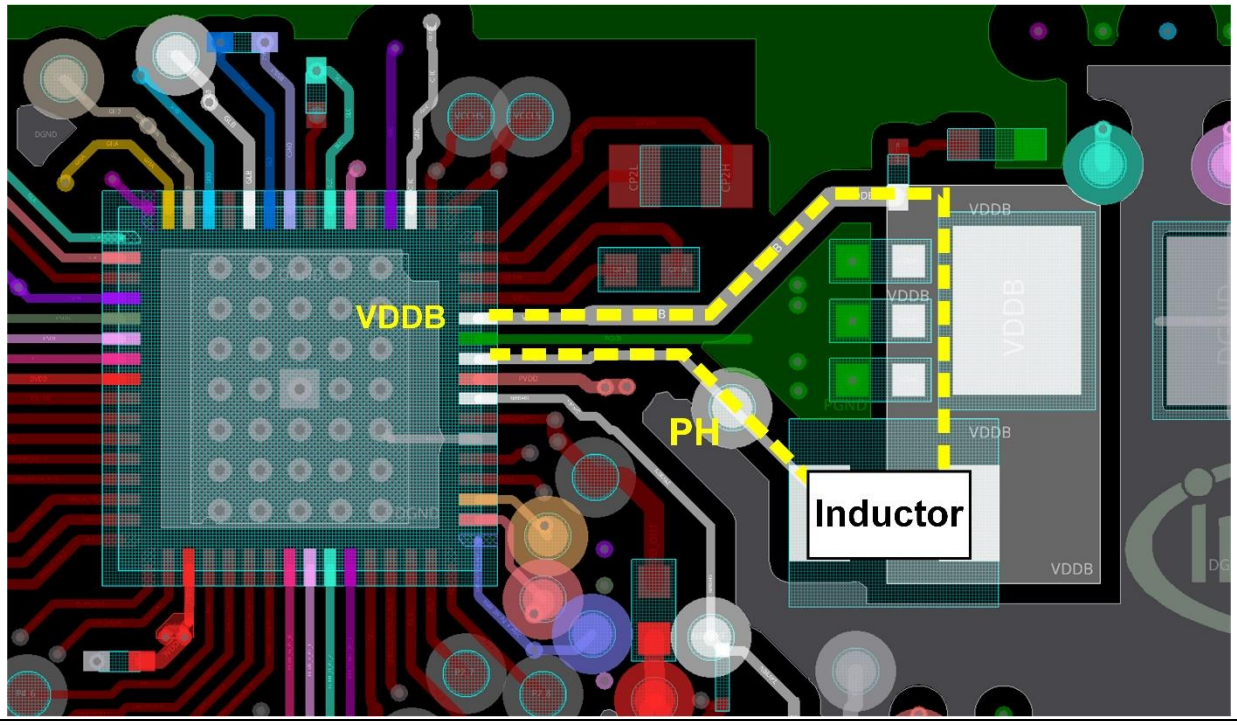

Figure 59 Buck converter layout recommendation. V_{PH} trace and buck loop area (highlighted) must be minimized

DVDD linear regulator must be decoupled with capacitors placed as close as possible to the DVDD pins and connect as short as possible to DGND on the other terminal. Other components supplied by DVDD voltage are recommended to use additional decoupling local capacitors at those components. This is helpful to suppress possible noise captured by the routing of those traces.

Gate Driver and Charge Pumps

Maintain as symmetric as possible gate signals including symmetry between phases (similar length for phase A, B and C) to avoid propagation delay mismatches. Keep as well gate current loops as short as possible and try to have as close as possible send and return signals.

The source signals of low side SLx, are shared between source of low side MOSFETs and top side sensing for shunt elements. It is recommended to optimize for the current sensing (symmetric tap of shunt terminal and parallel routing till current sense inputs), however, if current sense is not used, optimizing for gate driver performance is a good option.

Charge pump loops should be as small as possible, the charge pump flying capacitors must be placed close to the pins 29, 30, 31 and 32. Similar for the tank capacitors in VCCHS (pin 34) and VCCLS (pin 33). It is possible to place some of these capacitors in different layers as long as distance to the device is shortest possible.

Figure 60 shows and example of 6EDL7141 layout highlighting gate driver signals for high side and low side of phase A and the current sensing in a dual MOSFETs inverter.

Gate resistor can be used, however, user must know that the slew rate control of 6EDL7141 provides means to tune how fast MOSFETs switch in a programmable manner. Having Rg resistors will add additional voltage drop between 6EDL7141 and the gate of the MOSFET. Similarly, snubber elements (in parallel with MOSFETs) and bypass capacitors (high side drain to low side source) in the inverter can be used, nevertheless, the flexibility of the slew rate controller allows to remove those minimizing the BOM specially in a busy area of the layout, so more space can be used for the power section for example for better heat distribution in the PCB.

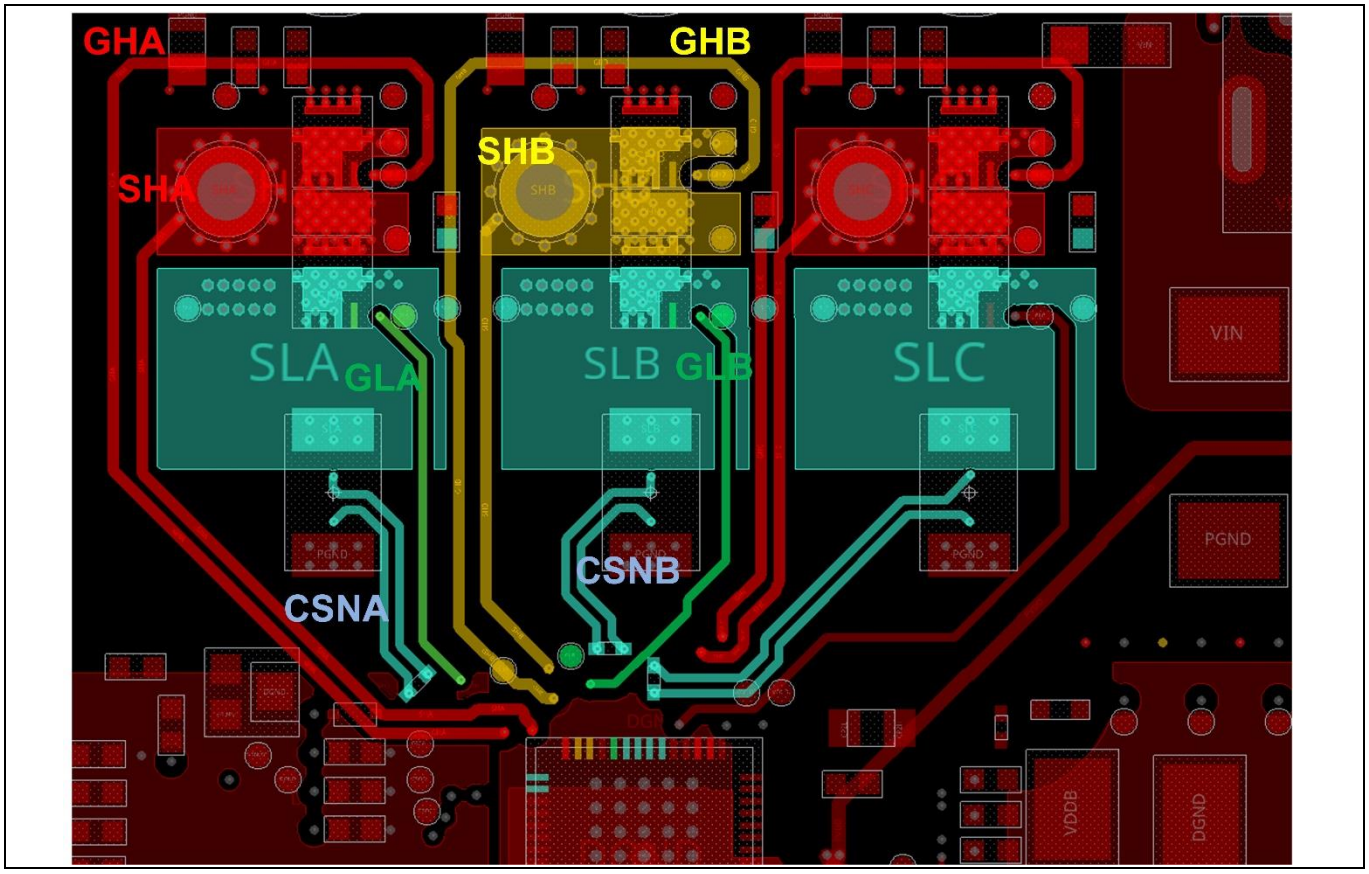

Figure 60 Gate driver and current sensing layout example. Signals are routed in a middle layer.

Current Sensing:

RC filter at SLx and CSNx must be done with care and is not preferred. R1 and R2 as shown in Figure 61, present voltage drop due to amplifier bias current and/or gate driver current, which affect the R_{shunt} current sensing accuracy.

R1 limits the current of low-side (LS) gate driver and acts in fact as Rg. A parallel capacitor (C1 as shown below) between SLx and CSNx can be used. This can increase switching noise during MOSFET switching, at the same time improve steady state value. Larger C values will accentuate this effect. Depending on application this value can be adjusted. The parallel capacitor should be close to the SLx and CSNx inputs pins on PCB and values between 100pF to 1nF can be a good starting point.

It is strongly recommended to use RC filter between current sense amplifier outputs (CSOx) and the ADC inputs in XMC1404 (AINx pins). Typical cut off frequency of 1MHz can be a good compromise between filtering capability and dynamic behavior, but user must decide depending on overall performance target.

Kelvin connection of shunt resistor is highly recommended as shown in Figure 60. Traces of SLx (red) and CSNx (blue) are routed in a middle layer in this case and covered with solid ground planes.

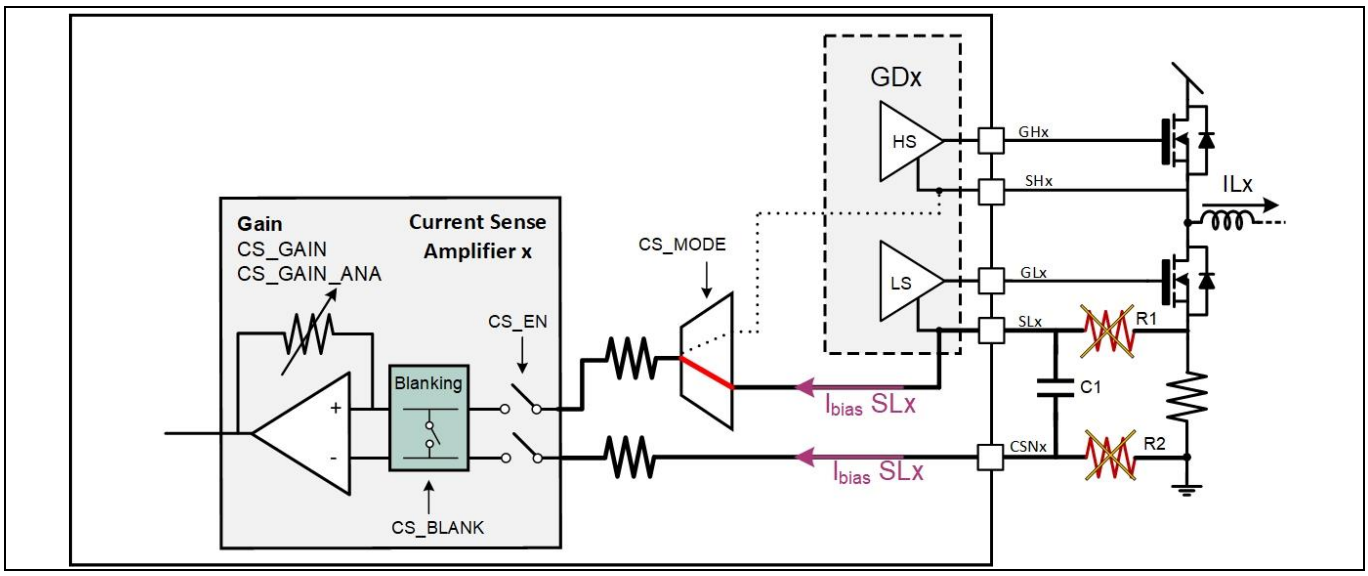

Figure 61 Current sense amplifier input filtering

12.3 Typical Applications

MOTIX™ IMD70xA is a controller with integrated 3-phase gate driver IC to be used with external power MOSFETs for BLDC motor control applications. IMD70xA integrates as well a synchronous buck converter and a linear voltage regulator to provide power for charge pumps (gate drivers), XMC1404 and other external sensors. It integrates as well 3 current sense amplifiers with programmable gain. This can be used for single, double or triple shunt applications. This current information is used by XMC1404 to control the motor and to enhance the system protection.

Hall sensors can directly be connected to IMD70xA (through XMC1404 POSIF interface) inputs. An example configuration of this solution is presented in Figure 62. In this case, IMD70xA uses a single current sense amplifier.

Alternatively, Figure 63 shows a typical schematic for sensorless motor control method for BLDC motors. All 3 integrated current sense amplifiers are used to amplify the current flowing through current shunts. Current sense amplifier outputs are connected to the microcontroller ADC inputs so XMC1404 can control either torque, speed or position of the motor.

These 2 examples show only a basic set up. GPIOs and ADC inputs can be used for purpose like communication with other systems (e.g. SPI, UART, I2C), measurement of other magnitudes in the drive or for general purpose I/O like buttons or reading of a potentiometer.

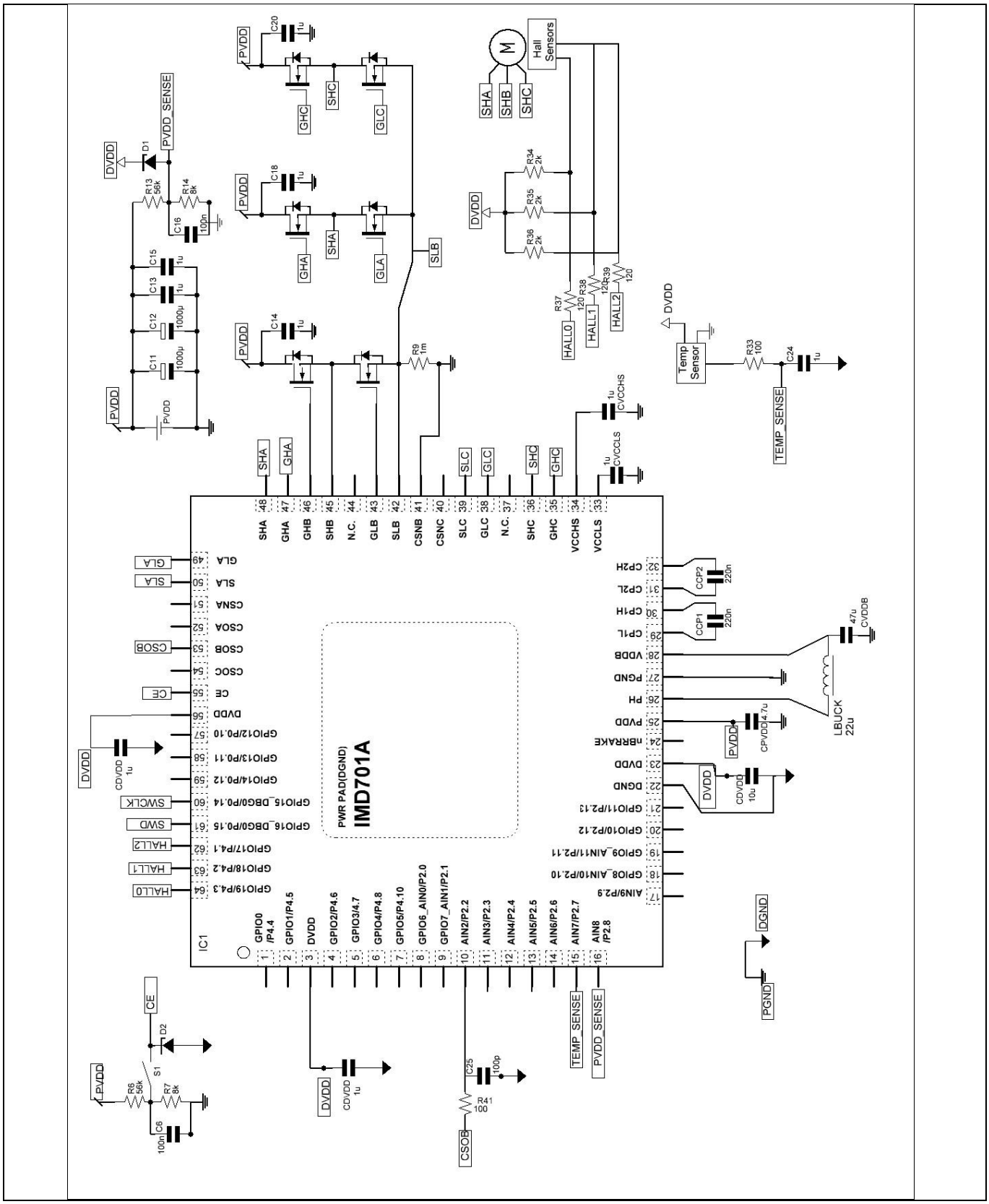

Figure 62 **Example IMD701A schematic for trapezoidal or trapezoidal commutation control of BLDC motors using a single shunt configuration and 3 Hall sensors. Only minimum set up shown. GPIOs and ADC inputs can be used for auxiliary and general purpose (communication, LEDs, buttons, etc.). Voltage dividers and capacitors voltage rating must be calculated for the specific target PVDD voltage**

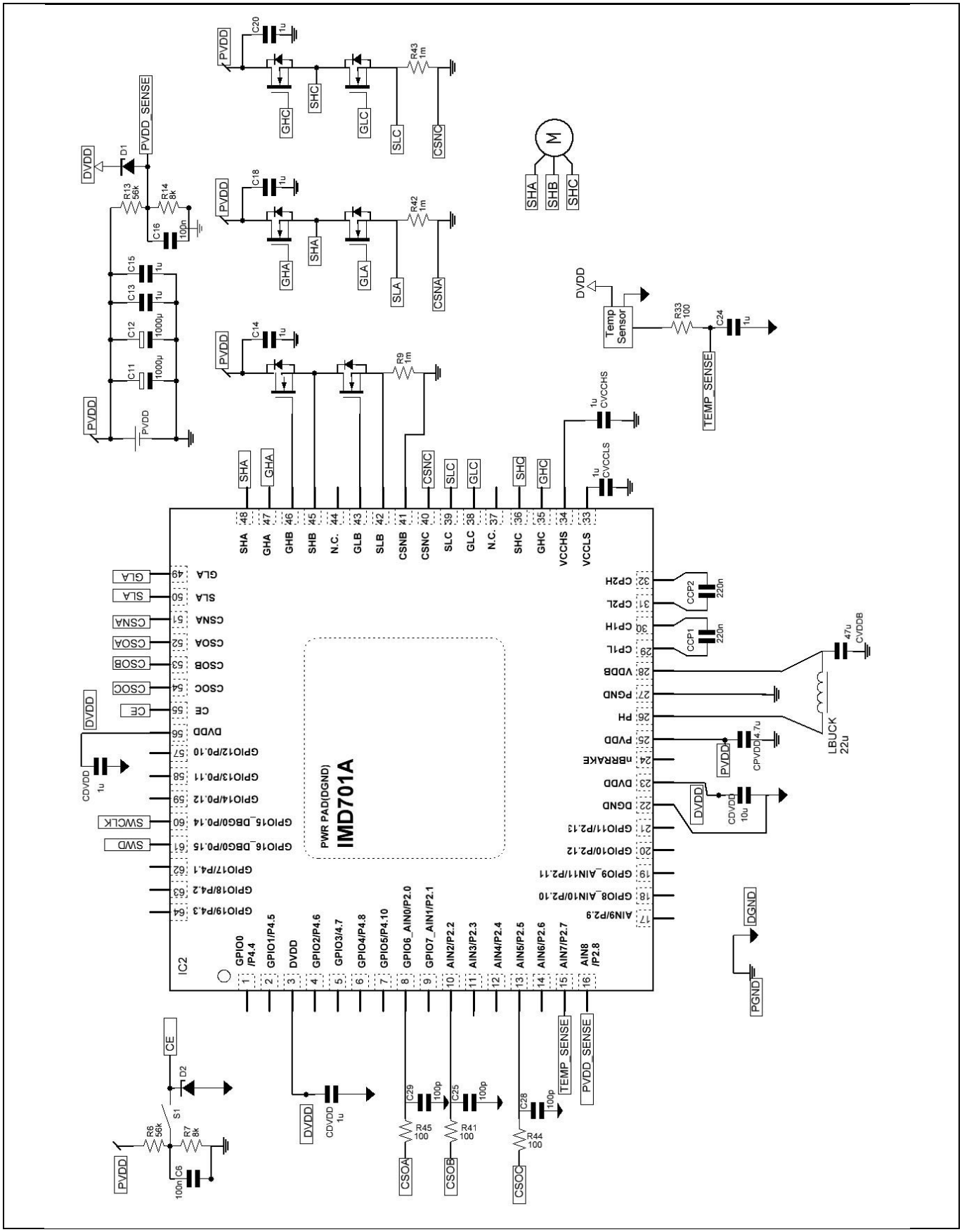

Figure 63 **Example IMD701A schematic for sensorless control of BLDC motors using 3 shunts for current measurement. Voltage dividers and capacitors voltage rating must be calculated for the specific target PVDD voltage**

13 ESD Protection

Following diagrams show ESD protections and pin internal diagrams for different pins of the device.

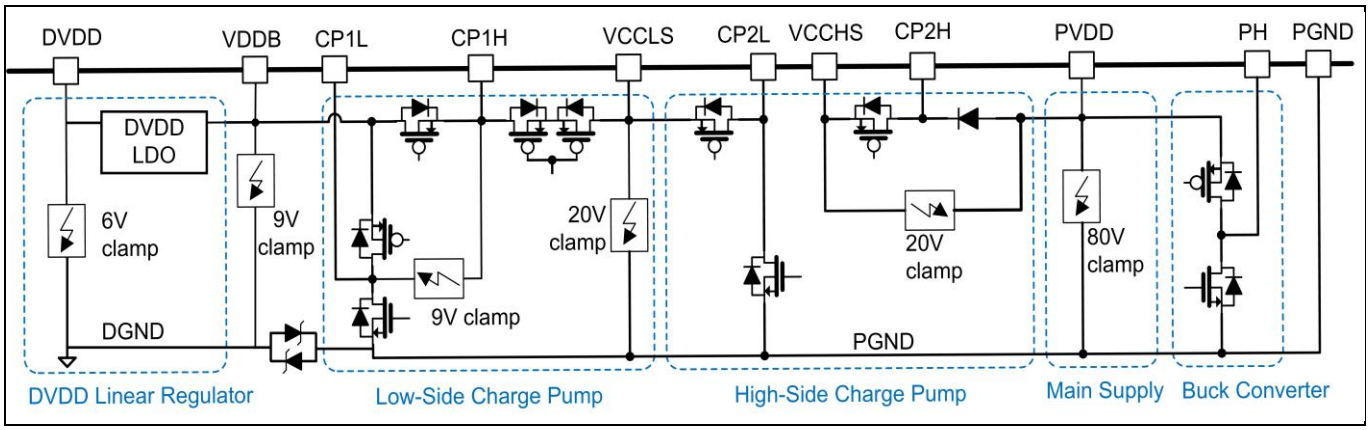

Figure 64 ESD protection diagram for power supply related pins

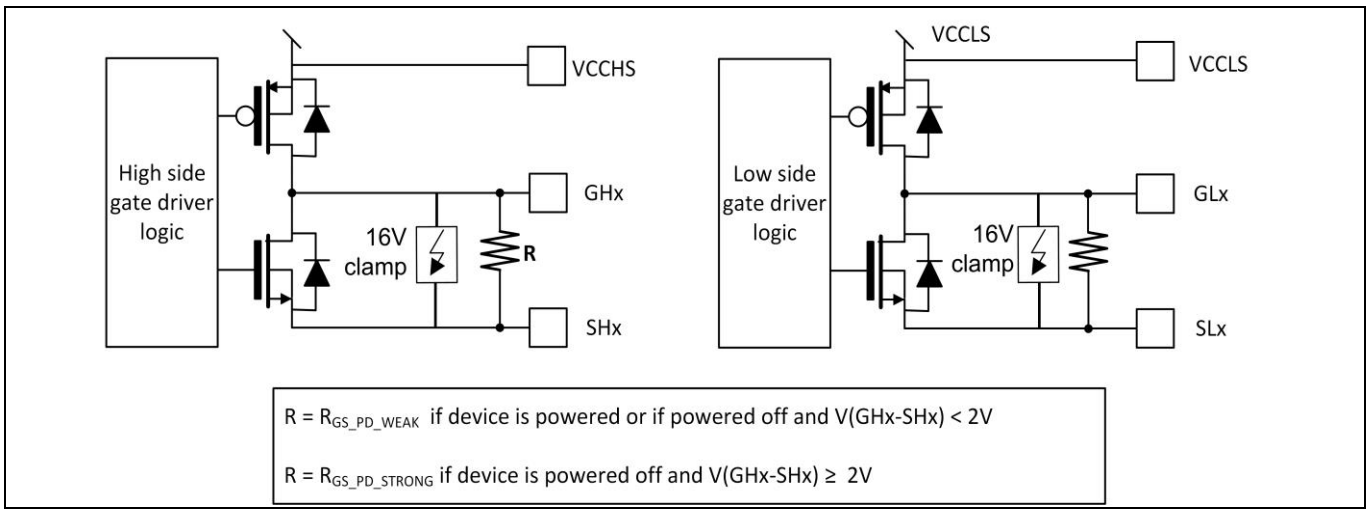

Figure 65 Pin diagram for gate driver output pins

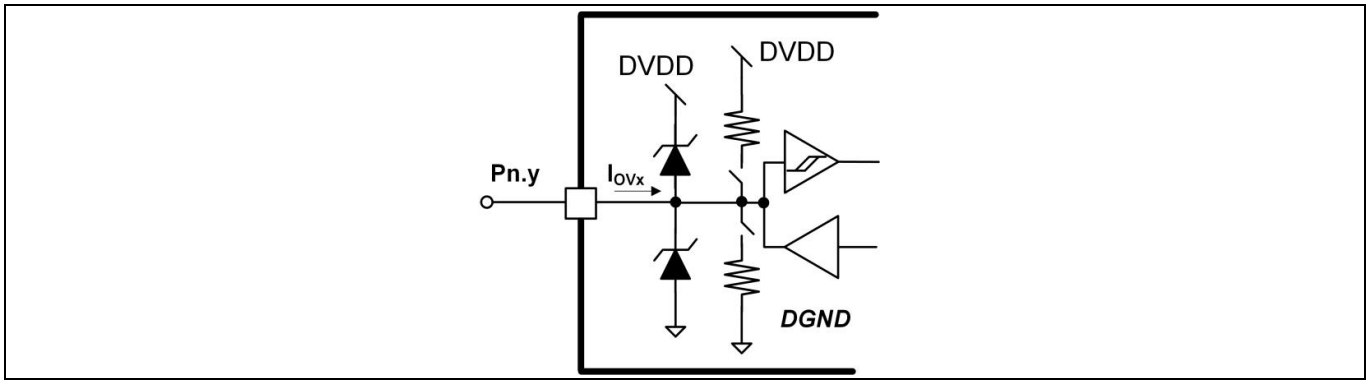

Figure 66 ESD protection and pin diagram for XMC pins

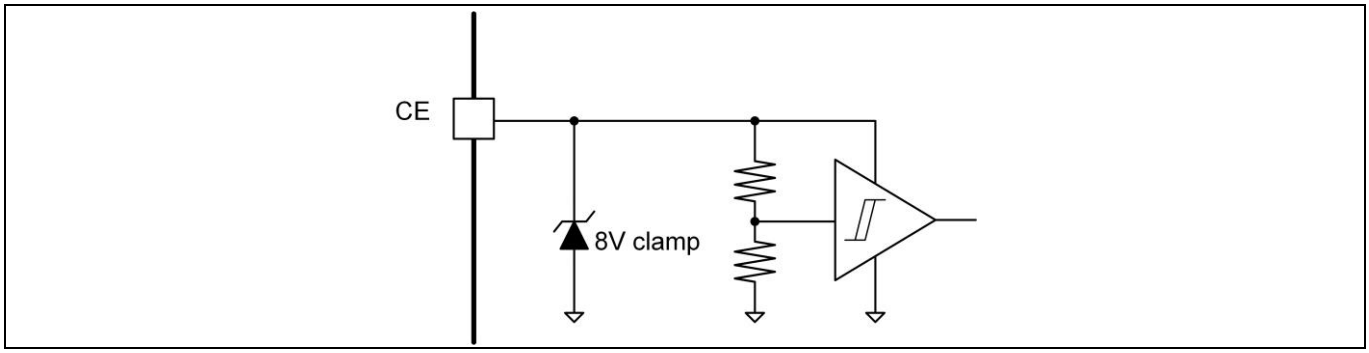

Figure 67 ESD protection and pin diagram for CE pin

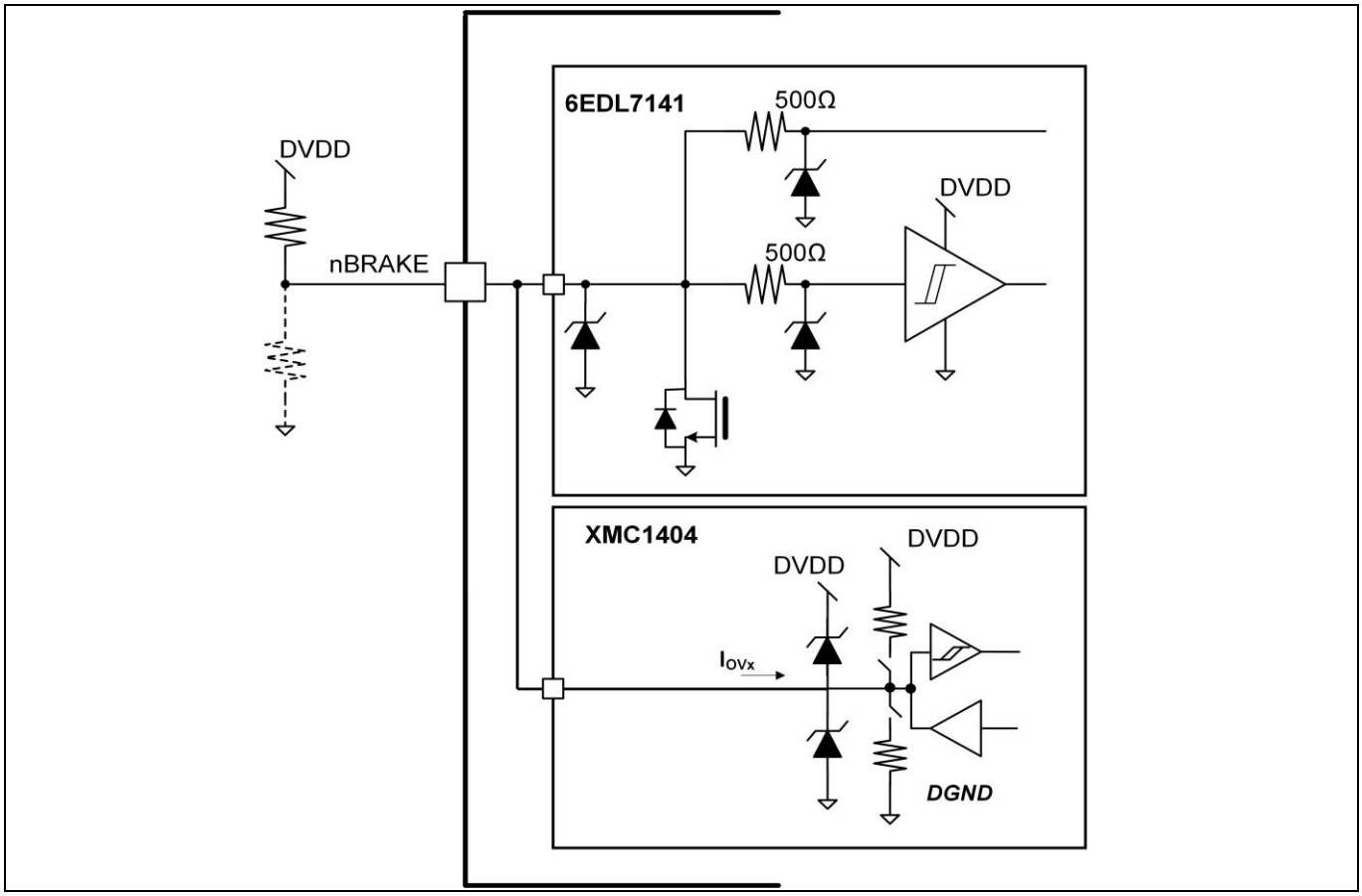

Figure 68 ESD protection and pin diagram for nBRAKE pin

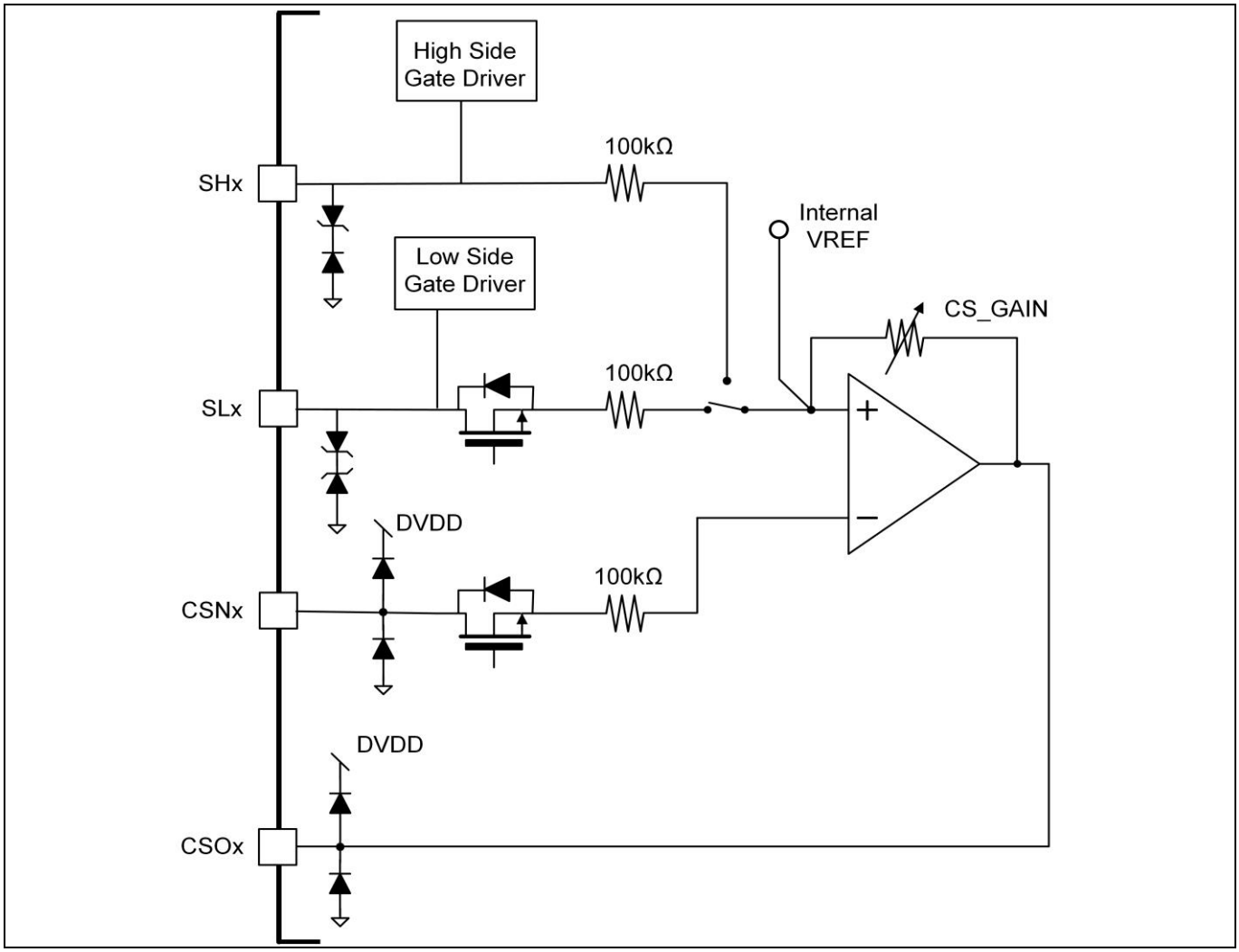

Figure 69 ESD protection and pin diagram for current sense amplifier related pins

14 Package Information

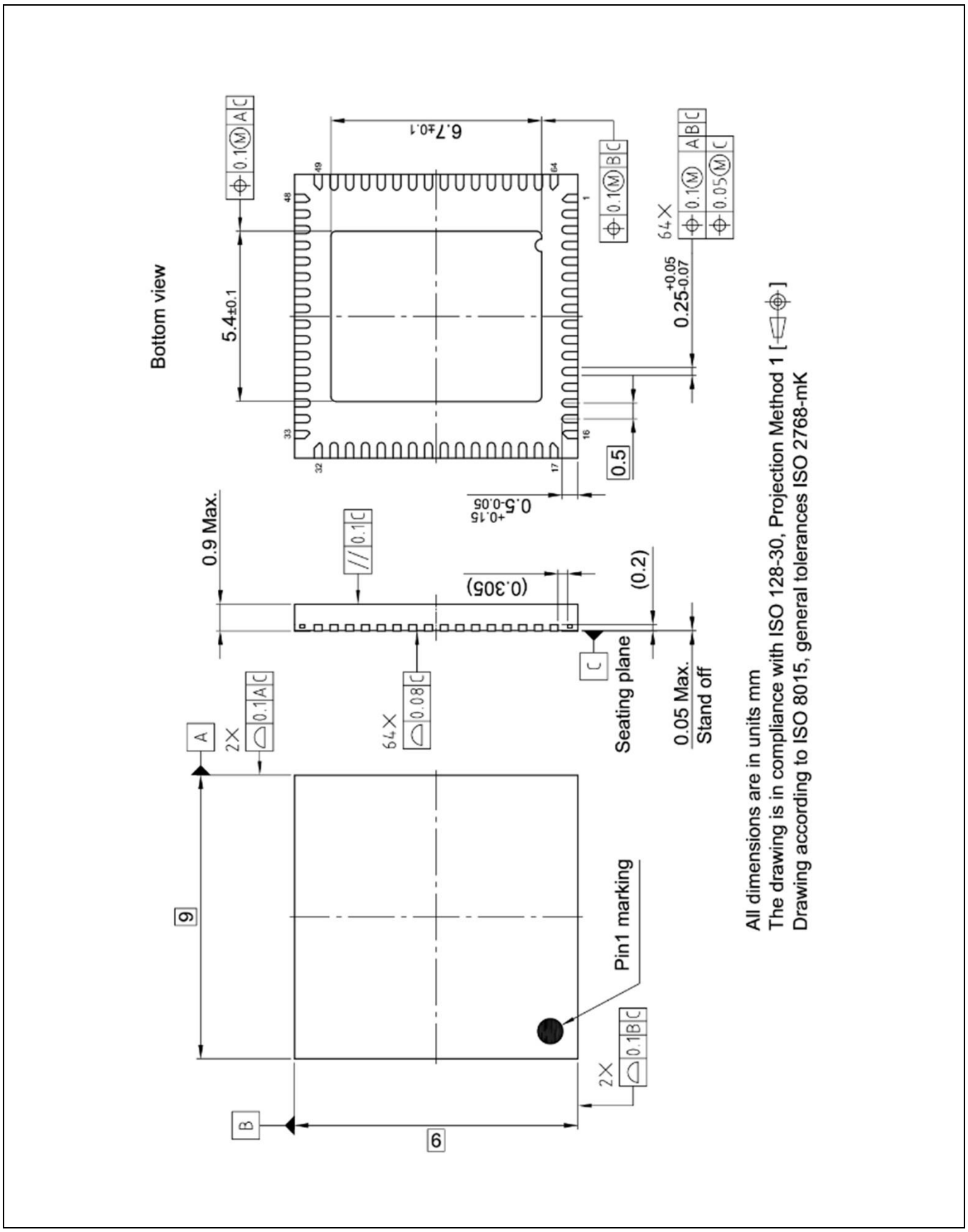

Figure 70 PG-VQFN-64-8 package outline

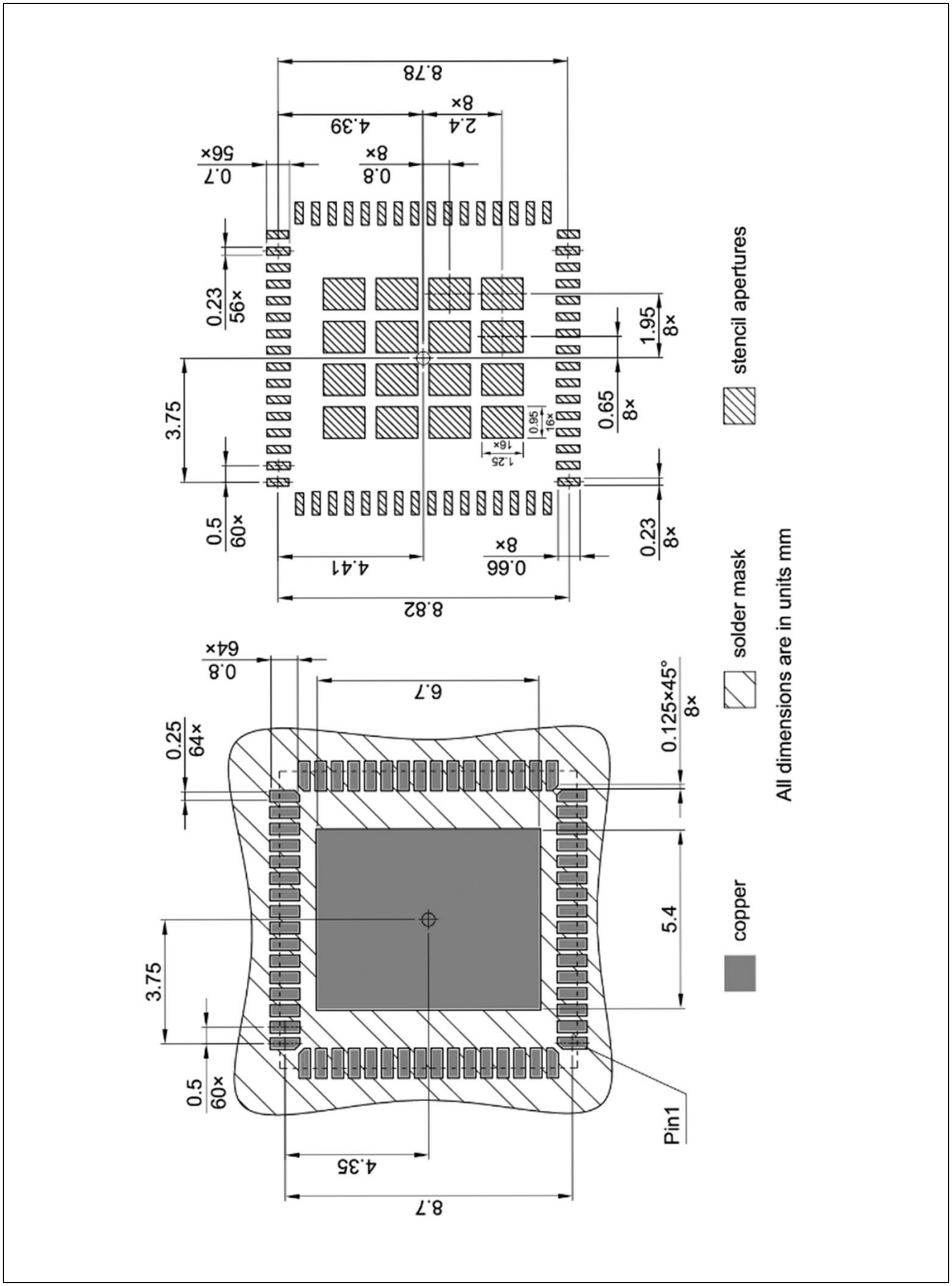

Figure 71 PG-VQFN-64-8 PCB footprint dimensions

Revision history

Version	Description of change
V1.00	First public version
V1.02	Datasheet update • Several editorial changes and typos • Clarification on CE pin voltage thresholds in Electrical Characteristics table • Added 'Thermal design' section in PCB layout recommendations • Changed SPI min clock period to 77ns in Table 11 • Changed DVDD OCP limit accuracy ($I_{DVDD\_I\_ACC}$) and added different specification for different OCP limit settings. • Removed pull down comment on nSCS pin in Table 2. • Typo in Table 2, SDI and SDO XMC reference to input/output functions were swapped

V1.20	Datasheet update
	• Correction of pin description of pins 49 and 50 in Table 1
	• Added PVDD as possible connection for VCCHS negative terminal in Table 30
	• Absolute Maximum Ratings table updated for following parameters: VCCLS, VCCHS, VCCHS-V_{SHx}, VCCHS-V_{GHx}, V_{CP1H}, V_{CP2L}, $V_{CP2H.}$
	• Changes in Electrical Characteristics table:
	  • $I_{GD\_ACCURACY}$ and f_{BUCK_SW} parameters condition modified
	  • t_{PROP_HS}, t_{PROP_LS} and $V_{CS\_REF\_ACC}$ min and max values modified and added condition
	  • $VDDB_{NOM\_LV}$, $V_{VDDB\_OVLO\_F}$, $\varepsilon_{ADC\_GAIN\_ERR}$, $I_{DVDD\_I\_ACC}$ and V_{CS_OS} specifications modified
	  • Following parameters are removed due to redundancy: f_{ADC_CLK}, V_{OD_LV}
	  • Following parameters have a newly added 1) note: f_{PWM_GD}, f_{BUCK_SW}, $t_{VDDB\_SFT\_START}$, t_{AN_T}, $t_{DVDD\_TON\_DLY}$, $t_{DVDD\_SFT\_START}$, t_{CS_BLANK}, $V_{CS\_REF\_ACC}$, t_{AUTO_ZERO}, $t_{AUTO\_ZERO\_CYCLE}$, $t_{CS\_OCP\_DEGLITCH}$, t_{OCP_BLANK}, $PVDD_{OTP\_PROG}$, T_{OTP_PROG}, $t_{WD\_EN\_DRV\_FREQ}$, t_{LOCK}
	• Correction in Table 12. Typo (extra row removed), and added extra condition to differentiate 3.3V and 5V options. Added also new paramenter rotor locked detection time configurability
	• Removed undefined parameters IMVDD and IMVSS parameters in Table 12
	• Other editorial changes like links not working or figure number missing
	• Typo corrections. E.g. FAULT_CLR should be FAULTS_CLR in register map section.
	• ADC_FILT_CFG_P mentioned twice, must be PVDD not P- Figure also changed in ADC section
	• Typo on active freewheeling coding in 1 -PWM 1 mode description
	• OTP programming section 9 typo: PVDD < $PVDD_{OTP\_PROG}$ was wrongly '>'
	• Duplicated spec VCCHS-V_{GHx} in Table 4.

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