Quad Universal Asynchronous Receiver/Transmitter (UART) with FIFO's

Description

The IMP16C554 is a universal asynchronous receiver and transmitter with 16 byte transmit and receive FIFO. A programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 1.5MHz.

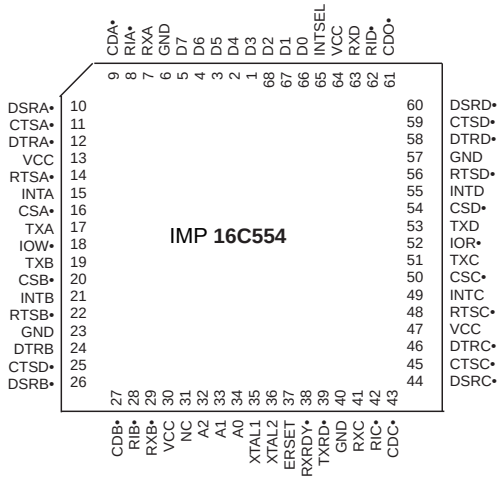
The IMP16C554 is an improved version of the IMP16C550 UART with higher operating speed and lower access time. The IMP16C554 on board status registers provides the error conditions, type and status of the transfer operation being performed. Included is complete MODEM control capability, and a processor interrupt system that may be software tailored to the user's requirements. The IMP16C554 provides internal loop-back capability for on board diagnostic testing.

The IMP16C554 is fabricated in an advanced 1.2u CMOS process to achieve low drain power and high speed requirements.

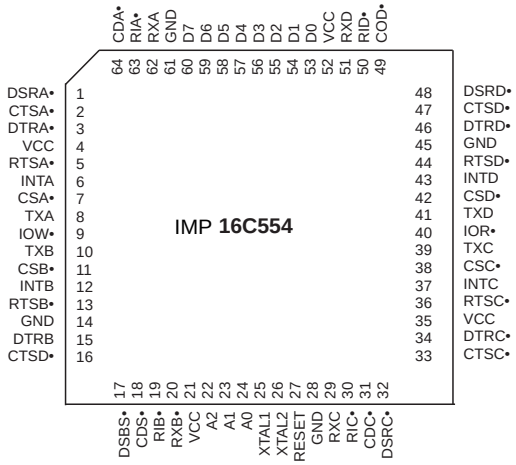
Key Features

- 16 byte receive FIFO with error flags
- Modem control signal (CTS*, RTS*, DSR*, DTR*, RI* ,CD*)
- Programmable character lengths(5,6,7,8)
- Even, odd, or no parity bit generation and detection
- Status report register
- Independent transmit and receive control
- TLL compatible inputs. outputs
- Software compatible with Ei8250, 1Ei16C550
- 460.8kHz transmit/receive operation with 7.372 MHz crystal or external clock source

Pin Configuration



68-PIN PLCC



64-PIN QFP

408-432-9100/www.impweb.com

SYMBOL DESCRIPTION

symbol	pin	Signal Type	Pin Description
D0-D7	5-66	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. Do is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A-B RX C-D	7.29 41.63	I	Serial data input. The serial information (data) received from serial port to IMP16C554 receive input circuit . A mark (high) is logic one and a space (low)is logic zero. During the local loopback mode the RX input is disabled from external connection and to the TX output internally.
TX A-B TX C-D	17.19 51.53	O	Serial data output. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark(high) state during reset, local loopback mode or when the transmitter is disabled.
CS*A-B CS*C-D	16.20 50.54	I	Chip select. (active low) A low at this pin enables the IMP16C554/CPU data transfer operation. Each UART sections of the IMP16C554 can be accessed independently.
XTAL1	35	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	36	O	Crystal input 2 or buffered clock output. See XTAL1.
LOW*	18	I	Write strobe.(active low)A low on this pin will transfer the contents of the CPU data bus to the addressed register.
GND GND	6.23 40.57	O	Signal and power ground.
IOR*	52	I	Read strobe.(active low)A low level on this pin transfers the contents of the IMP16C554 data bus to the CPU.

SYMBOL DESCRIPTION

symbol	pin	Signal Type	Pin Description
TXRDY*	39	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the IMP16C554 is full. It can be used as a single or multi-transfer.
A2	32	I	Address select line 2.To select internal registers.
A1	33	I	Address select line 1.To select internal registers.
A0	34	I	Address select line 0.To select internal registers.
RXRDY*	38	O	Receive ready.(active low) This pin goes low when the receive FIFO is full. It can be used as a single or multi-transfer.
INTSEL	65	I	Interrupt type select. Enable /disable the interrupt three state function. Normal interrupt output can be selected by connecting this pin to VCC(MCR bit-3 does not have any effect on the interrupt output).The three state interrupt output is selected when this pin is left open or connected to GND and MCR bit-3 is to “1”.
INT A-B INT C-D	15.21 49.55	O	Interrupt output.(active high) this pin goes high (when enable by the interrupt enable register)whenever a receiver error. receiver data available. transmitter empty, or modem status condition flag is detected.
RTS*A-B RTS*C-D	14.22 48.56	O	Request to send.(active low) To indicate that the transmitter has data ready to send .Writing a “1” in the modem control register(MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR*A-B DTR*C-D	12.24 46.58	O	Data terminal ready. (active low) To indicate that IMP16C554 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0).writing a “1” at the MCR bit-0 will set the DTR* output to low.

SYMBOL DESCRIPTION

symbol	pin	Signal Type	Pin Description
			This pin will be set to high state after writing a “0” to that register or after the reset. Note that this pin does not have any effect on the transmit or receive operation.
RESET	37	I	Master reset.(active high)A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.
CTS*A-B CTS*C-D	11.25 45.59	I	Clear to send. (active low) The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR*A-B DSR*C-D	10.26 44.60	I	Data set ready. (active low) A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD*A-B CD*C-D	9.27 43.61	I	Carrier detect.(active low) A low on this pin indicates the carrier has been detected by the modem.
RI*A-B RI*C-D	8.28 42.62	I	Ring detect indicator. (active low) A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC VCC	13.30 47.64	I	Power supply input.

IMP16C554 ACCESSIBLE REGISTERS

A2A1A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	Modem status interrupt	Receive line status interrupt	Transmit holding register	Receive holding register
0 1 0	FCR	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA Mode select	XMITFIFO reset	RCVRFIFO reset	FIFO enable
0 1 0	ISR	0/FIFOs enabled	0/FIFOs enabled	0	0	int priority bit-2	Int priority bit-1	Int priority bit-0	Int status
0 1 1	LCR	Divisor latch enable	Set break	Set parity	Even parity	Parity enable	Stop bits	Word length bit-1	Word length bit-0
1 0 0	MCR	0	0	0	Loop back	INT enable	Not used	RTS*	DTR*
1 0 1	LSR	o/FIFO error	trans empty	trans holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

DLL and DLM are accessible only when LCR bit-7 is set to "1".

PROGAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding	Transmit Holding
0	0	1	Register	Register
0	1	0	Interrupt Status	Interrupt Enable Register
0	1	1	Register	FIFO Control Register
1	0	0		Line Control Register
1	0	1	Line Status Register	Modem Control Register
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	
0	0	0		Scratchpad Register
0	0	1		LSB of Divisor Latch
				MSB of Divisor Latch

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR).The status of the transmit hold register is provided in the Line status Register(LSR).Writing to this register (THR)will transfer the contents of data bus(D7-D0) to the Transmitter shift register is empty. The transmit holding register empty flag will be set to “1” when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit. the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled. receiver interrupt will occur as follows.

A)The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B)The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO dorps below the trigger level.

C)The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1;resetting IER BIT 3-0 to zero puts the IMP16C554 in the FIFO polled mode of operation. Since the receiver and

transmitter are controlled separately either one or both can in the polled mode operation by utilizing the Line status Register.

A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
B) LSR BIT4-1 will specify which error(s) has occurred.
C) LSR BIT-5 will indicate when the transmit FIFO is empty.
D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
E) LSR BIT-6 will indicate when there are any errors in the receive FIFO.

The MS16C554 requires to have two step FIFO enable operation in order to enable receive trigger levels.

PROGRAMMABLE BAUD RATE GENERATOR

The IMP16C554 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to 2_{16}-1.The output frequency of the Baud out* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIR-0
0=disable the receiver ready interrupt.
1=enable the receiver ready interrupt.
IER BIR-1
0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.
IER BIR-2
0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.
IER BIR-3
0=disable the modem status register interrupt.
1=enable the modem status register interrupt.
IER BIR7-4
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The IMP16C554 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the IMP16C554 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following sre the prioritized interrupt levels:

Priority level

P	D3	D2	C1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Received Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

*RECEIVE TIME-OUT:
This mode is enabled when the UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time out value is T (Time out length in bits)=4 X P (Programmed word length)+12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used)+number of stop bits and start bit.

Example-A: if user programs the word length=7,and no parity and one stop bit. Time out will be:T=4x7(programmed word length)+12=40 bits Character time =40 / 9 (programmed word length=7)+(stop bit=1)+(start bi=1)=4.4 characters.

Example-B: if user programs the word length=7,with parity and one stop bit, the time out will be: T=4x7 (programmed word length)+12=40 bits Character time =40 / 10 (programmed word length=7) + (parity=1) +

(stop bit=1) + (start bi=1) =4 characters.

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
1=no interrupt pending.

ISR BIT 1-3:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:
These bits are not used and are set to zero in MS16C450 mode. BIT 6-7:are set to "1" in MS16C554 mode.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:
0=Diosable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.
This is bit should be enabled before setting the FIFO trigger levels.

FCR BIT-1:
0=No change.
1=Clears the contents of receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:
0=No change.
1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:
0=No change.
1= Changes RXRDY and TXRDY pins from mode "0" to mode "1".

Transmit operation in mode "0":
When IMP16C554 is in MS16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1,FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When IMP16C554 is in IMP16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-1=1,FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode "1":
When IMP16C554 is in IMP16C550 mode (FCR bit-0=1,FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode "0":
When IMP16C554 is in IMP16C550 mode (FCR bit-0=1,FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when are no more characters in the FIFO.

FCR BIT 4-5:
Not used.

FCR BIT 6-7:
These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7

1	1	8

LCR BIT-2:
The number of stop bits can specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5, 6, 7	1
1	5	1-1/2
1	6, 7, 8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
0= no parity
1=a parity bit is generated during the transmission.
receiver also checks for received parity.
LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0= ODD parity bit is generated by forcing an odd number of 1`s in the transmitted data, receiver also checks for same format.
1=EVEN parity bit is generated by forcing an even number of 1`s in the transmitted data, receiver also checks for same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to “1” in the transmitted and received data.
LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to “0” in the transmitted and received data.

LCR BIT-6:
Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).
0= normal operating condition.
1=forces the transmitter output (TX) to go low to alert the communication terminal.
LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation.
1=select divisor latch register.

MODEM CONTROL REGISTER (MCR)
This register controls the interface with the MODEM or a peripheral device (RS232).
MCR BIT-0:
0=force DTR* output to high.
1=force DTR* output to low.
MCR BIT-1:
0=force RTS* output to high.
1=force RTS* output to low.

MCR BIT-2:
No used, except in internal loop-back mode.

MCR BIT-3:
0=set the INT A-D output pin to three state mode.
1=Enable the INT A-D output pin.

MCR BIT-4:
0=normal operation mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, MCR* bit-2 and INT enable are connected to modem control inputs.
In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control interrupts are also operational. but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:
Not used. Are set to zero permanently.
LINE STATUS REGISTER (LSR)
This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:
0=no overrun error (normal).
1= overrun error , next character arrived before receive holding register was emptied or if FIFOs are enabled. an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is over written, but it is not transferred to the FIFO.

LSR BIT-2:
0=no parity error (normal).
1= parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:
0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:
0=transmit holding register is full. IMP16C554 will not accept any data for transmission.
1= transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:
0=transmit holding register and shift register are full.
1=transmit holding register and shift register are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:
0= Normal.
1= At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)
This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to “1” whenever a control input from the MODEM changes state. They are set to “0” whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS* input to the IMP16C554 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR* input to the IMP16C554 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI* input to the IMP16C554 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD* input to the ST16C554 has changed state since the last time it was read.

MSR BIT-4
This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:
This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:
This bit is equivalent to MCR bit-2 during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:
This bit is equivalent to INT enable in the MCR during local loop-back mode. It is the compliment of the CD* input.

Note: whenever MSR BIT3-0: is set to logic “1”, a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)
IMP16C554 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	

19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

MSR	7=0
FCR	MSR BITS 0-3=0, MSR BITS 4-7=input signals FCR BIT 0-7=0

IMP16C554 EXTERNAL RESET CONDITION

REGISTER	RESET STATE
IER	IER BIT 0-7=0
ISR	ISR BIT-0=1, ISR BIT 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR,BIT

SIGNALS	RESET STATE
TX A-D	High
RTS* A-D	High
DTR* A-D	High
RXRDY*	High
TXRDY*	Low
INT A-D	Three state mode

AC ELECTRICAL CHARACTERISTICS

TA=0 –70^{0}C,Vcc= 5.0V±10% unless otherwise specified

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
T1	Clock high pulse duration	20			ns	
T2	Clock low pulse duration	20			ns	
T3	Clock rise/fall time			10	ns	
T8	Chip select setup time	5			ns	
T9	Chip setup time	0			ns	
T12	Data setup time	15			ns	
T13	Data hold time	15			ns	
T14	IOW* delay from chip select	10			ns	
T15	IOW* strobe width	50			ns	
T16	Chip select hold time from IOW*	0			ns	
T17	Write cycle delay	55			ns	
Tw	Write cycle =T15+T17	105			ns	
T19	Data hold time	15		25	ns	
T21	IOR* delay from chip select	10			ns	
T23	IOR* strobe width	65			ns	
T24	Chip select hold time from LOR*	0			ns	
T25	Read cycle delay	55			ns	
Tr	Read cycle =T23+T25	115			ns	
T26	Delay from IOR* to data			35	ns	100 pF load
T28	Delay from IOW* to output			50	ns	100 pF load
T29	Delay to set interrupt from MODEM input			70	ns	100 pF load
T30	Delay to reset interrupt from IOR*			70	ns	100 pF load
T31	Delay from stop to set interrupt			1Rck	ns	100 pF load
T32	Delay from IOR* to reset interrupt			200	ns	100 pF load
T33	Delay from initial INT reset to transmit start	8		24	*	
T34	Delay from stop to interrupt			100	ns	
T35	Delay from IOW* to reset interrupt			175	ns	
T44	Delay from stop to set RxRdy			1RCL		
T45	Delay from IOR* to reset RxRdy			K	us	
T46	Delay from IOW* to set TxRdy			1	ns	
T47	Delay from start to reset TxRdy			195	*	
				8		
N	Baud rate devisor	1		216-1		

Note 1: = Baudout cycle

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0^0C to $+70^0$ C
Storage temperature	-40^0 C to 150^0 C
Package dissipation	500 Mw

DC ELECTRICAL CHARACTERISTICS

TA=0*-70* C, Vcc= 5.0 V ±10% unless otherwise specified.

symbol	Parameter	Limits Min	Typ	Max	Units	conditions
VILCK	Clock input low level	-0.5		0.6	V	
VIHCK	Clock input high level	3.0		vcc	V	
VIL	Input low level	-0.5		0.8	V	
VIH	Input high level	2.2		vcc	V	
VOL	Output low level on all outputs			0.4	V	LOL=6 mA
VOH	Output high level	2.4			V	LOH=-6 mA
ICC	Avg power supply current		6	14	mA	
IIL	Input leakage			±10	uA	
ICL	Clock leakage			±10	uA	
VILCK	Clock input low level	-0.3		0.8	V	VCC=3.0 V
VIHCK	Clock input high level	2.4		vcc	V	VCC=3.0 V
VIL	input low level	-0.3		0.8	V	V CC =3.0 V
VIH	input high level	2.0		vcc	V	Vcc=3.0V
VOL	Output low level on all outputs			0.4	V	VCC=3.0V, loL=8.5 mA
VOH	output high level	2.0			V	VCC=3.0V, loH=-4 mA
ICC	Avg power supply current		10	12	mA	VCC=3.0 V

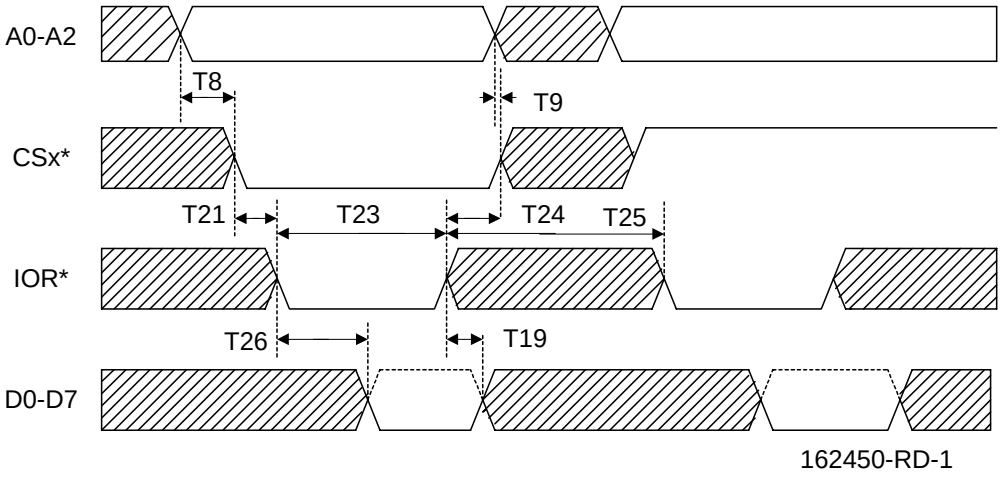


FIGURE 1 - GENERAL READ TIMING

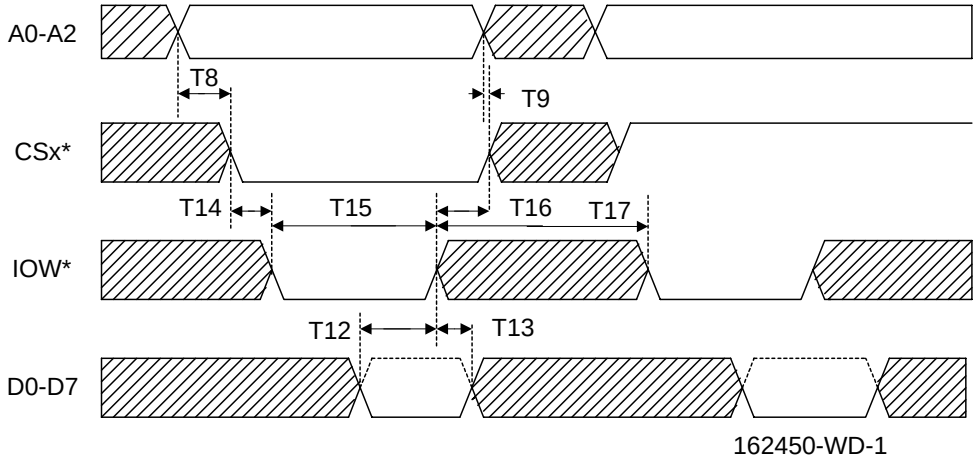


FIGURE 2 - GENERAL WRITE TIMING

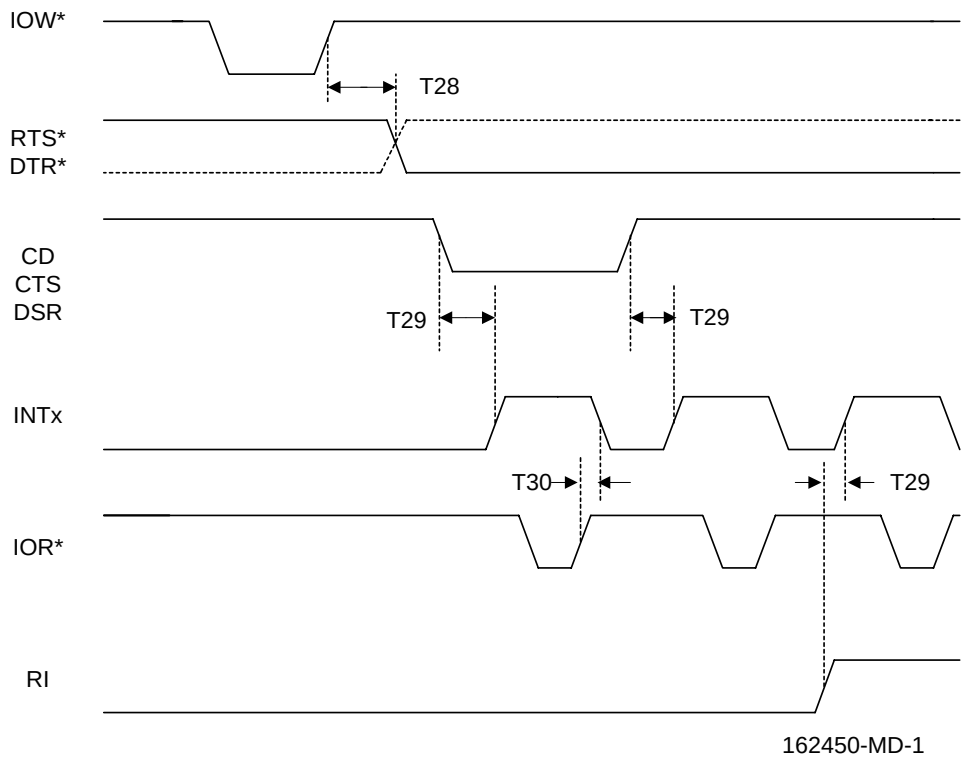


FIGURE 3 - MODEM TIMING

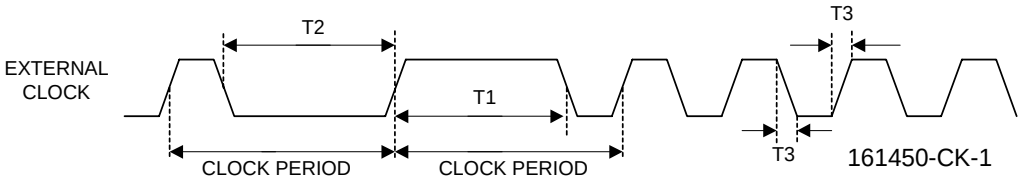


FIGURE 4 - CLOCK TIMING

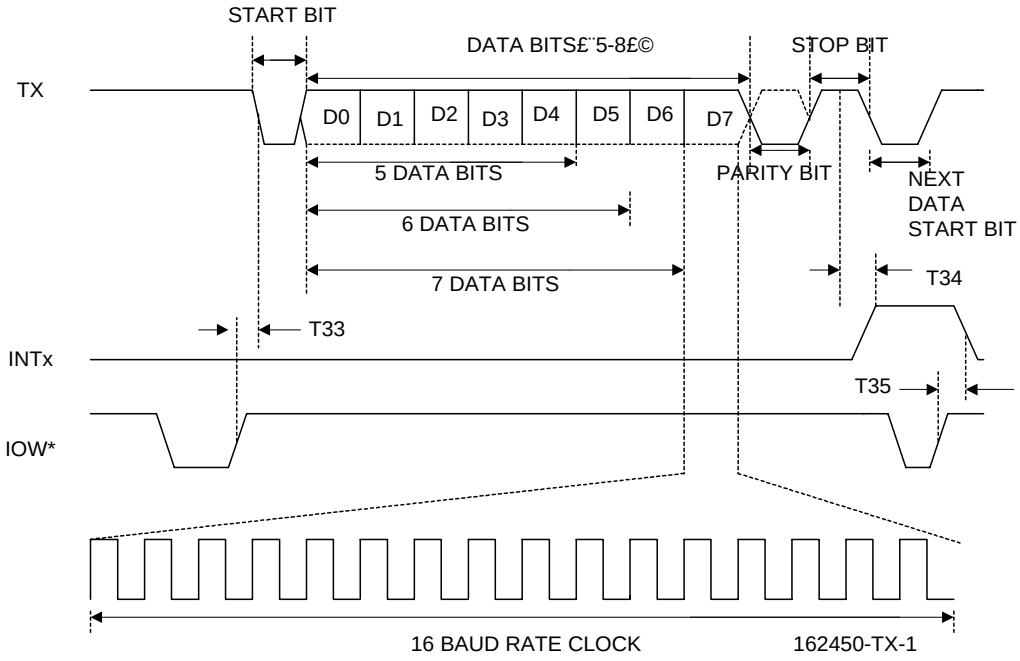


FIGURE 5

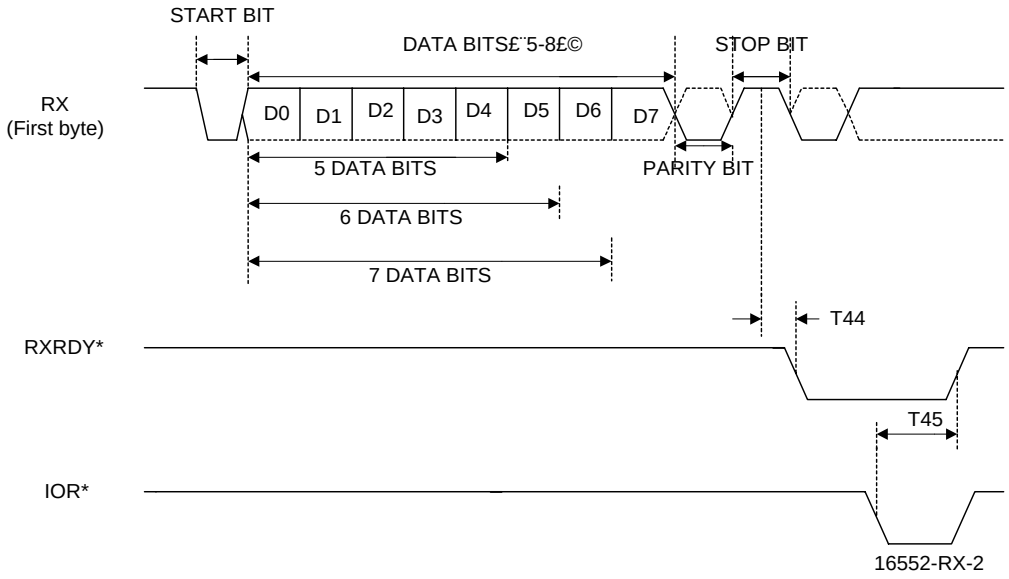


FIGURE 6 - RXRDY TIMING FOR MODE "0"

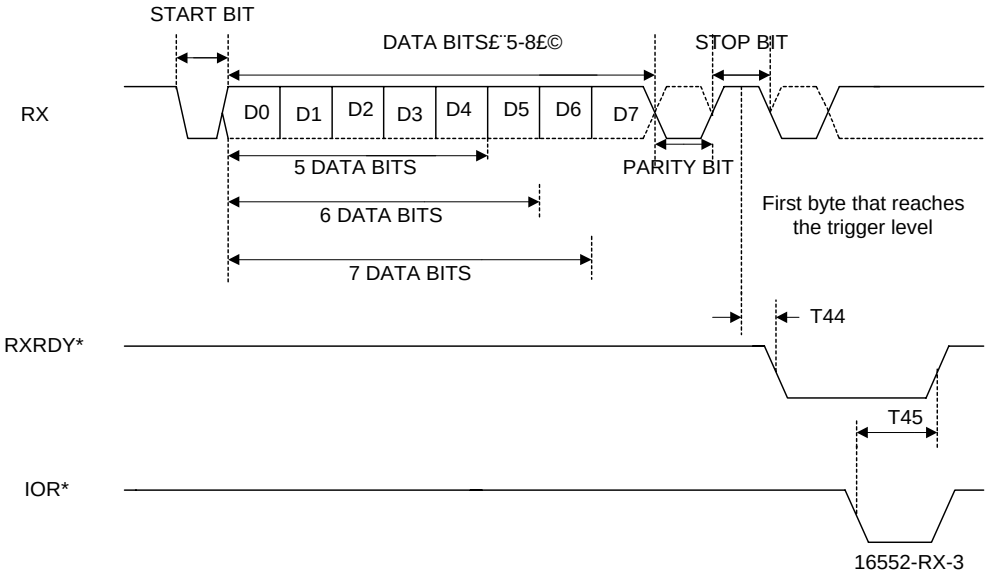


FIGURE 7 - RXRDY TIMING FOR MODE " 1"

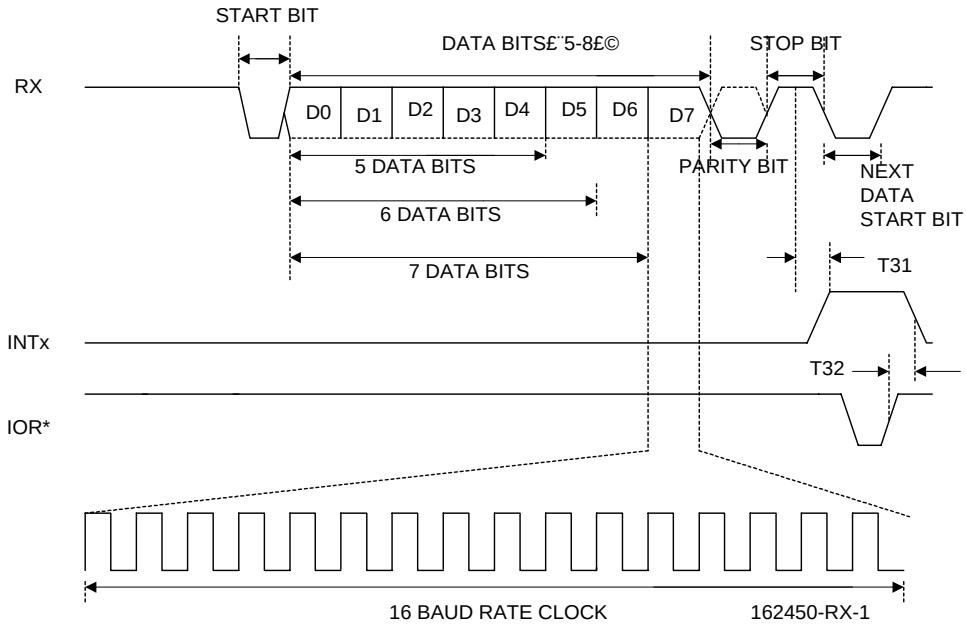


FIGURE 8 - RECEIVE TIMING

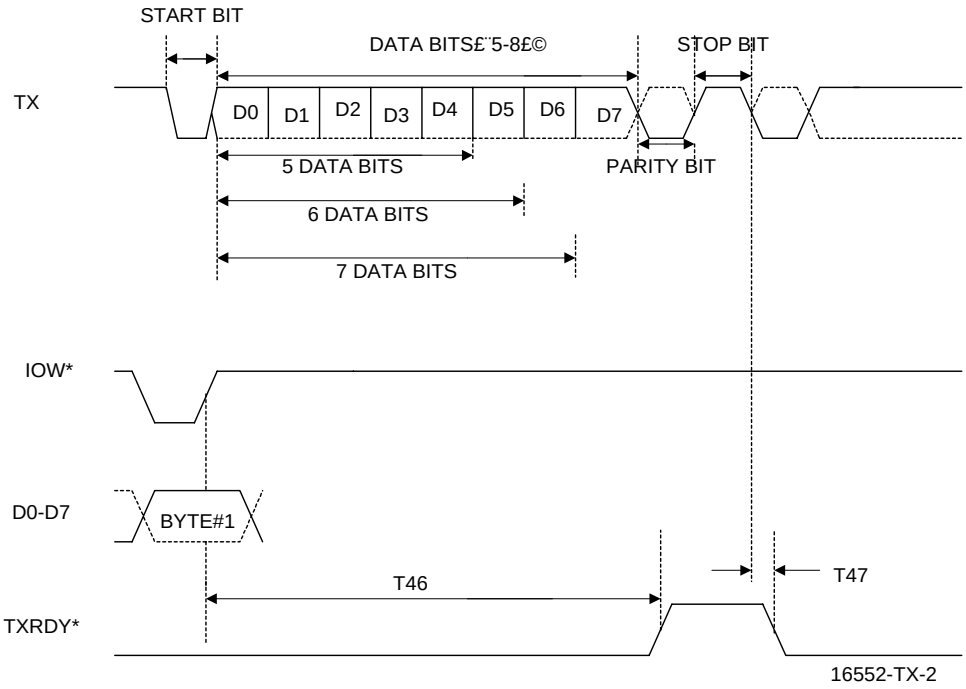


FIGURE 9 - TXRDY TIMING FOR MODE " 0"

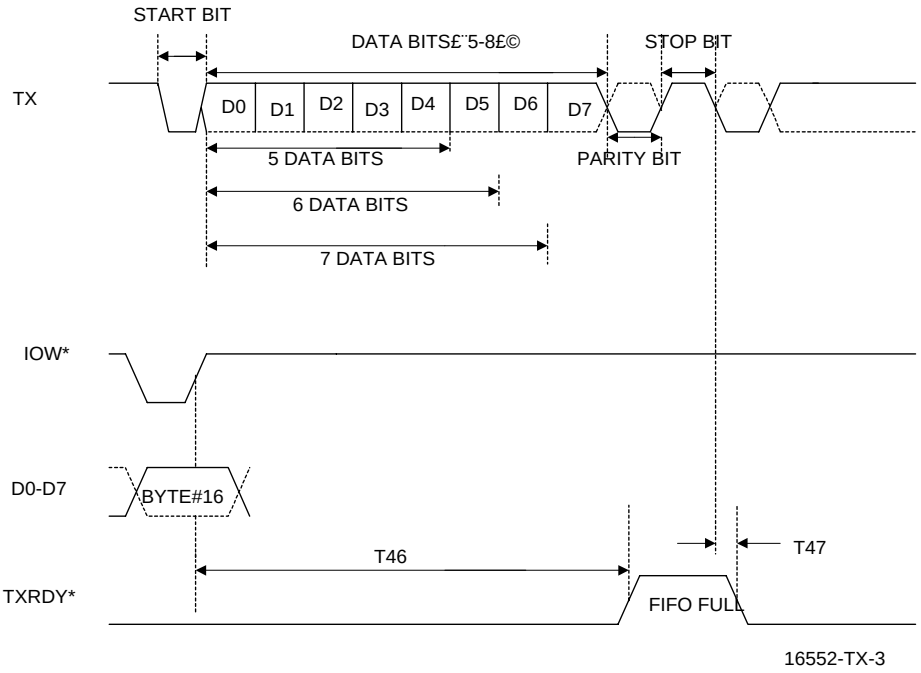


FIGURE 10 - TXRDY TIMING FOR MODE " 1"

Ordering Information

Part Number	Package	Operating Temperature
IMP16C554-CJ68	PLCC 68pins	0 to +70
IMP16C554-LJ68	PLCC 68pins	-40 to +85

Life Support Policy: IMP's products are not to be used in life support devices without prior written authorization.

IMP Retains the right to make changes to these specifications at any time without notice.