ISO 9001 Registered

# IMP3522D

## ADAPTIVE BALLAST CONTROL IC

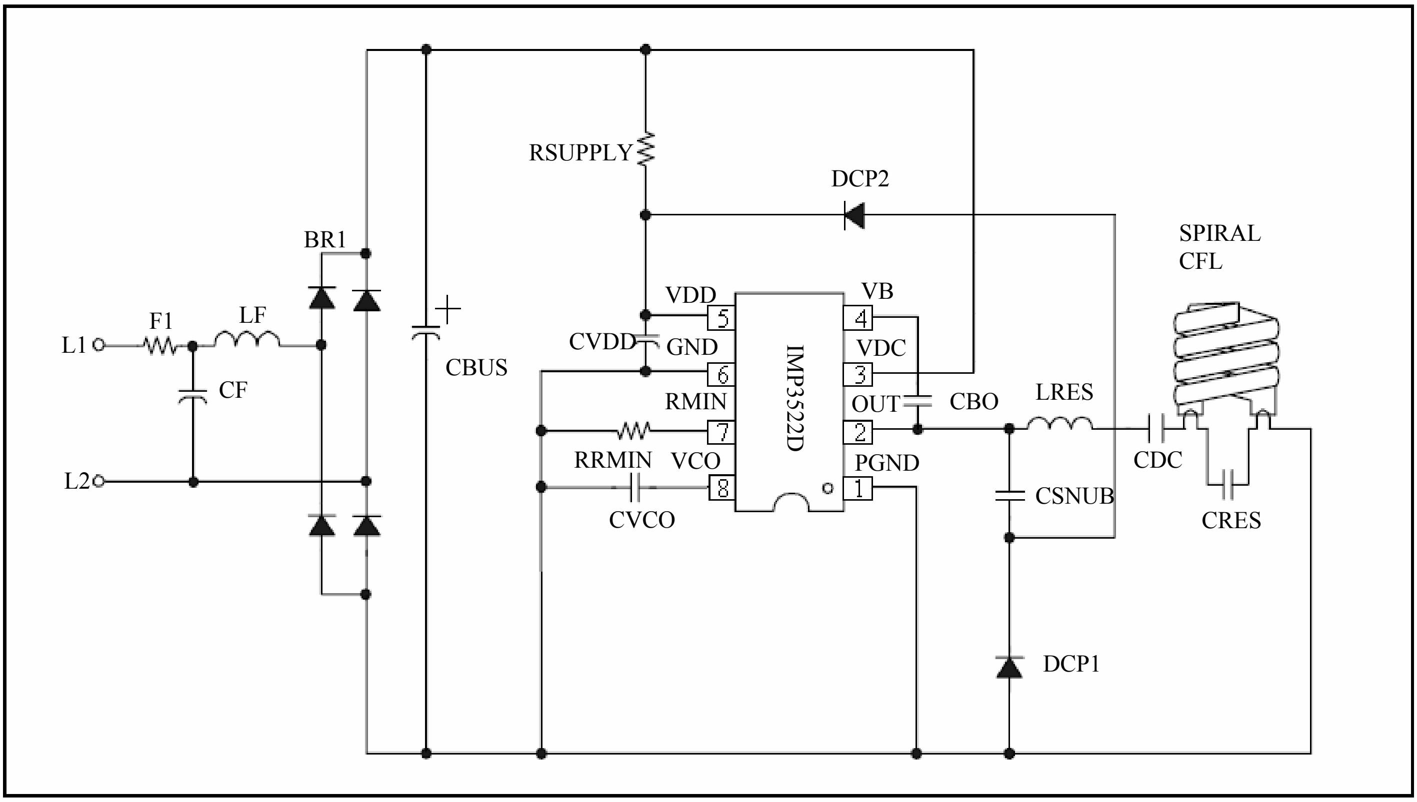
### General Description

The IMP3522D(S) is a complete adaptive ballast controller, 450V half-bridge driver and power MOS FET integrated into a single IC for Compact Fluorescent Lamps (CFL) applications. The IC includes adaptive zero-voltage switching (ZVS), internal crest factor over-current protection, as well as an integrated bootstrap FET. The heart of this IC is a voltage controlled oscillator with externally programmable minimum frequency. All of the necessary ballast features are integrated in a small 8-pin DIP package.

### Key Features

- -450V Half Bridge Driver
- -Integrated Bootstrap FET
- -Integrated Power MOS FET
- -Adaptive zero-voltage switching (ZVS)
- -Internal Crest Factor Over-Current Protection
- -0 to 6VDC Voltage Controlled Oscillator
- -Programmable minimum frequency
- -Micropower Startup Current (80uA)
- -Internal 15.6V zener clamp on $V_{DD}$
- -Small DIP8 Package
- -Also available LEAD-FREE (PbF)

### Typical Application



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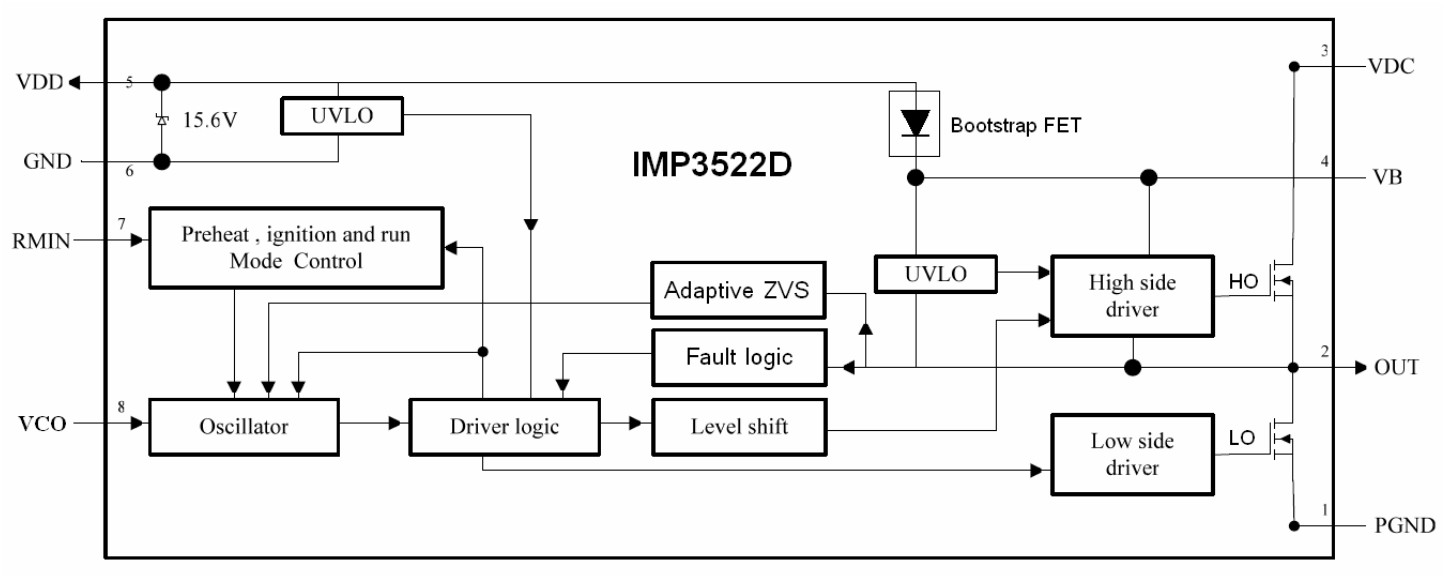
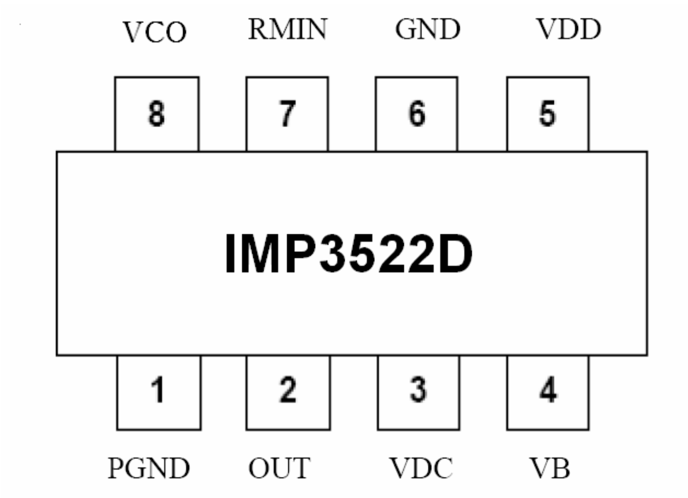
## Block Diagram




## Pin Assignments




| Pin # | Name | Description |
|---|---|---|
| 1 | PGND | Power ground |
| 2 | OUT | Half bridge output |
| 3 | VDC | High-voltage supply |
| 4 | VB | High-side floating supply |
| 5 | VDD | Supply voltage |
| 6 | GND | Signal ground |
| 7 | RMIN | Oscillator frequency set resistor |
| 8 | VCO | Preheating time set capacitor |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A$=25°C unless otherwise.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_B$ | High-side floating supply | -0.3 | | 475 | V |
| $V_{OUT}$ | Half bridge output | -0.3 | | 450 | |
| $V_{IN}$ | RMIN pins input voltage | -0.3 | | 7 | |
| $I_{VCO}$ | Voltage controlled oscillator input current (Note 1) | -5 | | 5 | mA |
| $I_{CL}$ | Clamping current level (Note 2) | -25 | | 25 | mA |
| $dV_{OUT}/dt$ | Allowable offset voltage slew rate | -50 | | 50 | V/ns |
| $T_A$ | Operating temperature range | -25 | | 125 | °C |
| $T_{STG}$ | Storage temperature range | -65 | | 150 | |
| $T_L$ | Lead temperature (soldering,10 seconds) | | | 300 | |

Note 1: This IC contains a zener clamp structure between the chip VCO and GND, which has a nominal breakdown voltage of 6V. Please note that this pin should not be driven by a DC, low impedance power source greater than 6V.

Note 2: This IC contains a zener clamp structure between the chip VDD and GND, which has a nominal breakdown voltage of 15.6V. Please note that this supply pin should not be driven by a DC, low impedance power source greater than the VCLAMP specified in the Electrical Characteristics section.

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions.

| Symbol | Definition | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$-$V_{out}$ | High side floating supply voltage | $V_{DD}$ - 0.7 | $V_{CLAMP}$ | V |
| $V_{OUT}$ | Steady state high side floating supply offset voltage | -1 | 450 | |
| $V_{DD}$ | Supply voltage | $V_{DDUV+}$ | $V_{CLAMP}$ | |
| $I_{DD}$ | Supply current | Note 3 | 10 | mA |
| $R_{RMIN}$ | Minimum frequency setting resistance | 20 | 140 | kΩ |
| $V_{VCO}$ | VCO pin voltage | 0 | 5 | V |
| $T_J$ | Junction temperature | -25 | 125 | ℃ |

Note 3: Enough current should be supplied into the VDD pin to keep the internal 15.6V zener clamp diode on this pin regulating its voltage, VCLAMP.

## Electrical Characteristic

$V_{DD} = V_{BO} = V_{BIAS}$ = 14V +/- 0.25V, RRMIN = 82kΩ and TA = 25°C unless otherwise specified.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| **Supply Characteristics** | | | | | | |
| $V_{DDUV+}$ | $V_{CC}$ and $V_{BO}$ supply undervoltage positive going threshold | 11.4 | 12.6 | 13.8 | V | $V_{DD}$ rising from 0V |
| $V_{DDUV-}$ | $V_{DD}$ and $V_{BO}$ supply undervoltage negative going threshold | 9.0 | 10.0 | 11.0 | V | |
| $V_{UVHYS}$ | $V_{DD}$ supply undervoltage lockout hysteresis | — | 2.7 | — | V | |
| $I_{QDDUV}$ | UVLO quiescent current | — | 45 | 80 | µA | $V_{DD}$ = 10V |
| $I_{QDDFLT}$ | Fault mode quiescent current | — | 100 | — | µA | |
| $I_{DDHF}$ | $V_{DD}$ supply current f=85KHz | — | 4.5 | — | mA | $V_{VCO}$=0V |
| $I_{DDLF}$ | $V_{DD}$ supply current f=35KHz | — | 2.0 | — | mA | $V_{VCO}$=6V |
| $V_{CLAMP}$ | $V_{DD}$ Zener clamp voltage | 14.4 | 15.4 | — | V | $I_{DD}$ = 10mA |
| **Floating Supply Characteristics ($V_B$-$V_{out}$)** | | | | | | |
| $I_{QBO0}$ | Quiescent $V_{BO}$ supply current | — | 80 | 150 | µA | $V_{DD}$=10V, $V_{BO}$=14V |
| $I_{QBOUV}$ | Quiescent $V_{BO}$ supply current | — | 20 | 40 | µA | $V_{DD}$=10V, $V_{BO}$=7V |
| $V_{BOUV+}$ | $V_{BO}$ supply undervoltage positive going threshold | 7.7 | 9.0 | 10.3 | V | |
| $V_{BOUV-}$ | $V_{BO}$ supply undervoltage negative going threshold | 6.8 | 8.0 | 9.2 | V | |
| **Oscillator I/O Characteristics** | | | | | | |
| $f_{(min)}$ | Minimum oscillator frequency (Note 4) | 30 | 36 | 40 | kHz | $V_{VCO}$=6V |
| $f_{(max)}$ | Maximum oscillator frequency (Note 4) | 70 | 90 | 100 | kHz | $V_{VCO}$=0V |
| D | Oscillator duty cycle | — | 50 | — | % | |
| $I_{VCOQS}$ | $I_{VCO}$ quick start | — | 80 | — | µA | $V_{VCO}$=0V |
| $I_{VCOFS}$ | $I_{VCO}$ frequency sweep | 0.8 | 1.6 | 2.0 | µA | $V_{VCO}$=2V |
| $I_{VCO\_5V}$ | $I_{VCO}$ when VCO is at 5V | — | 1.1 | — | µA | |
| $V_{VCO\_max}$ | Maximum VCO voltage | — | 6 | — | V | |
| **Protection Characteristics** | | | | | | |
| $V_{VCO\_RUN}$ | VCO voltage when entering run mode | — | 4.8 | — | V | |
| CSCF | Crest factor peak-to-average fault factor | — | 5.0 | — | N/A | $V_{OUT}$ offset = 0.5V |
| $V_{OUT\_OFFSET\_MAX}$ | Maximum crest factor VOUT offset voltage | — | 3.0 | — | V | |
| $V_{VCOSD}$ | $V_{VCO}$ shutdown voltage | 0.74 | 0.82 | 0.91 | V | |
| **Minimum Frequency Setting Characteristics** | | | | | | |
| $V_{RMIN}$ | RMIN lead voltage during normal operation | 4.8 | 5.1 | 5.4 | V | |
| $V_{RMINFLT}$ | RMIN lead voltage during fault mode | — | 0 | — | V | |
| **Bootstrap FET** | | | | | | |
| IBO1 | VB current | 30 | 70 | — | mA | $C_{BO}$=0.1uF, $V_{OUT}$=0V |
| IBO2 | VB current | 10 | 20 | — | mA | VBO = 10V |

Note 4: Frequency shown is nominal for RRMIN=82kΩ. Frequency can be programmed higher or lower with the value of $R_{RMIN}$.

## Application Information

**Under-voltage Lock-Out Mode**

The under-voltage lock-out mode (UVLO) is defined as the state the IMP3522D is in when VDD is below the turn-on threshold of the IC. The IMP3522D UVLO is designed to maintain an ultra-low supply current ($I_{QDDUV}$<80uA), and to guarantee that the IMP3522D is fully functional before the high- and low-side output gate drivers are activated. The VDD capacitor, CVDD, is charged by current through supply resistor, RSUPPLY, minus the start-up current drawn by the IMP3522D (Figure 1). This resistor is chosen to provide sufficient current to supply the IMP3522D from the DC bus. Once the capacitor voltage on VDD reaches the start-up threshold, $V_{DDUV+}$, the IMP3522D turns on and HO and LO start oscillating. Capacitor CVDD should be large enough to hold the voltage at VDD above the $V_{DDUV+}$, threshold for one half -cycle of the line voltage or until the external auxiliary supply can maintain the required supply voltage and current to the IC.

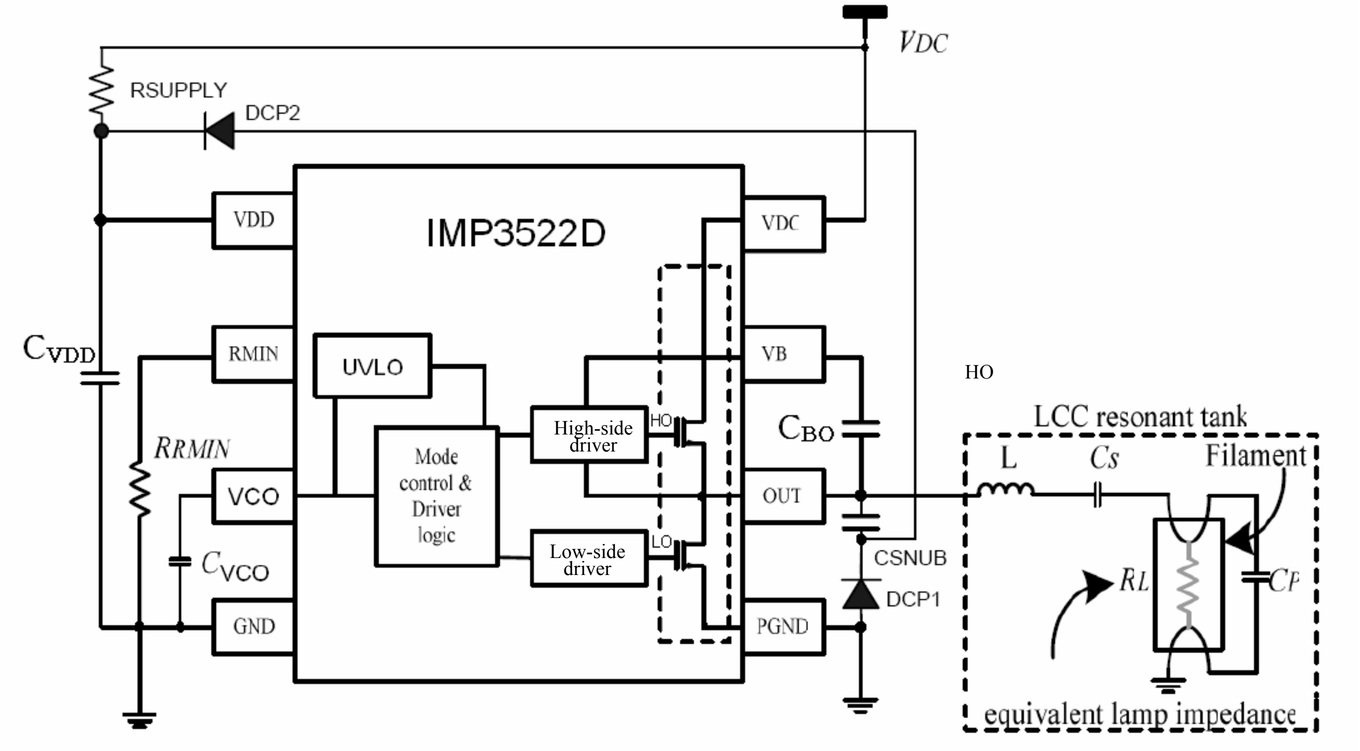



**Fig. 1 Start-up circuitry**

An internal bootstrap MOSFET between VDD and VB and external supply capacitor, CBO, determine the supply voltage for the high-side driver circuitry. An external charge pump circuit consisting of capacitor CSNUB and diodes DCP1 and DCP2, comprises the auxiliary supply voltage for the low-side driver circuitry. To guarantee that the high-side supply is charged up before the first pulse on pin HO, the first pulse from the output drivers comes from the LO pin. LO may oscillate several times until VB-VOUT exceeds the high-side UVLO rising threshold, $V_{BOUV+}$ (9 Volts), and the high-side driver is enabled. During UVLO mode, the high- and low-side gate driver outputs, HO and LO, are both low and pin VCO is pulled down to GND for resetting the starting frequency to the maximum.

## Application Information (Continued)

**Frequency Sweep Mode**

When VDD exceeds $V_{DDUV+}$ threshold, the IMP3522D enters frequency sweep mode. An internal current source (Figure2) charges the external capacitor on pin VCO, CVCO, and the voltage on pin VCO starts ramping up linearly. An additional quick-start current ($I_{VCOQS}$) is also connected to the VCO pin and charges the VCO pin initially to 0.85V. When the VCO voltage exceeds 0.85V, the quick-start current is then disconnected internally and the VCO voltage continues to charge up with the normal frequency sweep current source ($I_{VCOFS}$) (Figure 3). This quick-start brings the VCO voltage quickly to the internal range of the VCO.

The frequency ramps down towards the resonance frequency of the high-Q ballast output stage causing the lamp voltage and load current to increase. The voltage on pin VCO continues to increase and the frequency keeps decreasing until the lamp ignites. If the lamp ignites successfully, the voltage on pin VCO continues to increase until it internally limits at 6V ($V_{VCO\_MAX}$). The frequency stops decreasing and stays at the minimum frequency as programmed by an external resistor, RRMIN, on pin RMIN. The minimum frequency should be set below the high-Q resonance frequency of the ballast output stage to ensure that the frequency ramps through resonance for lamp ignition (Figure 4). The desired preheat time can be set by adjusting the slope of the VCO ramp with the external capacitor CVCO.

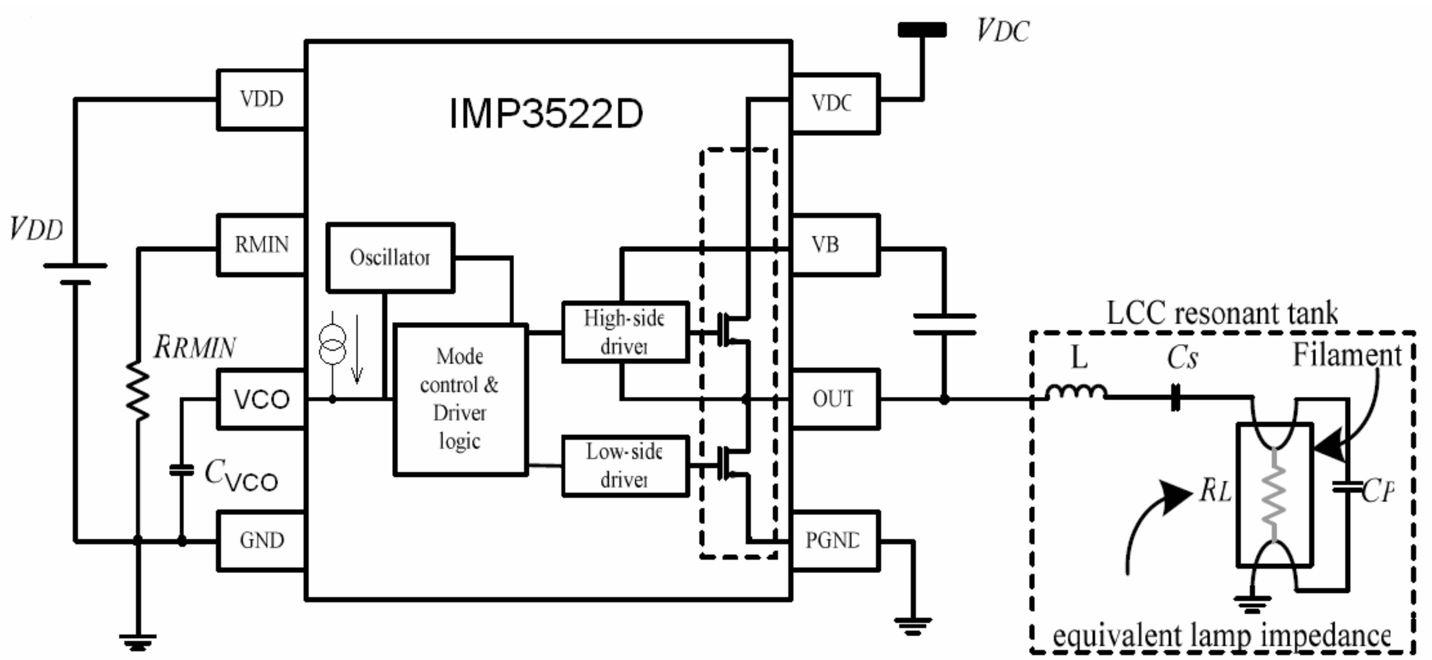



**Fig. 2 Frequency sweep circuitry mode circuitry**

## Application Information (Continued)

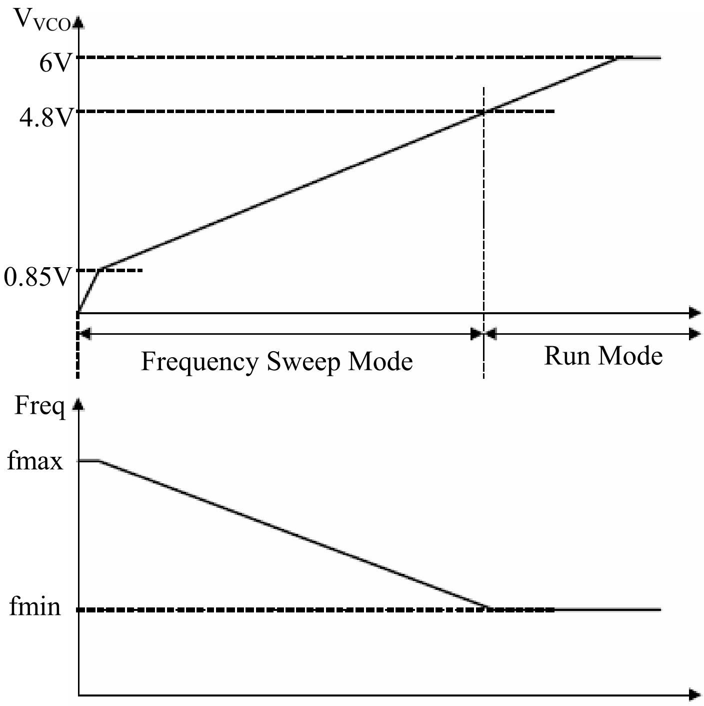



**Fig. 3 IMP3522D Frequency sweep mode timing diagram.**

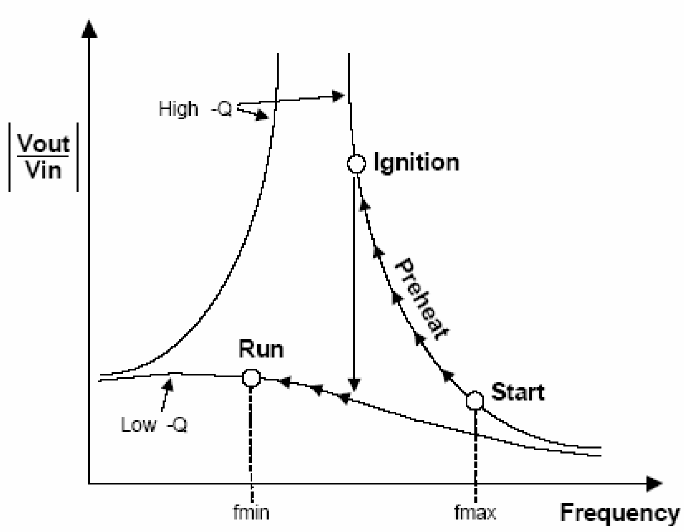



**Fig. 4 Resonant tank Bode plot with lamp operating points.**

**Run Mode**

The IMP3522D enters RUN mode when the voltage on pin VCO exceeds 4.8V ($V_{VCO\_RUN}$). The lamp has ignited and the ballast output stage becomes a low-Q, series-L, parallel- RC circuit. Also, the VOUT sensing and fault logic blocks (Figure 5) both become enabled for protection against non- ZVS and over-current fault conditions. The voltage on the VCO pin continues to increase and the frequency deceases further until the VCO pin voltage limits at 6V ($V_{VCO\_MAX}$) and the minimum frequency is reached. The resonant inductor, resonant capacitor, DC bus voltage and minimum frequency determine the running lamp power. The IC stays at this minimum frequency unless non-ZVS occurs at the OUT pin, a crest factor over-current condition is detected at the OUT pin, or VDD decreases below the UVLO- threshold (see State Diagram).

## Application Information (Continued)

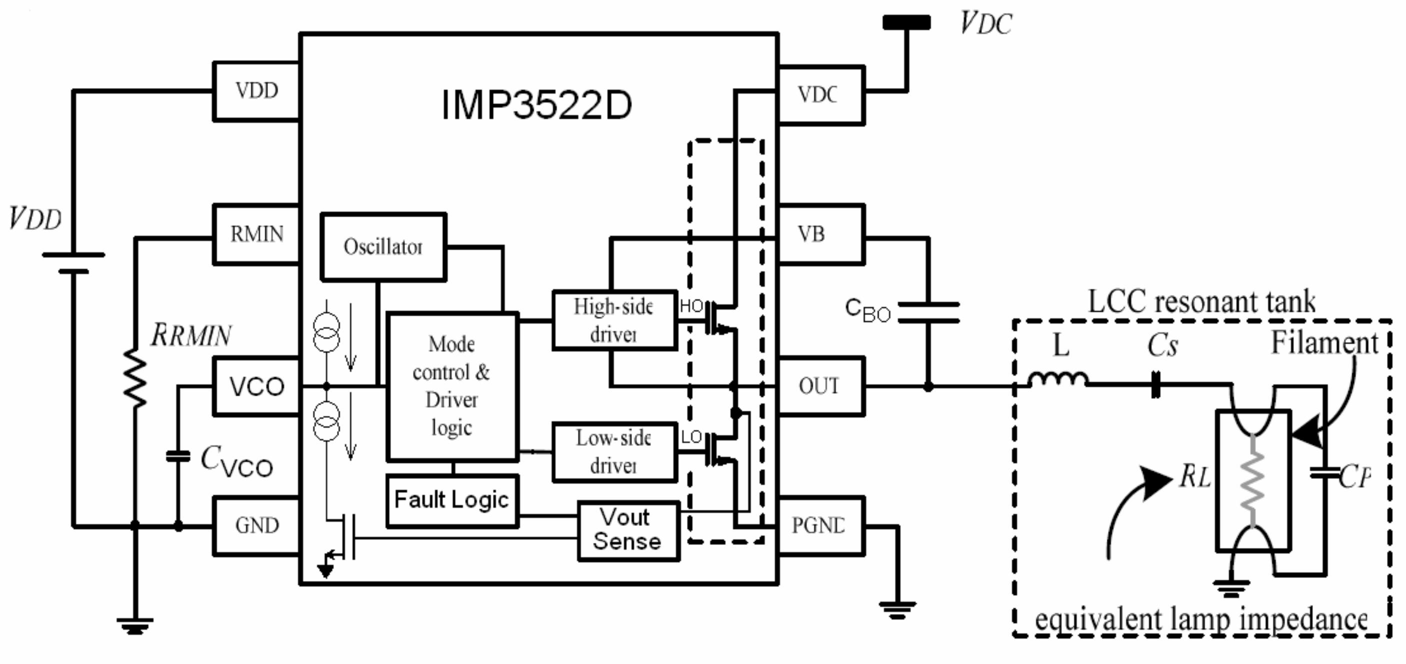



**Fig. 5 IMP3522D Run mode circuitry.**

**Non Zero-Voltage Switching (ZVS) Protection**

During run mode, if the voltage at the OUT pin has not slewed entirely to GND during the dead-time such that there is voltage between the drain and source of the lowside half-bridge MOSFET when LO turns-on, then the system is operating too close to, or, on the capacitive side of, resonance. The result is non-ZVS capacitive-mode switching that causes high peak currents to flow in the half-bridge MOSFETs that can damage or destroy them (Figure 6). This can occur due to a lamp filament failure(s), lamp removal (open circuit), a dropping DC bus during a mains brown-out or mains interrupt, lamp variations over time, or component variations. To protect against this, an internal high-voltage MOSFET is turned on at the turn-off of HO and the VOUT-sensing circuit measures VOUT at each rising edge of LO. If the VOUT voltage is non-zero, a pulse of current is sinked from the VCO pin (Figures 5 and 6) to slightly discharge the external capacitor, CVCO, causing the frequency to increase slightly. The VCO capacitor then charges up during the rest of the cycle slowly due to the internal current source.

The frequency is trying to decrease towards resonance by charging the VCO capacitor and the adaptive ZVS circuit "nudges" the frequency back up slightly above resonance each time non-ZVS is detected at the turn-on of LO. The internal high-voltage MOSFET is then turned off at the turn-off of LO and it withstands the high-voltage when VOUT slews up to the DC bus potential. The circuit then remains in this closed-loop adaptive ZVS mode during running and maintains ZVS operation with changing line conditions, component tolerance variations and lamp/load variations. During a lamp removal or filament failure, the lamp resonant tank will be interrupted causing the half-bridge output to go open circuit (Figure 7). This will cause capacitive switching (hard-switching) resulting in high peak MOSFET currents that

## Application Information (Continued)

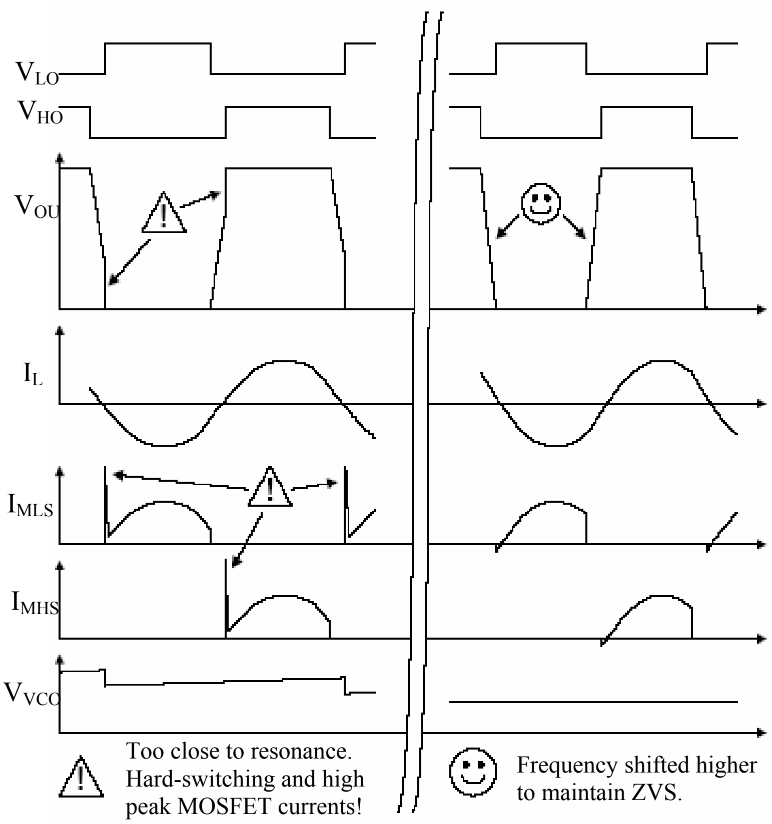



**Fig. 6 IMP3522D non-ZVS protection timing diagram.**

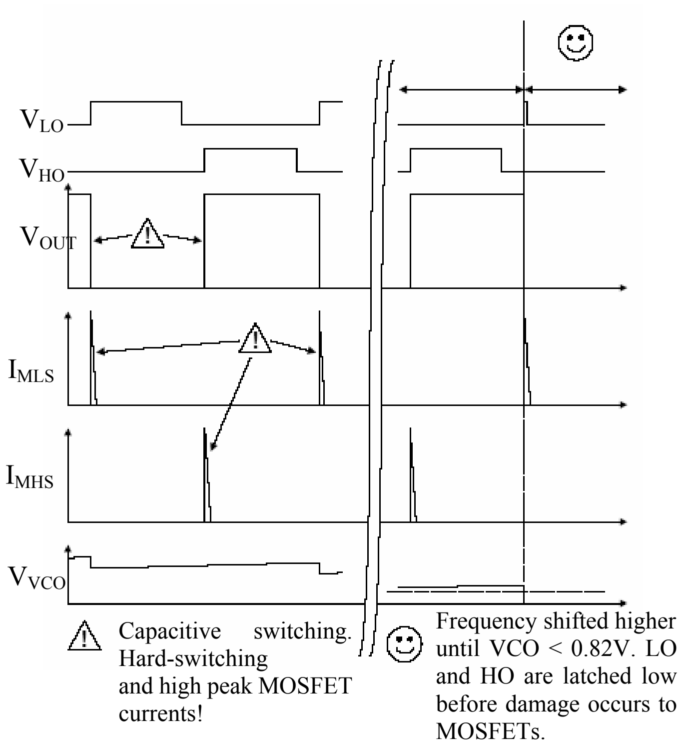



**Fig. 7 Lamp removal or open filament fault condition timing diagram**

can damage them. The IMP3522D will increase the frequency in attempt to satisfy ZVS until the VCO pin decreases below 0.82V ($V_{VCOSD}$). The IC will enter Fault Mode and latch the LO and HO gate driver outputs 'low' for turning the half-bridge off safely before any damage can occur to the MOSFETs.

**Crest Factor Over-current Protection**

During normal lamp ignition, the frequency sweeps through resonance and the output voltage increases across the resonant capacitor and lamp until the lamp ignites. If the lamp fails to ignite, the resonant capacitor voltage, the inductor voltage and inductor current will continue to increase until the inductor saturates or the output voltage exceeds the maximum voltage rating of the resonant capacitor or inductor. The ballast must shutdown before damage occurs. To protect against a lamp non-strike fault condition, the IMP3522D uses the VOUT-sensing circuitry (Figure 5) to also measure the low-side half-bridge MOSFET current for detecting an over-current fault. By using the RDSon of the lowside MOSFET for current sensing and the VOUT-sensing circuitry, the IMP3522D eliminates the need for an

## Application Information (Continued)

additional current sensing resistor, filter and current-sensing pin. To cancel changes in the RDSon value due to temperature and MOSFET variations, the IMP3522D performs a crest factor measurement that detects when the peak current exceeds the average current by a factor of 5 (CSCF). Measuring the crest factor is ideal for detecting when the inductor saturates due to excessive current that occurs in the resonant tank when the frequency sweeps through resonance and the lamp does not ignite. When the VCO voltage ramps up for the first time from zero, the resonant tank current and voltages increase as the frequency decreases towards resonance (Figure 8). If the lamp does not ignite, the inductor current will eventually saturate but the crest factor fault protection is not active until the VCO voltage exceeds 4.8V ($V_{VCO\_RUN}$) for the first time. The frequency will continue decreasing to the capacitive side of resonance towards the minimum frequency setting and the resonant tank current and voltages will decrease again. When the VCO voltage exceeds 4.8V ($V_{VCO\_RUN}$), the IC enters Run Mode and the non-ZVS protection and crest factor protection are both enabled. The non-ZVS protection will increase the frequency again cycle-by-cycle towards resonance from the capacitive side. The resonant tank current will increase again as the frequency nears resonance until the inductor saturates again.

The crest factor protection is now enabled and measures the instantaneous voltage at the OUT pin only during the time when LO is 'high' and after an initial 1us blank time from the rising edge of LO. The blank time is necessary to prevent the crest factor protection circuit from reacting to a non- ZVS condition. An internal averaging circuit averages the instantaneous voltage at the OUT pin over 10 to 20 switching cycles of LO. During Run Mode, the first time the inductor saturates when LO is 'high' (after the 1us blank time) and the peak current exceeds the average by 5 (CSCF), the IMP3522D will enter Fault Mode and both LO and HO outputs will be latched 'low'. The half-bridge will be safely disabled before any damage can occur to the ballast components.

The crest factor peak-to-average fault factor varies as a function of the internal average (Figure 20). The maximum internal average should be below 3.0 volts. Should the average exceed this amount, the multiplied average voltage can exceed the maximum limit of the VOUT sensing circuit and the VOUT sensing circuit will no longer detect crest factorfaults. This can occur when a half-bridge MOSFET is selected that has an RDSon that is too large for the application causing the internal average to exceed the maximum limit.

**FAULT MODE**

During Run Mode, should the VCO voltage decrease below 0.82V ($V_{VCOSD}$) or a crest factor fault occur, the IMP3522D will enter Fault Mode (see State Diagram). The LO and HO gate driver outputs are both latched 'low' so that the half-bridge is disabled. The VCO pin is pulled low to GND and the RMIN pin decreases from 5V to GND. VDD draws micro -power current ($I_{DDFLT}$) so that VDD stays at the clamp voltage and the IC remains in Fault Mode without the need for the charge-pump auxiliary supply. To exit Fault Mode and return to Frequency Sweep Mode, VDD must be cycled below the UVLO- threshold and back above the UVLO+ threshold.

## Application Information

(Continued)

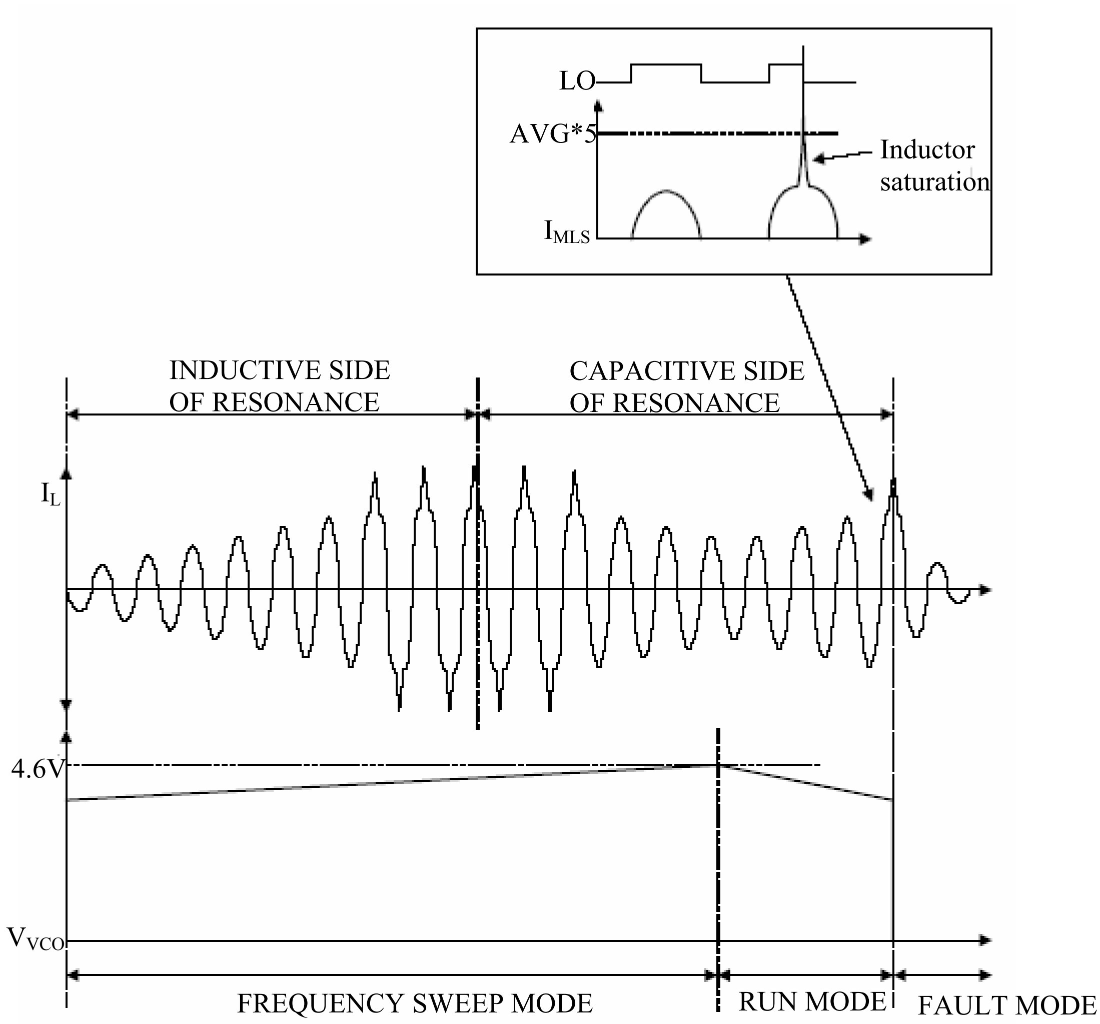
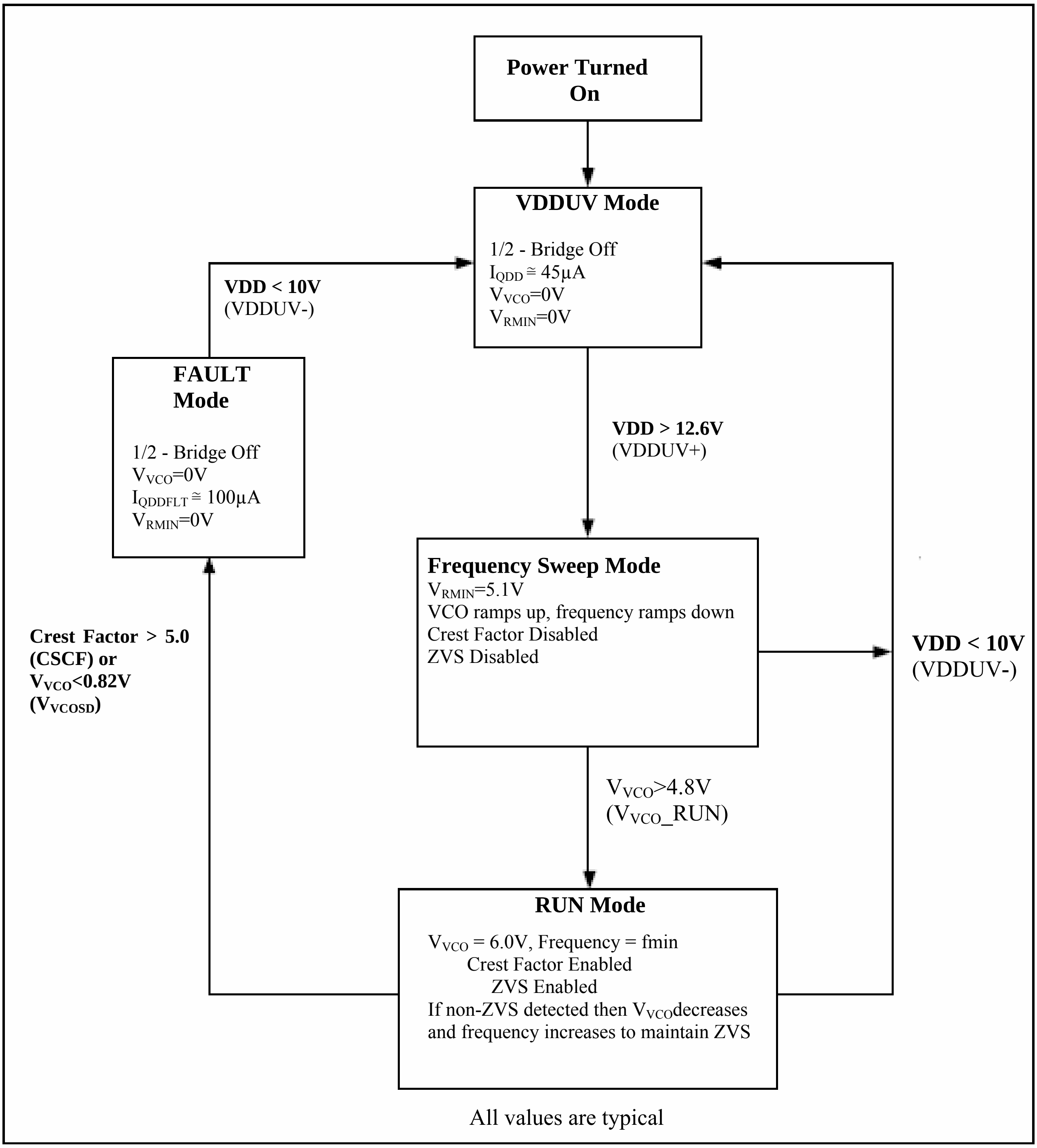


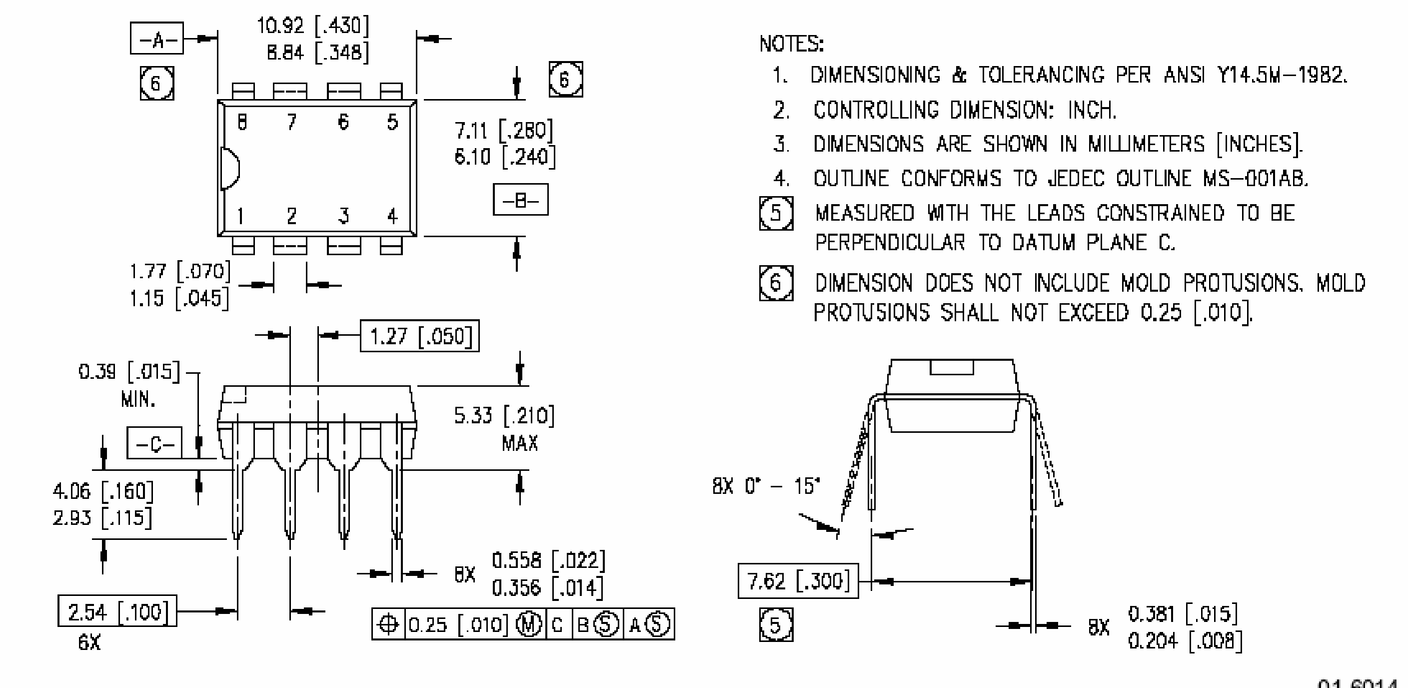

**Fig. 8 Crest factor protection timing diagram**

## State Diagram



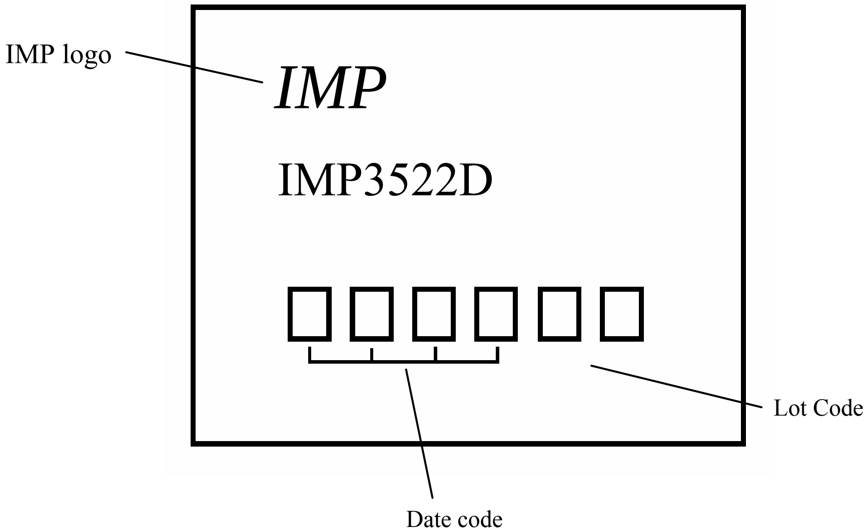
# ADAPTIVE BALLAST CONTROL IC

## Mechanical Dimensions




IMP3522D 8-Lead PDIP

## Leadfree part marking information



## ORDER INFORMATION

**Basic Part (Non-Lead Free)**

8-Lead PDIP IMP3522D order IMP3522D

**Leadfree Part**

8-Lead PDIP IMP3522D order IMP3522DPbF

**ISO 9001 Registered**

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